NAND Flash Part Numbering System

Micron's part numbering system is available at www.micron.com/support/designsupport/documents/png

	MT	29F	2G	08	Α	Α	Α	Α	Α	WP -	XX	ХX	x	ES	: A	<u> </u>
licron Technology																Design Revision (shrink)
ngle-Supply Flash																Production Status
= NAND Flash																Blank = Production
E = Enterprise NAND Flash																ES = Engineering Samples
·																QS = Qualification Samples
nsity																MS = Mechanical Sample
= 1Gb				-												
= 2Gb																Features
= 4Gb																E = Internal ECC enabled
= 8Gb																M = Media
i = 16Gb																R = FortisFlash features
i = 32Gb																S = Security features
i = 64Gb G = 128Gb																X = Product Longevity Program
G = 128Gb G = 256Gb																Z = Polyimide (if applicable)
G = 384Gb																Operating Temperature Range*
G = 512Gb																Blank = Commercial (0°C to +70°C)
= 1024Gb																AAT = Automotive Grade (-40°C to +105°C)
= 1152Gb																AIT = Automotive Industrial (-40°C to +85°C)
T = 1536Gb																IT = Extended (-40°C to +85°C) (AKA ET)
= 2048Gb																WT = Wireless Temp (-25°C to +85°C)
= 3072Gb																*Wafers support only the 0°C to +70°C temperature range
= 4096Gb																
= 6144Gb																Speed Grade
																Blank = Async only
vice Width = 1 bit					1											12 = 166 MT/s 10 = 200 MT/s
= 1 DIT = 8 bits																10 = 200 M1/s 6 = 333 MT/s
: 16 bits																5 = 400 MT/s
10 013																37 = 533 MT/s
el																3 = 667 MT/s
rk Level																
SLC																Package Code (dimensions in mm)**
MLC-2																WP = 48-pin TSOP I (CPL version)
MLC-3																WC = 48-pin TSOP I (OCPL version)
																C5 = 52-pad VLGA, 14 x 18 x 1.0 (SDP/DDP/QDP)
ssification																G1 = 272-ball VBGA, 14 x 18 x 1.0 (SDP, DDP, 3DP, QDP)
rk Die nCE	RnB	IO Channels														G2 = 272-ball TBGA, 14 x 18 x 1.3 (QDP, 8DP) G6 = 272-ball LBGA, 14 x 18 x 1.5 (16DP)
1 0	0	10 Channels														H1 = 100-ball VBGA, 12 x 18 x 1.0
1 1	1	1														H2 = 100-ball TBGA, 12 x 18 x 1.0
2 1	1	1														H3 = 100-ball LBGA, 12 x 18 x 1.4 (8DP)
2 2	2	2														H4 = 63-ball VFBGA, 9 x 11 x 1.0
2 2	2	1														HC = 63-ball VFBGA, 10.5 x 13 x 1.0
3 3	3	3														H6 = 152-ball VBGA, 14 x 18 x 1.0 (SDP, DDP)
4 2	2	1														H7 = 152-ball TBGA, 14 x 18 x 1.2 (QDP)
4 2	2	2														H8 = 152-ball LBGA, 14 x 18 x 1.4 (8DP)
4 4	4	4														H9 = 100-ball LBGA, 12 x 18 x 1.6 (16DP)
4 4	4	2														J1 = 132-ball VBGA, 12 x 18 x 1.0 (SDP, DDP)
8 4	2	2														J2 = 132-ball TBGA, 12 x 18 x 1.2 (QDP)
16 8	4	2														J3 = 132-ball LBGA, 12 x 18 x 1.4 (8DP) J4 = 132-ball VBGA, 12 x 18 x 1.0 (5DP, DDP)
8 4	4	2														J5 = 132-ball TBGA, 12 x 18 x 1.0 (SDP, DDP)
16 8	4	4														J6 = 132-ball LBGA, 12 x 16 x 1.2 (QDP) J6 = 132-ball LBGA, 12 x 18 x 1.4 (8DP)
																J7 = 152-ball LBGA, 14 x 18 x 1.5 (16DP)
erating Voltage R																J9 = 132-ball LBGA, 12mm x 18mm x 1.5mm (16DP)
V _{cc} : 3.3V (2.70–3.60V), V _{cc}	g: 3.3V (2.70	⊢3.60V)														**Wafers are available for some products, please contact
1.8V (1.70-1.95V)																Micron for more information.
V _{CC} : 3.3V (2.70–3.60V), V _{CCC}																All NAND packages are Pb-free.
V _{CC} : 3.3V (2.70–3.60V), V _{CCC}			.70–1.95V)													
V _{cc} : 3.3V (2.50–3.60V), V _{ccc}									L							Interface
V _{cc} : 3.3V (2.60–3.60V) , V _{cc}			70 1 0510													Mark Interface
V _{CC} : 3.3V (2.50–3.60V), V _{CCC} V _{CC} : 3.3V (2.50–3.60V), V _{CCC}			(V6E.1-07													A Async only B Sync/Async
V _{CC} : 3.3V (2.50–3.60V), V _{CCQ} : V _{CC} : 3.3V (2.60–3.60V), V _{CCQ}																C Sync only
V _{CC} : 3.3V (2.60–3.60V), V _{CCC}			70-1.95\/\)													D SPI
- (c. 3.3 v (2.00-3.00 v), VCCC	,. J.JV (2.00	5.50V/ OF 1.6V (1.	., J-1.33V)													
																Generation Feature Set
																A = 1st set of device features
																B = 2nd set of device features (rev only if different than
																C = 3rd set of device features (rev only if different)
																D = 4th set of device features (rev only if different)
																etc.

Rev. 1/25/2016

© 2016 Micron Technology, Inc.
Micron and the Micron logo are trademarks of Micron Technology, Inc.
Products and specifications are subject to change without notice. Dates are estimates only.

