BT8x0 PCB RF Design

For Laird Bluetooth -ST-type modules   *v1.0*

INTRODUCTION

The BT8x0 series of modules has the following two product types:

- -SA – Has an integrated chip antenna
- -ST – Exports the RF signal to an external RF connector (i.e., u.FL) via a solder pad on the module

This document mainly describes how to design the RF trace to keep good insertion, return loss, and 50Ω impedance for the RF signal trace from the solder pad of the BT module to u.FL connector for the -ST type.

Note: The -SA type has its own good LC matching circuit to perform 50Ω impedance matching on-board from the RF output port of the main chipset to the chip antenna.

ANTENNA CIRCUIT FOR -ST

We recommend that you place a π - type of matching circuit between the solder pad of RF output port of the BT module and the u.FL for 50Ω impedance matching, as shown in the Figure 1.
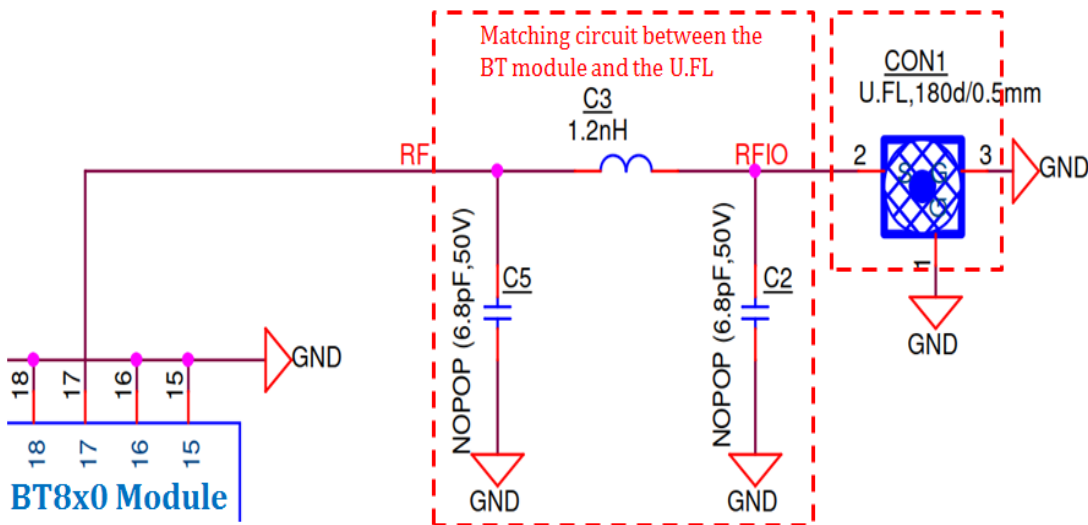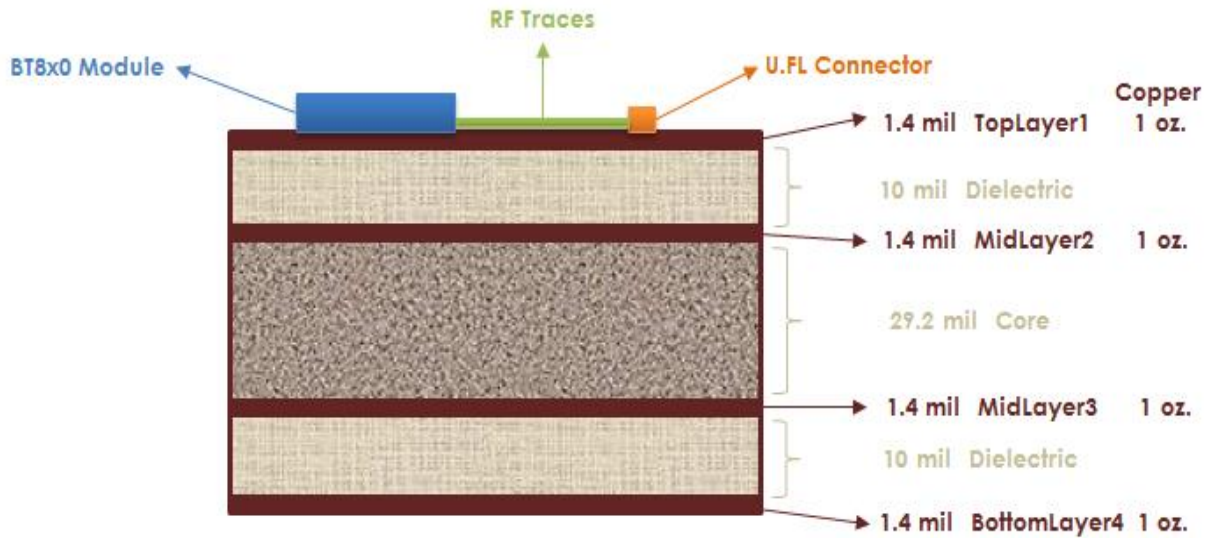

Figure 1: Recommended antenna circuit

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PCB LAYER STACK

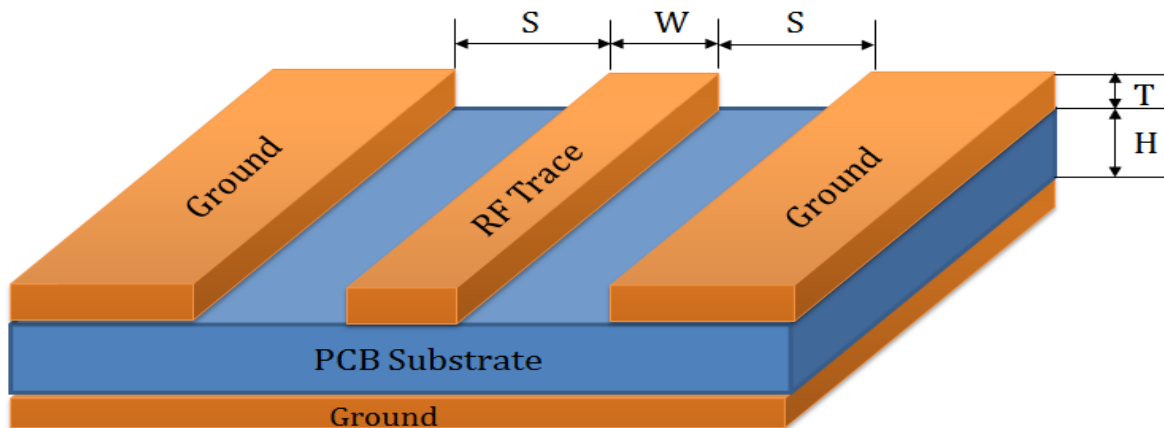We recommend that OEMs use at least a 4-layer stack for platform design, as shown on the Figure 2.

*Figure 2: 4-layer stack*

IMPEDANCE CALCULATION FOR RF TRACE

We recommend the coplanar waveguide structure, as shown in Figure 3.

H: PCB substrate thickness
T: Copper thickness
W: RF Trace width for 50Ω
S: Space between RF trace and Ground Plane

Figure 3: Recommended coplanar waveguide structure

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In accordance to the PCB stack shown in Figure 2, calculate RF trace of impedance with the appropriate trace width and spacing between trace and ground, as shown on the Figure 4.
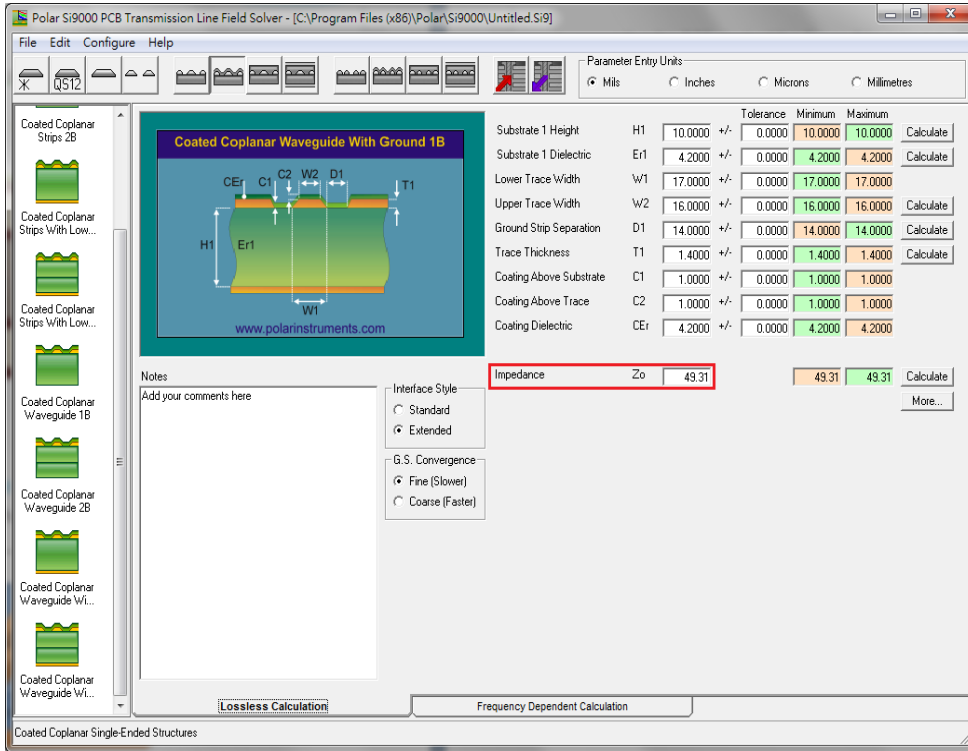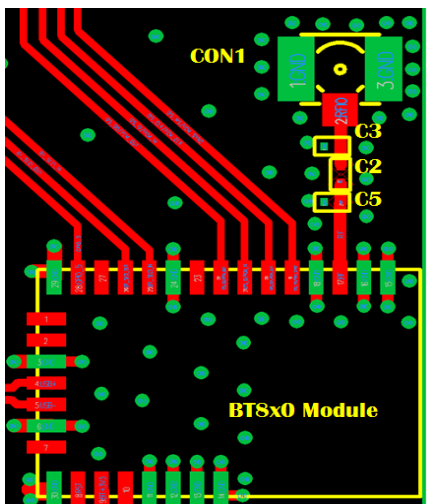

Figure 4: Calculating RF trace of impedance

For calculation and to get a correct impedance, input the trace width (W1) and spacing (D1) to the PCB design rule/layout tool and assign these rules for the RF trace.

PCB PLACEMENT AND LAYOUT

Figure 5 shows the placement of the matching circuit and u.FL connector.

Figure 5: Matching circuit and u.FL connector placement

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Place the matching circuit and u.FL close to the RF feed pad of the BT8x0 module.

To keep the integrated ground plane to the surrounding RF trace and u.FL connector on both top layer and reference layer (MidLayer 2; see Figure 2), place adequate ground vias to the surrounding as well as shown in Figure 6 and Figure 7.
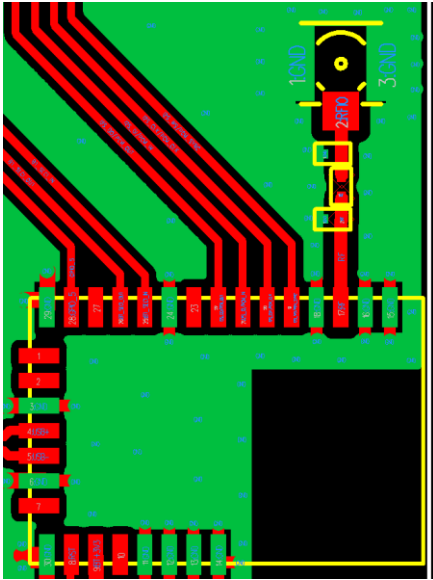
Figure 6: Top layer
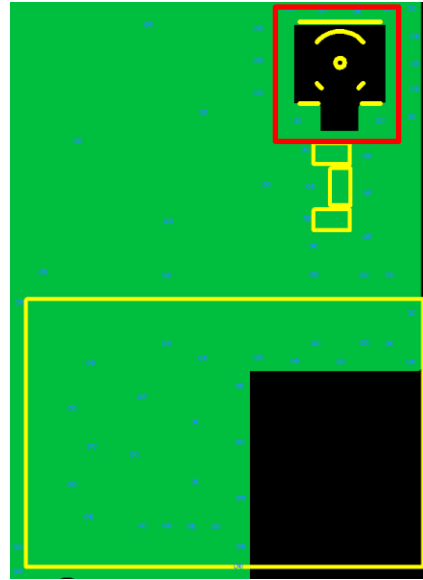
Figure 7: Reference layer

Note: We recommend that you keep no ground copper for all layers of the u.FL connector, as shown in the red box of Figure 7.

REVISION HISTORY

Version	Date	Notes	Contributor(s)	Approver
1.0	12 Jan 2018	Initial Release	Jacky Kuo	Jonathan Kaye

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