

# USB 2.0 High-Speed (480 Mbps) Signal Switch Targeted for Battery Powered Applications

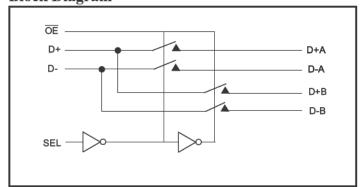
### **Features**

- · USB 2.0 compliant (high speed and full speed)
- $R_{ON}$  is 5.5 $\Omega$  typical @  $V_{CC} = 3.0V$
- · Low bit-to-bit skew
- Low Crosstalk: -40dB @ 500 Mbps
- Off Isolation: −35dB @ 500 Mbps
- Near-Zero propagation delay: 250ps
- · Switching speed: 9ns
- · Channel On Capacitance: 5.5pF
- V<sub>CC</sub> Operating Range: 2.7V to 4.2V ±10%
- Data pin I/O ESD: 12kV HBM protection per JESD22-A114D specification
- · 1,000 MHz Bandwidth
- I/O pins have over-voltage protection and can tolerate a short to Vbus
- · Packaging (Pb-free & Green):
  - 10-contact UQFN (ZM10) (1.4x1.8)
  - 10-contact TQFN (ZL10) (1.3X1.6)

### Application

- · Routes signals for USB 2.0
- · Hand-held devices

### Block Diagram



### **Truth Table**

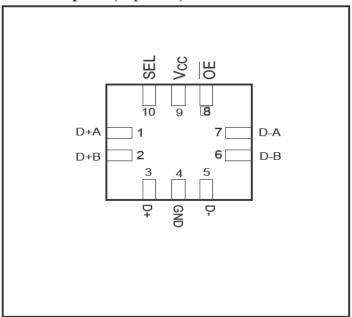
OE SEL Function			
Н	X	I/O's = Hi-Z	
L	L	D(+/-) to D(+/-)A	
L	Н	D(+/-) to D(+/-)B	

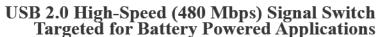
# Description

The PI3USB10LP-A is a single differential channel 2:1 multiplexer/demultiplexer USB 2.0 Switch. Industry leading advantages include a propagation delay of less than 250ps, resulting from its low channel resistance and I/O capacitance. The device multiplexes differential outputs from a USB Host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew, high channel-to-channel noise isolation and is compatible with various standards, such as High Speed USB 2.0 (480 Mb/s).

The PI3USB10LP-A offers overvoltage protection per the USB 2.0 specification. With the chip powered on or off, all I/O pins can withstand a short to Vbus (5V  $\pm$ 10%). This feature can only be offered if a 100-ohm pull up resistor is placed between V<sub>CC</sub> pin to the power supply.

## **Pin Description** (Top View)







### **Maximum Ratings**

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	65°C to +150°C
Supply Voltage to Ground Potential	0.5V to +4.6V
DC Input Voltage	0.5V to V <sub>CC</sub> +0.5V
DC Output Current	120mA
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# DC Electrical Characteristics for USB 2.0 Switching over Operating Range

 $(T_A = -40^{\circ}C \text{ to } +85^{\circ}C, V_{CC} = 3.0 - 4.4V)$ 

Paramenter	Description	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Units
37	Input HIGH Voltage	Guaranteed	$V_{CC} = 4.2V$	1.8			
$V_{ m IH}$	Input HIGH voltage	HIGH level	$V_{CC} = 3.3V$	1.6			v
$ m V_{IL}$	Input LOW Voltage	Guaranteed HIG	H level			0.8	V
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = Max., I_{SE}$	$_{\rm EL} = -18 \text{mA}$		-0.7	-1.2	
$ m I_{IH}$	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>SEL</sub> = VCC				±5	□A
${ m I_{IL}}$	Input LOW Current	V <sub>CC</sub> = Max., V <sub>SEL</sub> = GND				±5	⊔A
R <sub>ON</sub>	Switch On-Resistance <sup>(3)</sup>	$V_{CC}$ = Min., -0.4V $\leq$ V <sub>input</sub> $\leq$ 1.0V, $I_{INPUT}$ = -40mA			5.5	6.5	
R <sub>FLAT(ON)</sub>	On-Resistance Flatness <sup>(3)</sup>	$\begin{split} V_{CC} = Min., -0.4V \leq V_{input} \leq 1.0V, \\ I_{INPUT} = -40mA \end{split}$			1.5		Ω
$\Delta R_{ON}$	On-Resistance match from center ports to any other port <sup>(3)</sup>	V <sub>CC</sub> = Min., -0.4 I <sub>INPUT</sub> = -40mA	$4V \le V_{input} \le 1.0V$ ,		0.9	2.0	

#### Notes:

- 1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- 2.  $V_{CC} = 3.0 4.4V$ ,  $T_A = 25$ °C ambient and maximum loading.
- 3. Measured by the voltage drop between D and  $D_n$  pin at indicated current through the Switch On-Resistance is determined by the lower of the voltages on the two  $(D, D_n)$  pins.

# Power Supply Characteristics ( $V_{CC} = 3.0 - 4.4V$ )

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Тур.	Max.	Units
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = Max., V_{SEL} = GND \text{ or } V_{CC}$			1	μA

### Notes:

1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.



# Capacitance ( $T_A = 25$ °C, f = 1MHz)

Parameters <sup>(3)</sup>	Description	Test Conditions <sup>(1)</sup>	Typ. <sup>(2)</sup>	Max.	Units
$\mathrm{C_{IN}}$	Input Capacitance		3.6		
$C_{OFF}$	Port I Capacitance, Switch OFF	$V_{SEL} = 0V$	3.0		pF
C <sub>ON</sub>	Switch Capacitance, Switch ON		5.5		

# Dynamic Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	Min.	Typ. <sup>(2)</sup>	Max.	Units
$X_{TALK}$	Crosstalk	$R_{L} = 50\Omega, f = 250 \text{ MHz}$		-40		dB
O <sub>IRR</sub>	OFF Isolation	KL - 30\$2, 1 - 230 MINZ		-34		шь
BW	-3dB Bandwidth	$R_{\rm L} = 50\Omega$		1,000		MHz
BW	–0.5dB Bandwidth	$R_{\rm L} = 50\Omega$		270		MHz

#### Notes:

- 1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C ambient and maximum loading.
- 3. This parameter is determined by device characterization but is not production tested.

# **Switching Characteristics**

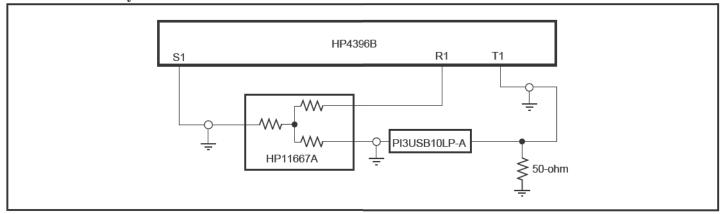
Parameters	Description	Test Conditions (1)	Min.	Тур.	Max.	Units
t <sub>PD</sub>	Propagation Delay <sup>(2,3)</sup>			0.25		
t <sub>PZH</sub> , t <sub>PZL</sub>	Line Enable Time - SEL to D(+/-), D(+/-)n	See Test Circuit for Electrical Charac-	0.5		15.0	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Line Disable Time - SEL to D(+/-), D(+/-)n	teristics	0.5		9.0	
t <sub>SKC-C</sub>	Output skew, channel-to-channel <sup>(2)</sup>	]		3.5	14	
t <sub>SKb-b</sub>	Output skew, bit-to-bit (opposite transition of the same output $(t_{PHL}-t_{PLH})^{(2)}$			7.5	20	ps

### Notes:

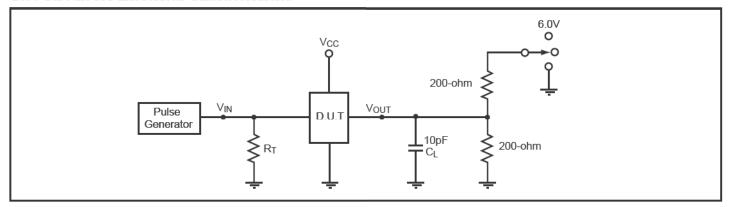
- 1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Guaranteed by design.
- 3. The switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the switch when used in a system is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.



## **Test Circuit for Dynamic Electrical Characteristics**



### **Test Circuit for Electrical Characteristics**



#### Notes:

 $C_L$  = Load capacitance: includes jig and probe capacitance.

R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

All input impulses are supplied by generators having the following characteristics: PRR  $\leq$  MHz,  $Z_0 = 50\Omega$ ,  $t_R \leq 2.5$ ns,  $t_F \leq 2.5$ ns.

The outputs are measured one at a time with on transition per measurement.

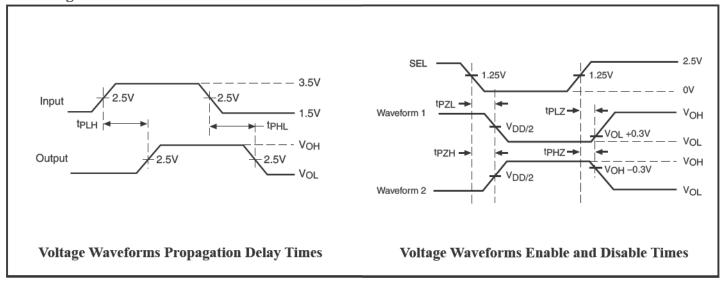
### **Switch Positions**

Test	Switch
t <sub>PLZ</sub> , t <sub>PZL</sub> (output on I-side)	6.0V
t <sub>PHZ</sub> , t <sub>PZH</sub> (output on I-side)	GND
Prop Delay	Open

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## Switching Waveforms



## Applications Information

## **Logic Inputs**

The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a +3.3V supply, the output enables or select pins may be driven low to 0V and high to 3.6V. Driving IN Rail-to-Rail® minimizes power consumption.

### Power Supply Sequencing

Proper power supplysequencing is recommended for all CMOS devices. Always apply VCC and GND before applying signals to input/output or control pins.

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# **Eye Diagram Measurements**

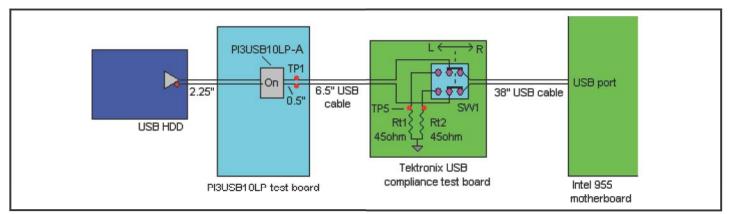


Figure 1: USB2.0 High-speed (480 Mbps) Signal Integrity Test Setup

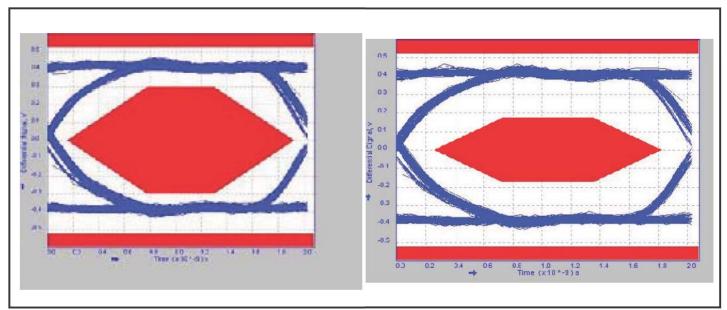
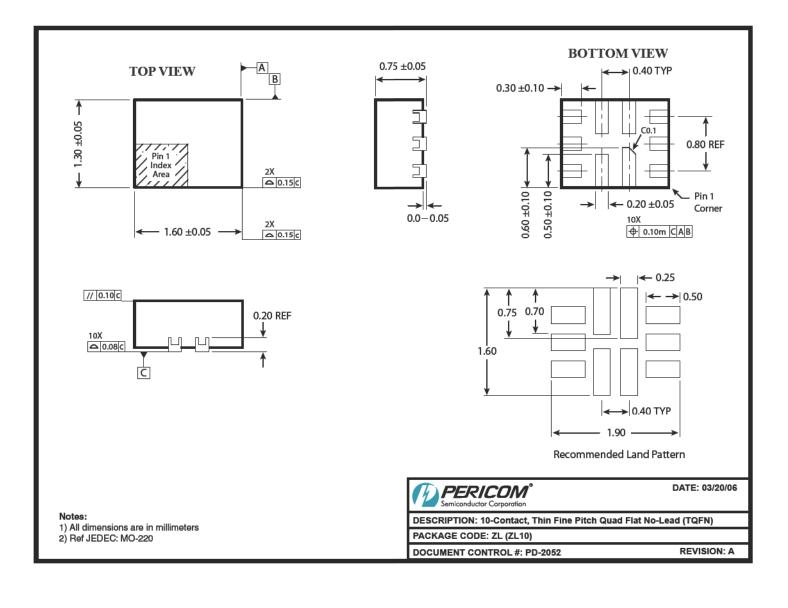


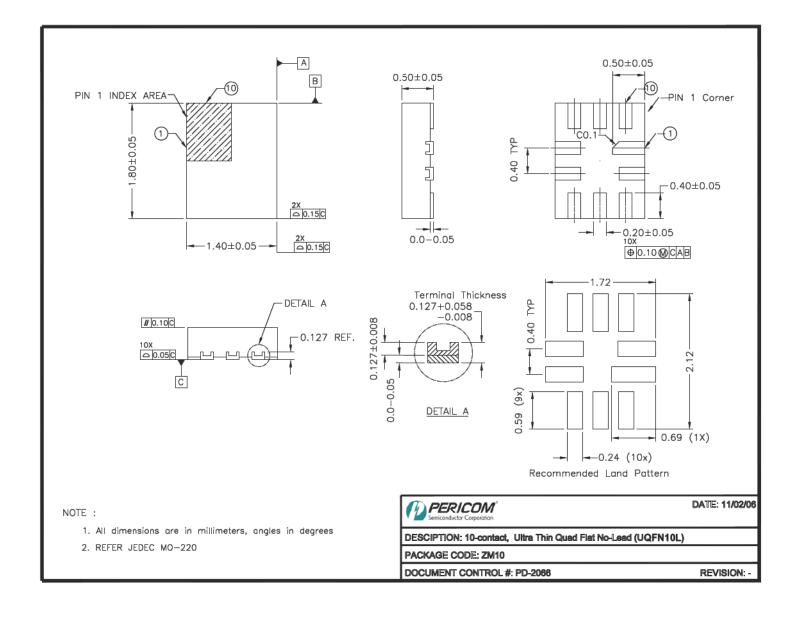
Figure 2: USB 2.0 High Speed (480Mbps) TP1, left eye, and TP5, right eye, with PI3USB10LP-A in the signal path

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## **Ordering Information**

Ordering Code	Package Code	Package Description	Top Mark
PI3USB10LP-AZLE	ZL	Pb-free & Green, 10-contact TQFN	AP
PI3USB10LP-AZME	ZM	Pb-free & Green, 10-contact UQFN	AP

#### Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding X suffix = Tape/Reel

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