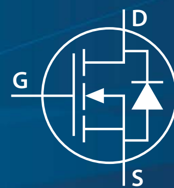
EPC2016C – Enhancement Mode Power Transistor

V_{DS} , 100 V
$R_{DS(on)}$, 16 mΩ
I_D , 18 A



EFFICIENT POWER CONVERSION

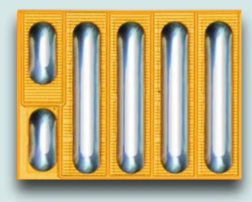
RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	V
I_D	Continuous (T_A = 25°C, $R_{θJA}$ = 13.4°C/W)	18	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	75	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	2	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	4	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	69	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.



EPC2016C eGaN® FETs are supplied only in passivated die form with solder bars.
Die size: 2.1 x 1.6 mm

Applications

- High Speed DC-DC conversion
- Class-D Audio
- High Frequency Hard-Switching and Soft-Switching Circuits

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 300 µA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		25	150	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.5	3	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.15	0.25	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 3 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 11 A		12	16	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.8		V

All measurements were done with substrate connected to source.

Dynamic Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 50 V		360	420	pF
C_{OSS}	Output Capacitance			210	310	
C_{RSS}	Reverse Transfer Capacitance			3.2	4.8	
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, I_D = 11 A		3.4	4.5	nC
Q_{GS}	Gate-to-Source Charge			1.1		
Q_{GD}	Gate-to-Drain Charge			0.55	1	
$Q_{G(TH)}$	Gate Charge at Threshold			0.7		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 50 V		16	24	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

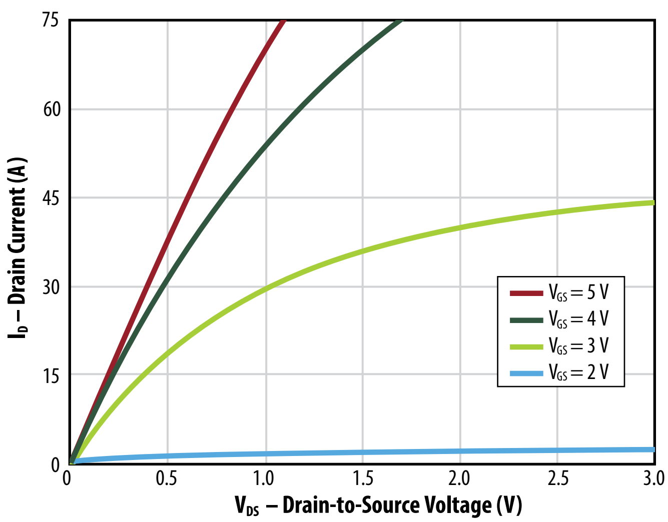


Figure 2: Transfer Characteristics

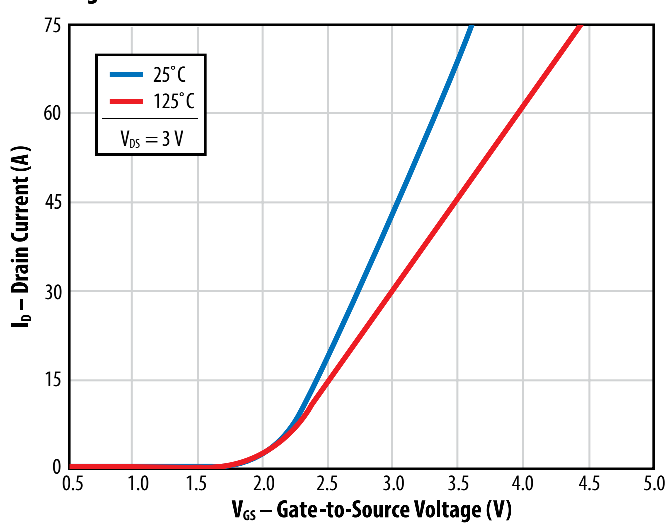


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

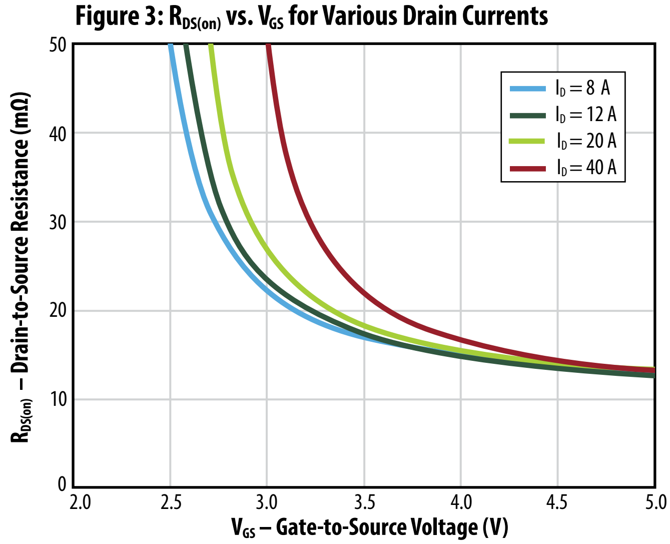


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

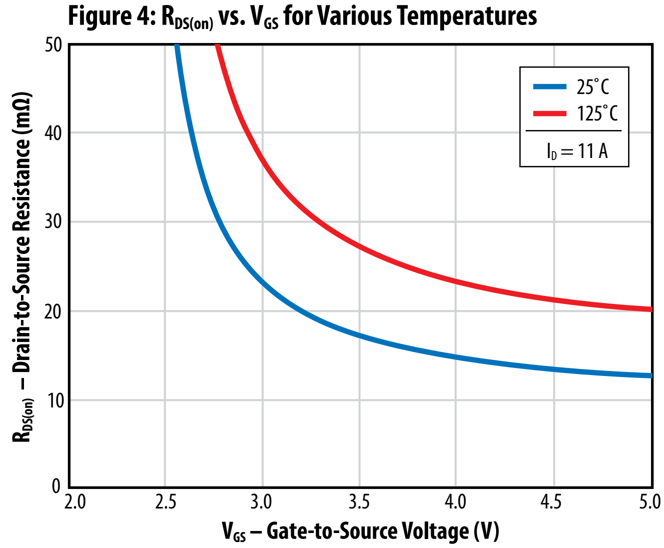


Figure 5a: Capacitance (Linear Scale)

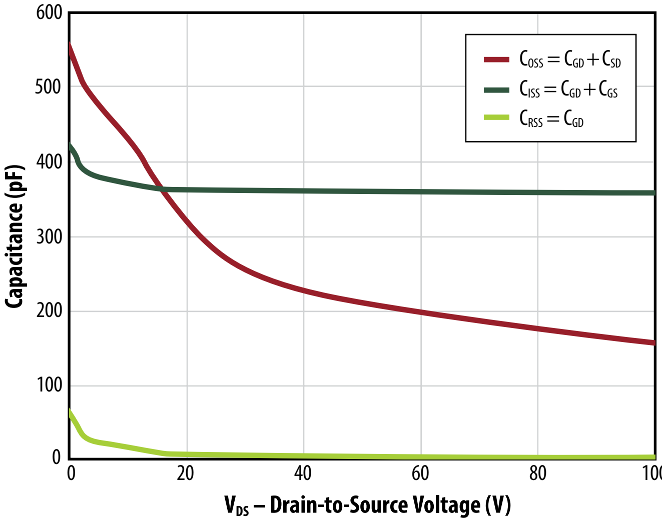


Figure 5b: Capacitance (Log Scale)

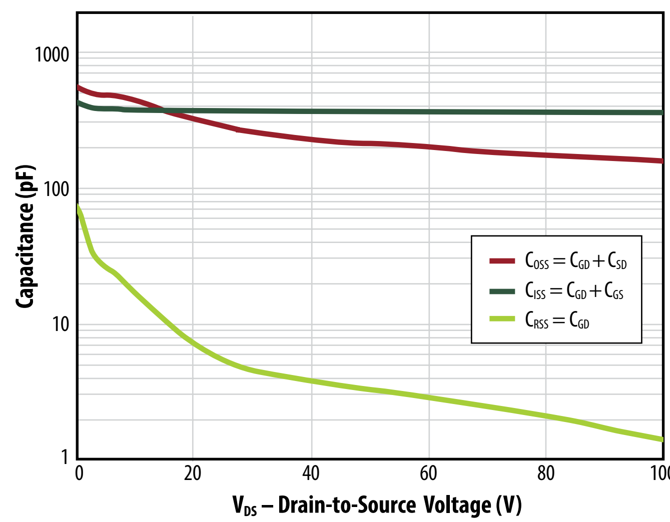


Figure 6: Gate Charge

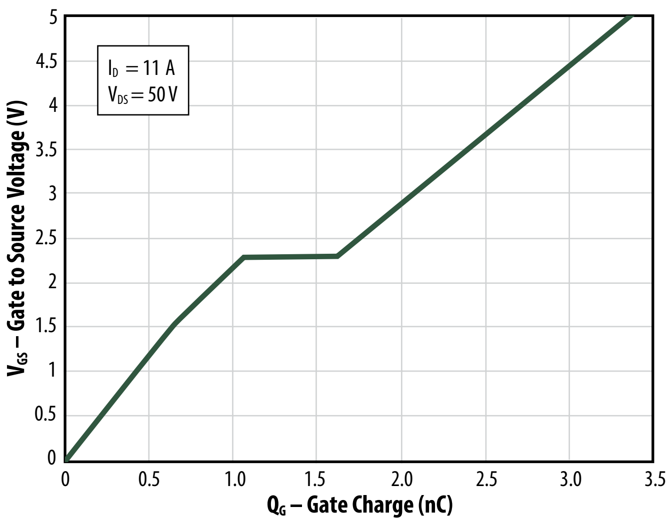


Figure 7: Reverse Drain-Source Characteristics

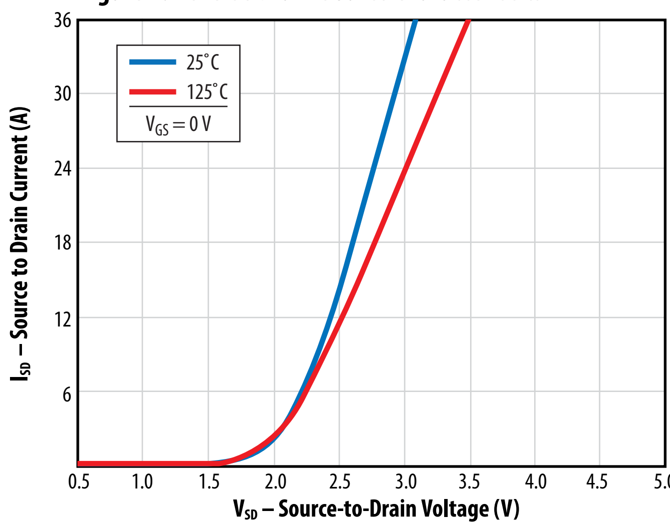


Figure 8: Normalized On-State Resistance vs. Temperature

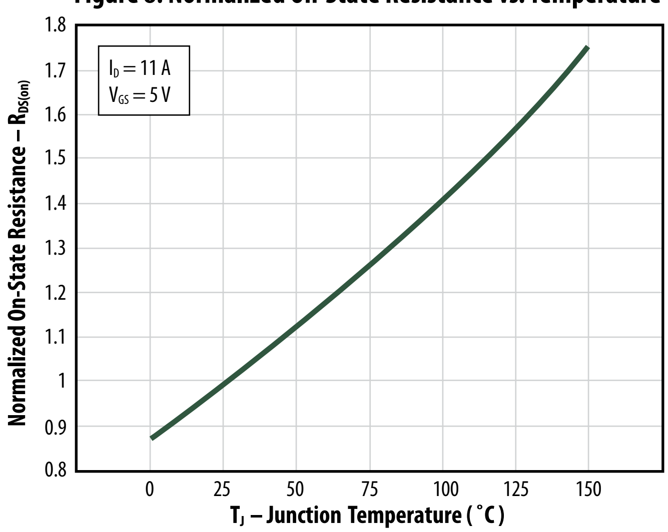
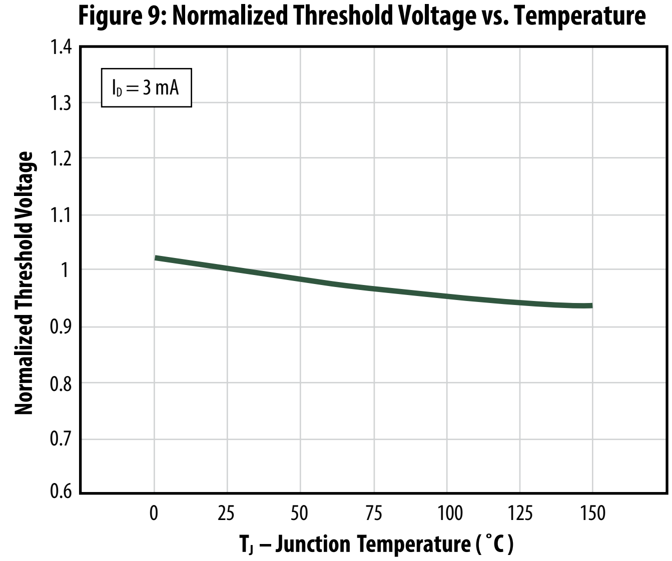


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shortened to source.

Figure 10: Gate Current

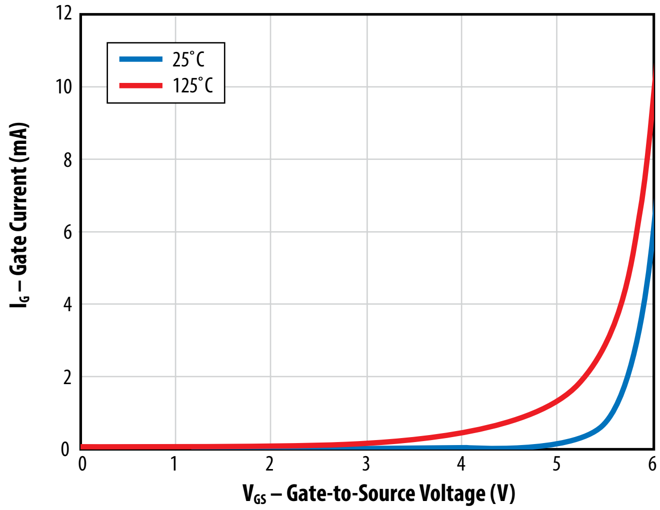
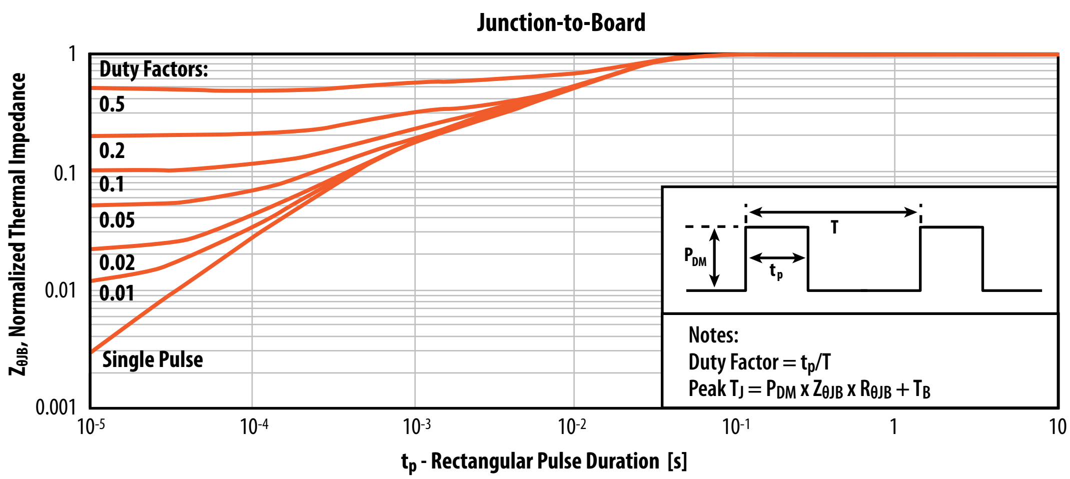


Figure 11: Transient Thermal Response Curves



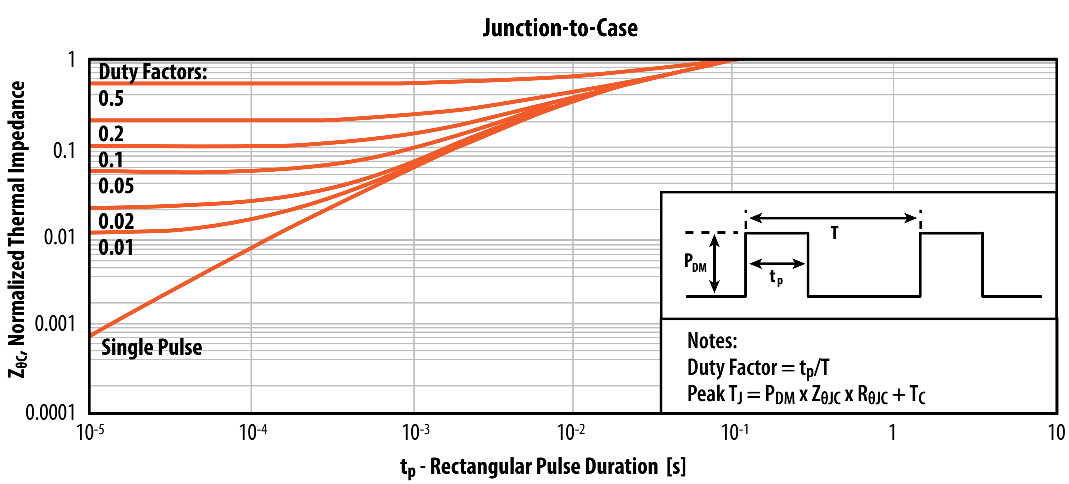
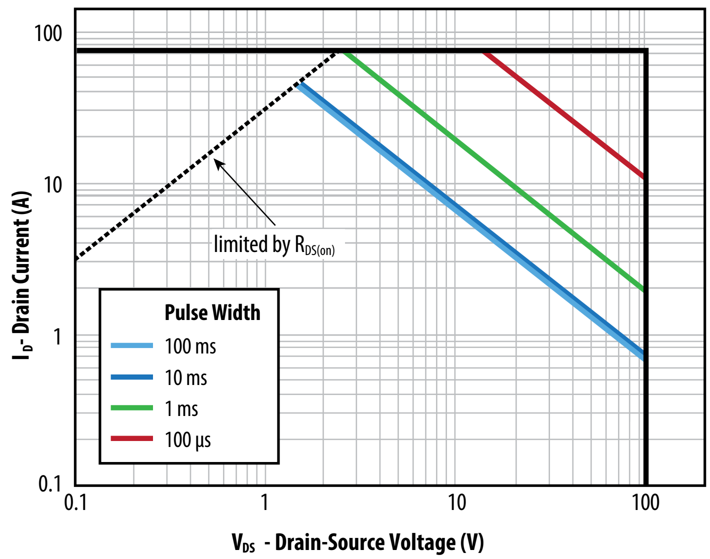


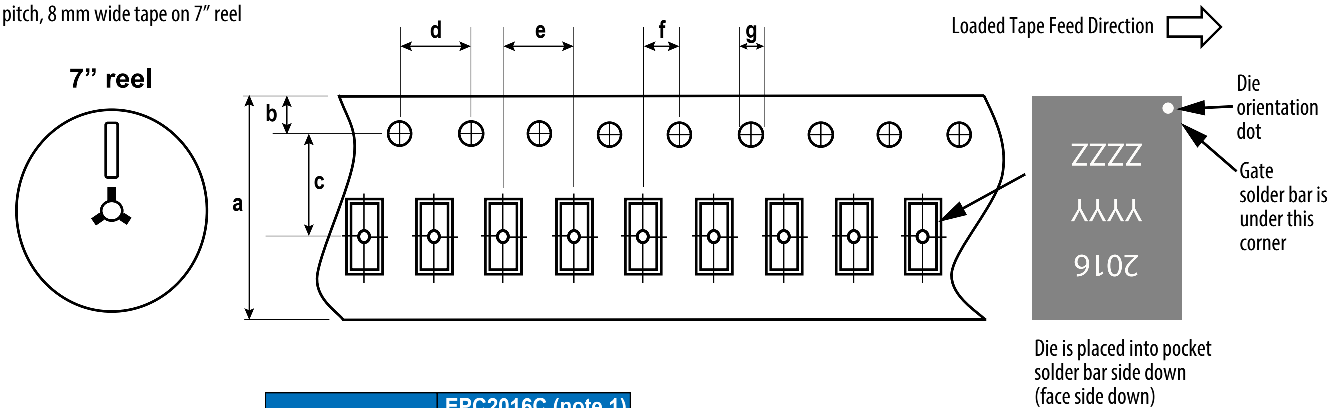
Figure 12: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

TAPE AND REEL CONFIGURATION

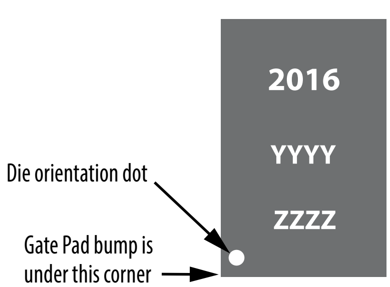
4 mm pitch, 8 mm wide tape on 7" reel



	EPC2016C (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

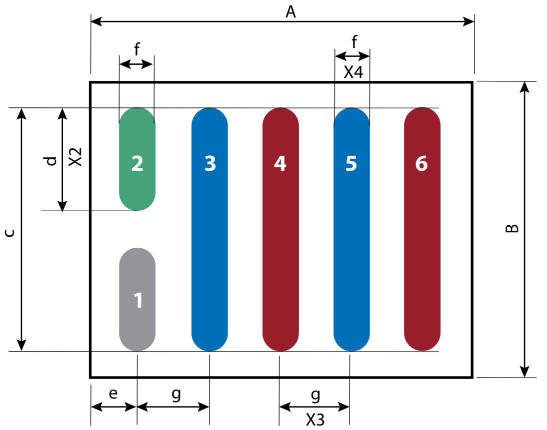
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2016C	2016	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2076	2106	2136
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

Pad no. 1 is Gate;

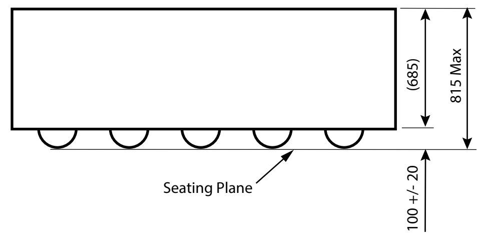
Pads no. 3, 5 are Drain;

Pads no. 4, 6 are Source;

Pad no. 2 is Substrate.*

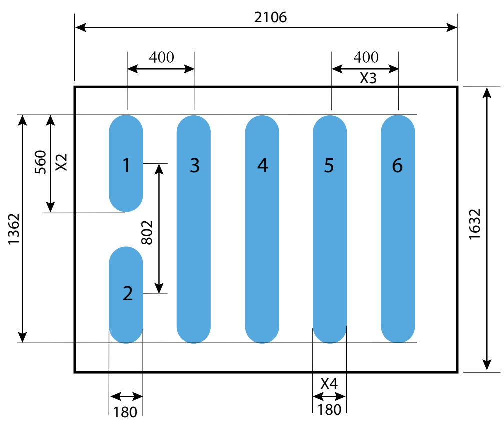
*Substrate pin should be connected to Source

Side View



RECOMMENDED LAND PATTERN

(units in µm)



The land pattern is solder mask defined.

Pad no. 1 is Gate;

Pads no. 3, 5 are Drain;

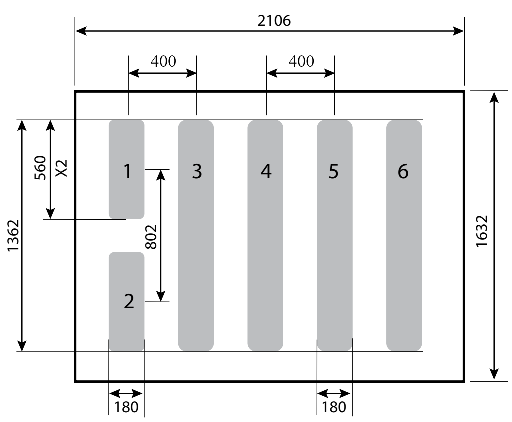
Pads no. 4, 6 are Source;

Pad no. 2 is Substrate. *

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4mil (100 µm) thick, must be laser cut , opening per drawing. The corner has a radius of R60

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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Revised April, 2021