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Home > Products > Clock / Timing Devices > PC-Notebook-Server Clocks > DDR I and DDR II Buffers > Zero Delay Buffers > 9P750 > Add to myIDT [?] You may also like 9P750CGLFT 9P750CGLFT							
Category:	Zero Delay Buffers						
Generic Part:	9P750			Time			
Market Group:	PC CLOCK			mone	ey 👘		
Description:	PC BUFFER Recommended Application: DDR Zero Delay Clock Buffer Product Description/Features: • Low skew, low jitter PLL clock driver • 12 pairs of differential outputs support up to DDR400 • Outputs divided into 3 groups - Group A is reference - Groups B and C have default offsets from Group A, but also have skew programmable in steps relative to Group A - Skew step (unit) set via RSTEP resistor • Static Phase Offset (SPO) of entire device can be programmed - RSPO sets overall SPO (analog delay) - I2C register settings allow fine tuning in steps defined by RSTEP • Spread spectrum tolerant inputs • 2.5 V differential reference clock input Switching Characteristics: • PEAK - PEAK jitter (>100MHz): <75ps • CYCLE - CYCLE jitter (>100MHz):<65ps • OUTPUT - OUTPUT skew: <50ps • DUTY CYCLE: 49% - 51% • Slew rate: 1V/ns - 2V/ns • Input clock duty cycle: 40% - 60%						

Parameters

Package	TSSOP 48 (PAG48)	
Voltage	3.3 V	
Package	TSSOP 48	
Speed	NA	
Temperature	С	
Status	Active	
Sample	No	
Minimum Order Quantity	2000	
Factory Order Increment	2000	

Distributor Inventory

No Pricing information is available from our Distributors at this time.					
Docum	ients				
Туре	Title	Size	Revision Date		
Misc	PC Clocks Contact Info	61 KB	05/29/2007		

Package

Description	TSSOP 6.10 MM	
Class	PLASTIC	
Moisture Sensitivity Level (MSL)	1	
Category	Green	
Moisture Exposure Floor Life	Unlimited @ <30°C/85% RH	
Peak Reflow Temprature	260°C	
Rebake Conditions	N/A	
Length	12.5	
Mark	G	
Width	6.1	
Pitch	0.5	
Thickness	1.0	
Status	Active	