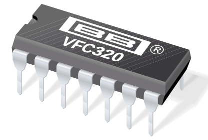


SBVS017A – AUGUST 2001

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY: 12 to 14 bits
  ±0.005% max at 10kHz FS
  ±0.03% max at 100kHz FS
  ±0.1% typ at 1MHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- GAIN DRIFT: 20ppm/°C max
- OUTPUT TTL/CMOS COMPATIBLE

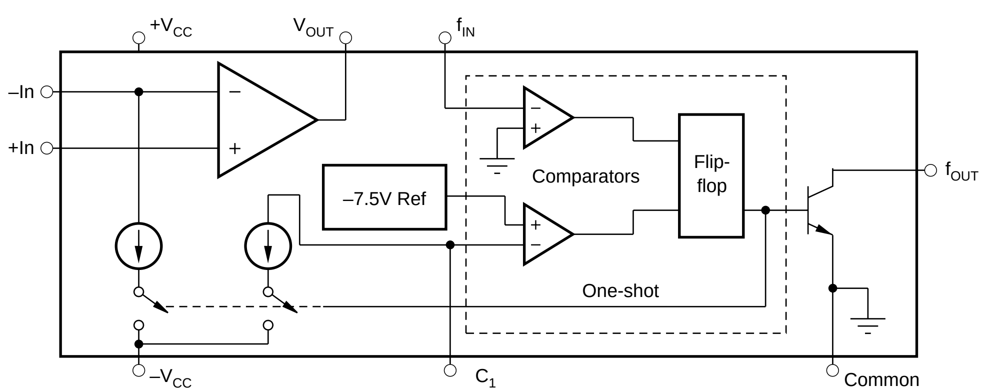
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with –In and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$). The VFC320 is available in two performance grades. The VFC320 is specified for the –25°C to +85°C, range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C and ±15VDC power supply, unless otherwise noted.

		VFC320BP			VFC320CP			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V/F CONVERTER $f_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with e_2 = 0	>0		Note 2				V
	Fig. 4 with e_1 = 0	<0		–10				V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 || 5	650 || 5		*	*		kΩ || pF
Common-Mode Impedance		300 || 3	500 || 3		*	*		kΩ || pF
ACCURACY								
Linearity Error(1) (4) (5)	Fig. 4 with e_2 = 0(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.030		*	*	% FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% FSR
Offset Error Input								
Offset Voltage(3)				±15			*	ppm FSR
Offset Drift(7)			±0.5			*		ppm FSR/°C
Gain Error(3)			±5	±10		*	*	% FSR
Gain Drift(7)	f = 10kHz			50			20	ppm FSR/°C
Full Scale Drift (Offset Drift and Gain Drift)(7)(8)(9)	f = 10kHz			50			20	ppm FSR/°C
Power Supply Sensitivity	$\pm V_{CC}$ = 14VDC to 18VDC			±0.015			*	% FSR%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			Decades
Settling Time	(V/F) to Specified Linearity For a Full Scale Input Step		Note 10			*		
Overload Recovery	<50% Overload		Note 10			*		
OPEN COLLECTOR OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*	µA
Voltage, Logic "1"	External Pull-up Resistor Required (See Figure 4)			V_{PU}			*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		ns
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ f_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 || 10	150 || 10		*	*		kΩ || pF
Logic "1"		+1.0		$+V_{CC}$	*		*	V
Logic "0"		$-V_{CC}$		–0.05	*		*	V
Pulse-width Range		0.25			*			µs
OUTPUT FROM OP AMP								
Voltage	I_O = 6mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-Loop			0.1			*	Ω
Capacitive Load	Without Oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		±13		±20	*		*	V
Quiescent Current			±6.5	±7.5		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades		–25		+85	*		*	°C
S Grade		–55		+125				°C
Operating								
B and C Grades		–40		+85	*		*	°C
S Grade		–55		+125				°C
Storage		–65		+150	*		*	°C

* Specification the same as for VFC320BP.

NOTES: (1) A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity. (2) Determined by R_{IN} and full scale current range constraints. (3) Adjustable to zero. See Offset and Gain Adjustment section. (4) Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. (5) When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy. (6) For e_1 = 0 typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz. (7) Exclusive of external components' drift. (8) FSR = Full Scale Range (corresponds to full scale and full scale input voltage.) (9) Positive drift is defined to be increasing frequency with increasing temperature. (10) One pulse of new frequency plus 50ns typical.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, –Input	$\pm V_{CC}$
Input Voltage, +Input	$\pm V_{CC}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

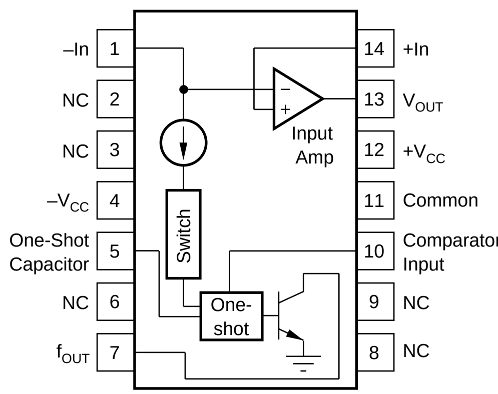
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
VFC320BP	DIP-14	010	N	–40°C to +85°C			
VFC320CP	DIP-14	010	N	–40°C to +85°C			

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "VFC320BP/2K5" will get a single 2500-piece Tape and Reel.

PIN CONFIGURATION

Top View **DIP**



DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero.) Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta_{VIN}$) with operation as close to the chosen full scale frequency as possible

The high linearity of the VFC320 makes the device an excellent choice for use as the front end of Analog-to-Digital (A/D) converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission.)

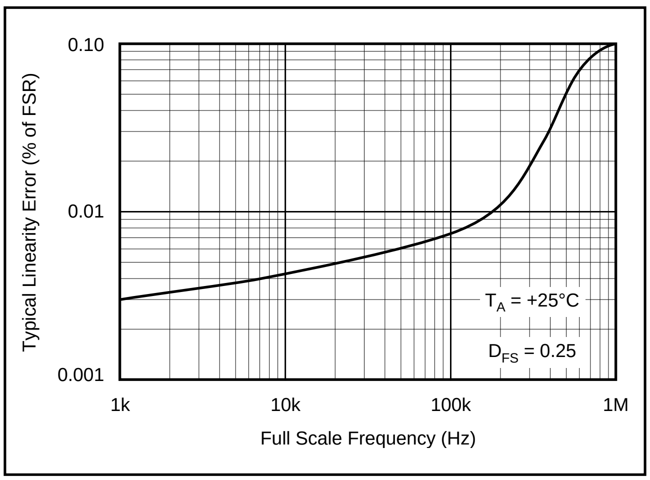


Figure 1. Linearity Error vs Full Scale Frequency.

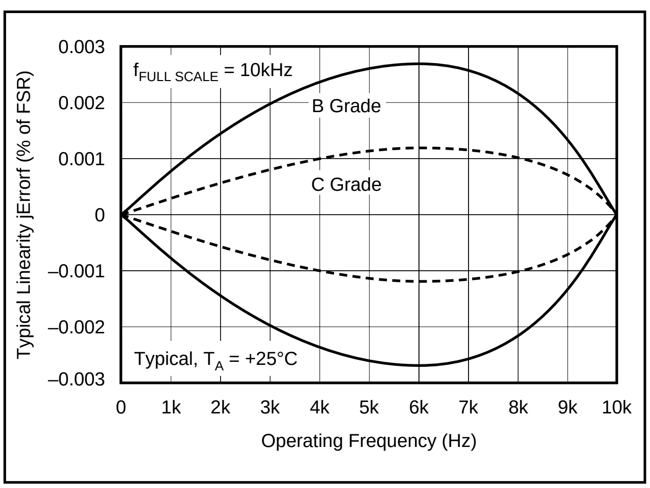


Figure 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC320 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC320.

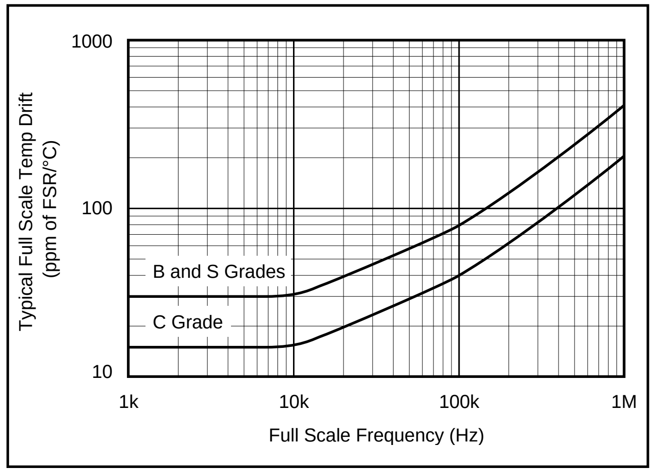


Figure 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC320 to changes in input signal level is specified for a full scale step, and is 50ns plus 1 pulse of the new frequency. For a 10V input signal step with the VFC320 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10µs.

THEORY OF OPERATION

The VFC320 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a on-shot), two switched current sinks, and an open collector output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = –7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this –7.5V threshold point C_1, comparator B resets the flip-flop, and the ramp voltage

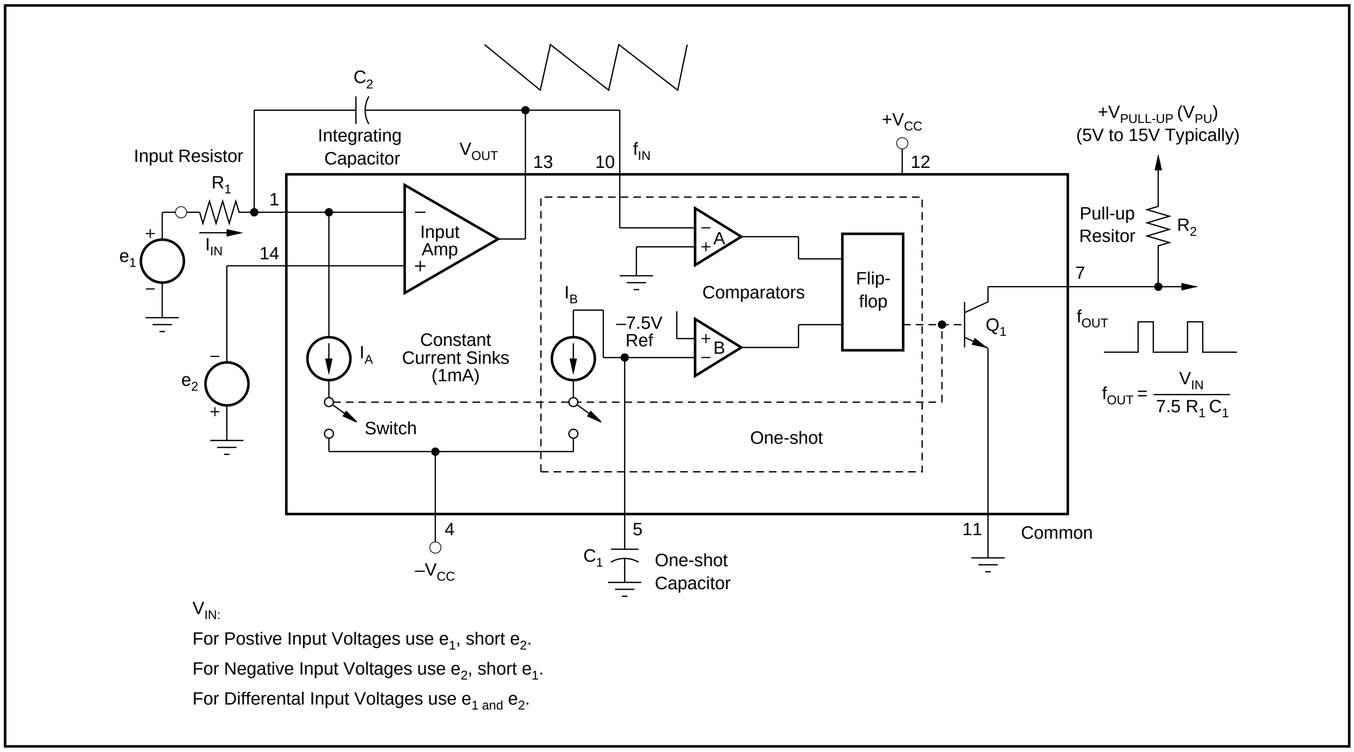


FIGURE 4. Functional Block Diagram of the VFC320.

begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC320 is derived for the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \qquad (1)$$

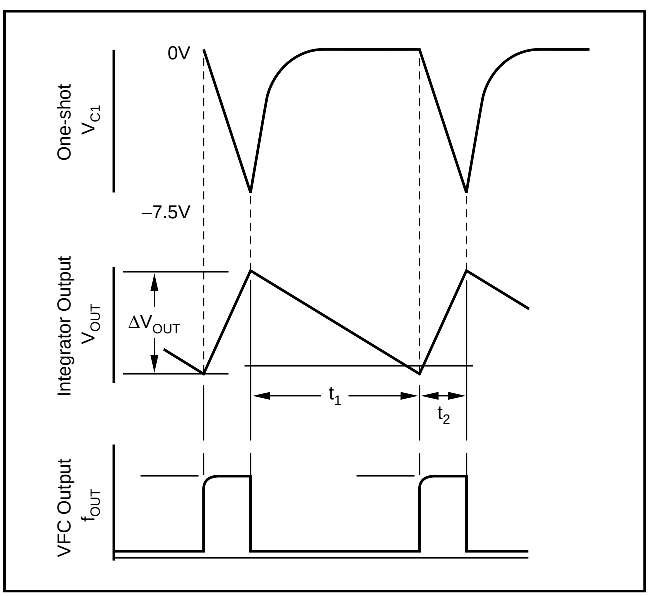


FIGURE 5. Integrator and VFC Output Timing.

In the time $t_1 + t_2$ the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\ t_1 + (I_{IN} - I_A)\ t_2 \qquad (2)$$

$$\text{So that } I_{IN}\ (t_1 + t_2) = I_A\ t_2 \qquad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \qquad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A\ R_2\ R_2} \qquad (6)$$

In the time t_1, I_B charges the one-shot capacitor C_1 until its voltage reaches –7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_{IN}\,7.5}{I_B} \qquad (7)$$

$$\text{Using (7) in (6) yield } f_{OUT} = \frac{V_{IN}}{7.5R_1C_1} \bullet \frac{I_B}{I_A} \qquad (8)$$

Since $I_A = I_B$ the result is

$$f_{OUT} = \frac{V_{IN}}{7.5\ R_1\ C_1} \qquad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC320 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period (t_1 + t_2). For the VFC320, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle, D, is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \bullet f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\,\max / R_1}{1mA} = \frac{I_{IN}\,\max}{1mA}$$

Thus D_{FS} = 0.25 corresponds to I_{IN} max = 0.25mA.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VCF320 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

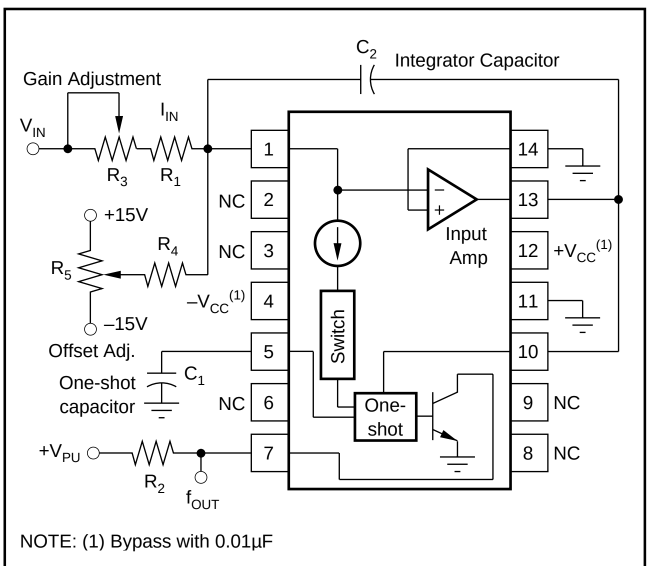


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

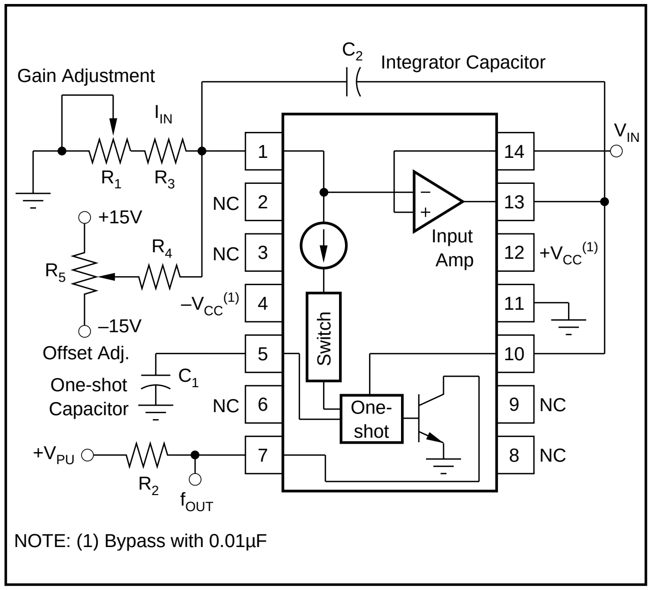


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general, the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale (D_{FS} = 0.25 typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, (5) selecting the integrator capacitor C_2, and (6) selecting the output pull-up resistor, R_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than D_{FS} = 0.25 may be used but linearity will be affected.

The nominal value is R_1 is

$$R_1 = \frac{V_{IN}\max}{0.25mA} \tag{10}$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ NOM} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \tag{11}$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1$ = 0.25mA there is approximately 15pF of residual capacitance so that the design value is

$$C_1(pF) = \frac{33 \bullet 10^6}{f_{FS}} - 15 \tag{12}$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC320 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at D_{FS} = 25%.

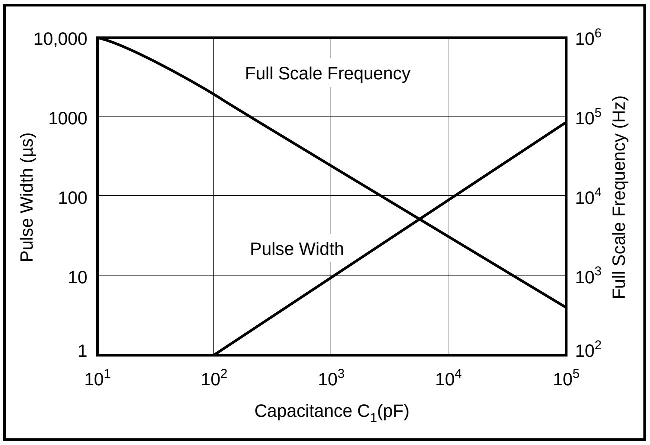


FIGURE 8. Output Pulse Width (D_{FS} = 0.25) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator determine a range of acceptable values,

$$C_2\ (\mu F) = \begin{cases} 100/f_{FS};\ \text{if } f_{FS} \leq 100\text{kHz} \\ 0.001;\ \text{if } 100\text{kHz} < f_{FS} \leq 500\text{kHz} \\ 0.0005;\ \text{if } f_{FS} > 500\text{kHz} \end{cases} \qquad (13)$$

Output Pull Up Resistor R_2

The open collector output can sink up to 8mA and still be TTL-compatible. Select R_2 according to this equation:

$$R_2 \text{ min } (\Omega)\ V_{PULLUP}/(8\text{mA} - I_{LOAD})$$

A 10% carbon film resistor is suitable for use as R_2.

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for initial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1 to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 • full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat stems 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC320 is 0.015% of FSR/% max. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01µF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 (D_{FS} = 0.25)

$$C_1 = [(33 \cdot 10^6)/f_{MAX}] - 15 \qquad [(66 \cdot 10^6)/f_{MAX}] - 15 \text{ if } D_{FS} = 0.5$$

$$= [(33 \cdot 10^6)/100\text{kHz}] - 15$$

$$= 315\text{pF}$$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 (D_{RS} = 0.25)

$$R_1 + R_3 = V_{IN} \text{ max}/0.25\text{mA} \qquad V_{IN} \text{ max}/0.5\text{mA} \text{ if } D_{FS} = 0.5$$

$$= 10\text{V}/0.25\text{mA}$$

$$= 40\text{k}\Omega$$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$$C_2 = 10^2/F_{MAX}$$

$$= 10^2/100\text{kHz}$$

$$= 0.001\mu\text{F}$$

Choose a 0.001µF capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP}/(8mA - I_{LOAD})$

$=5V/(8mA - 1.6mA)$, one TTL-load = 1.6mA

$=781\Omega$

Choose a 750Ω 1/4-watt carbon compensation resistor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC320 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1t (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold.

Errors are nulled using 0.001 • full scale frequency to null offset, and full scale frequency to null the gain error. The procedure is given on this page. Use equations from V/F calculations to find R_1, R_3, R_4, C_1 and C_2.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC320 ideal for a variety of VFC applications. High accuracy allows the VFC320 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits

Figures 10-14 show typical applications of the VFC320.

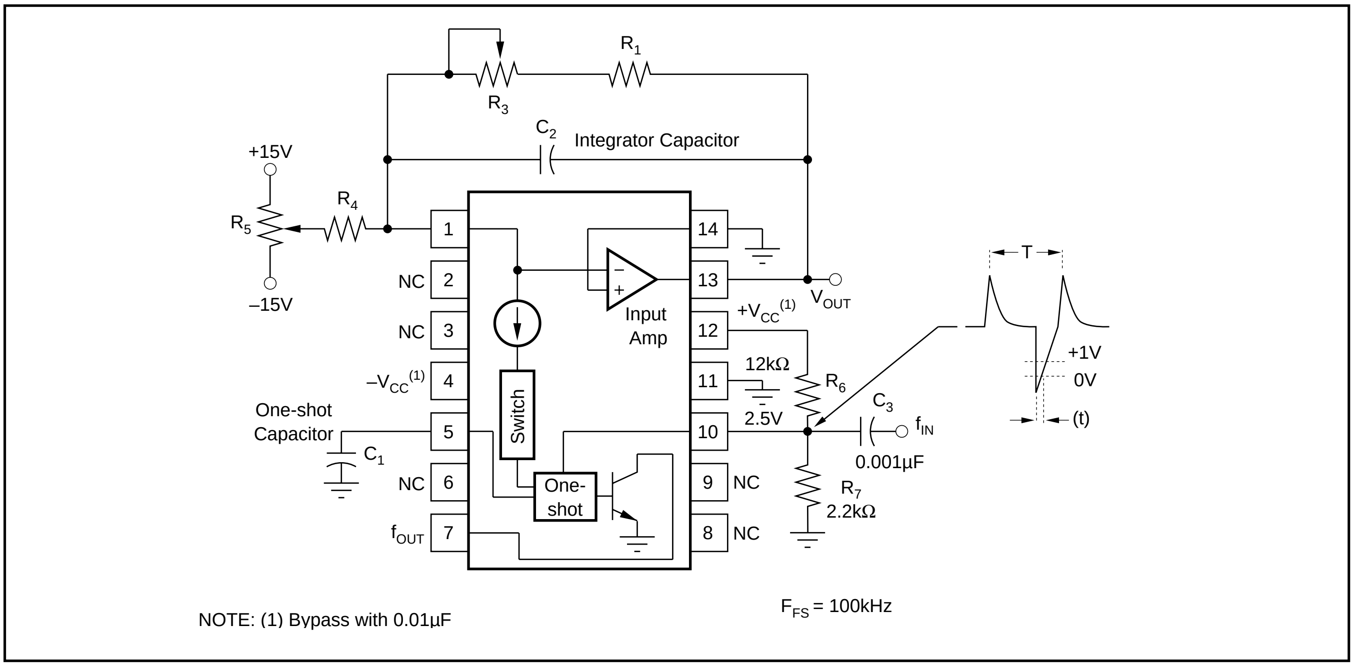


FIGURE 9. Connection Diagram for F/V Conversion.

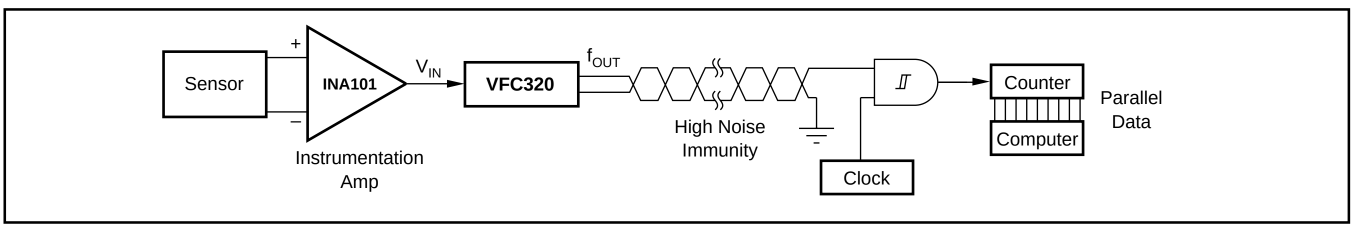


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

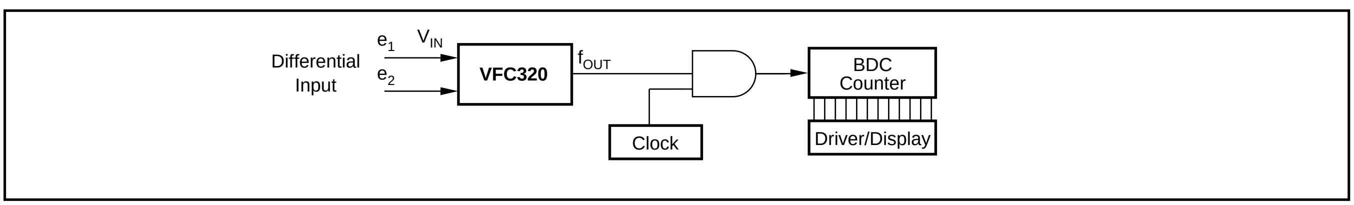


FIGURE 11. Inexpensive Digital Panel Meter.

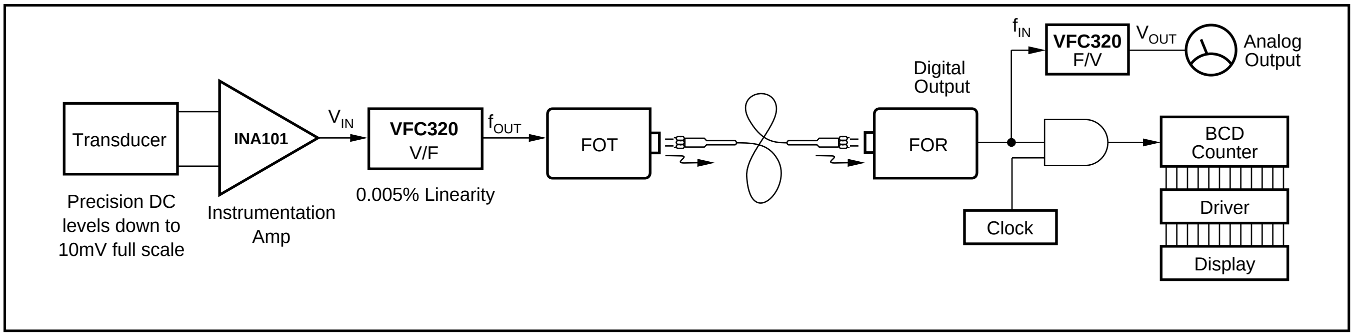


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (Analog and Digital Output).

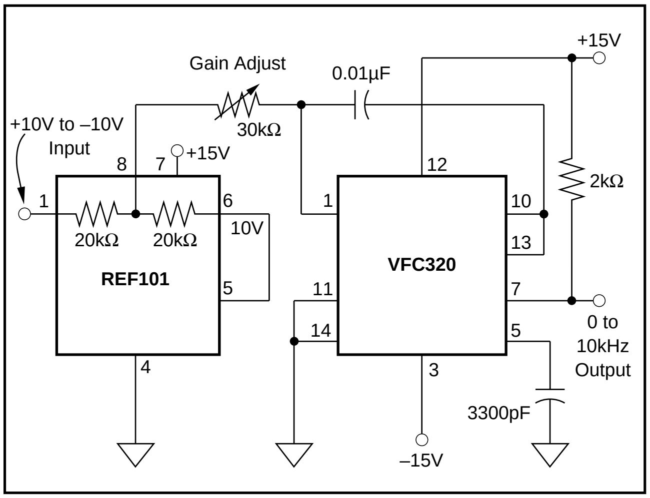


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

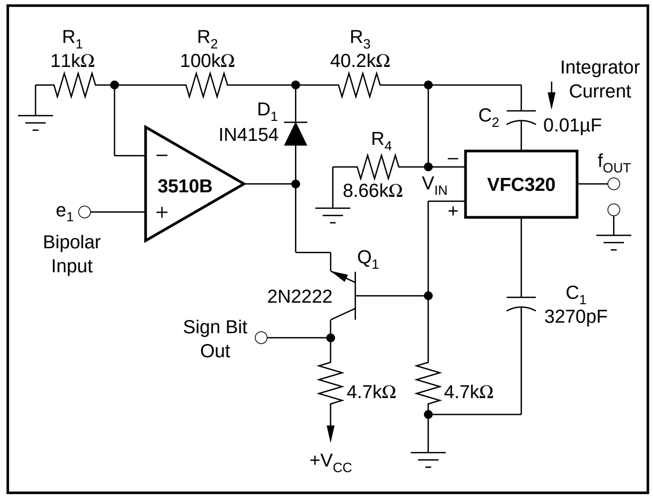


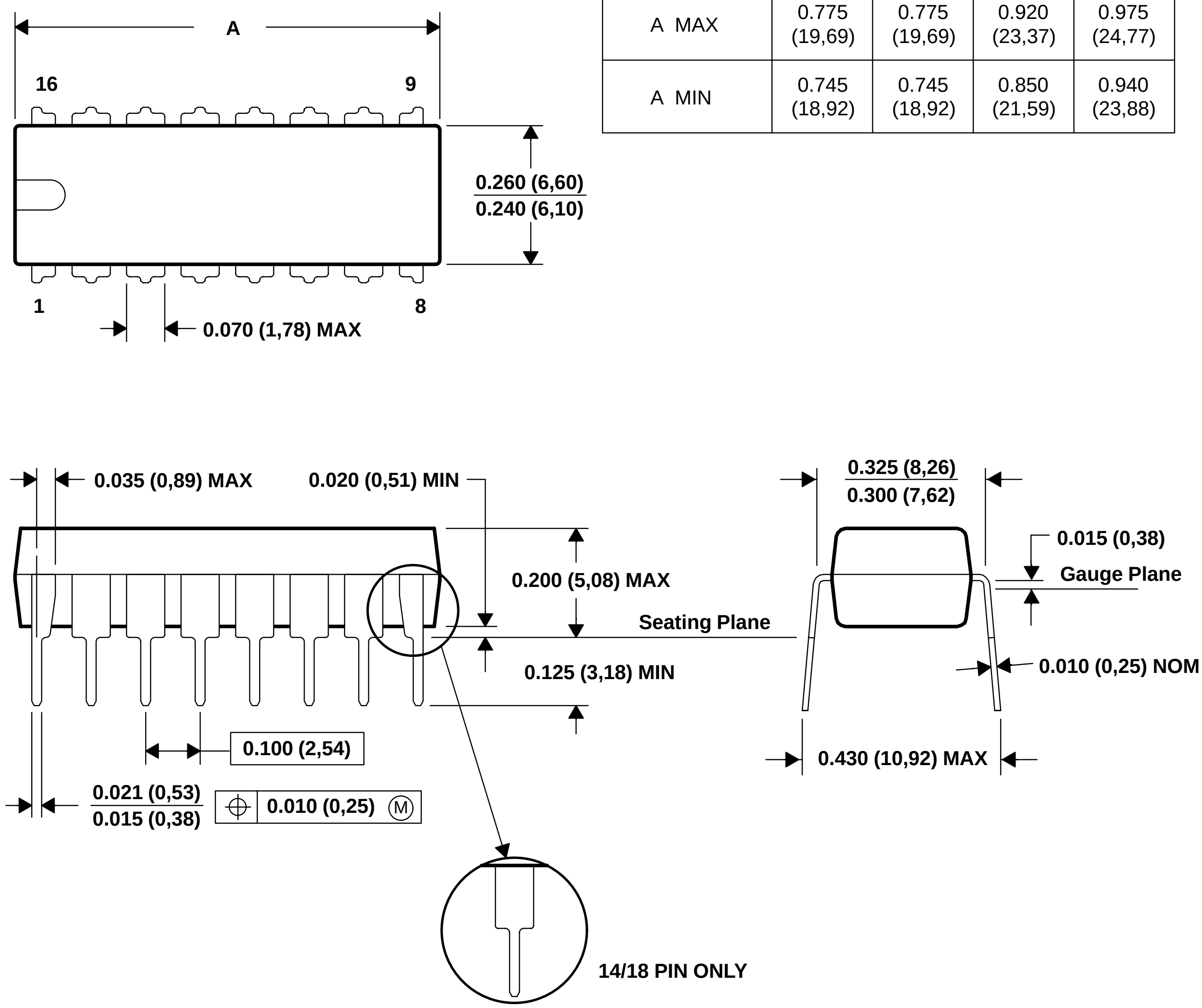
FIGURE 14. Absolute value circuit with the VFC320. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $| e_1 |$. The sign bit output provides indication of the input polarity.

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VFC320BP	ACTIVE	PDIP	N	14	25	RoHS & Green	Call TI	N / A for Pkg Type	-25 to 85	VFC320BP	Samples
VFC320CP	ACTIVE	PDIP	N	14	25	RoHS & Green	Call TI	N / A for Pkg Type	-25 to 85	VFC320CP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

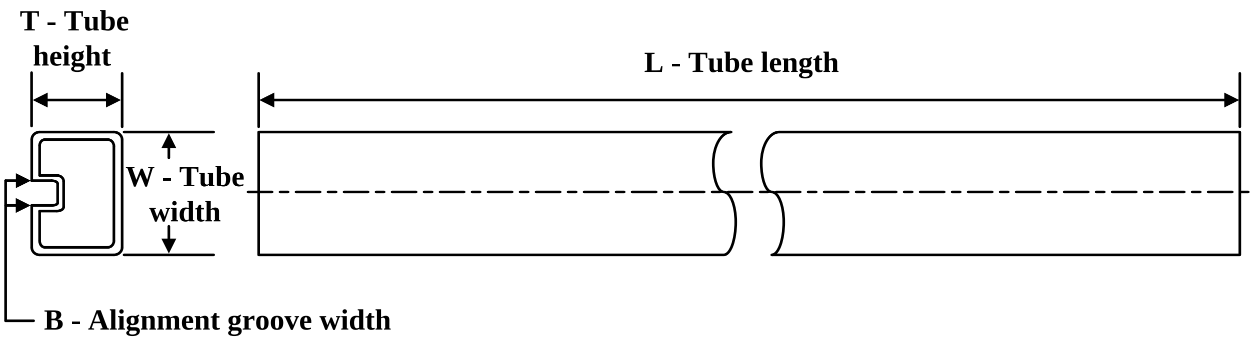
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
VFC320BP	N	PDIP	14	25	506	13.97	11230	4.32
VFC320CP	N	PDIP	14	25	506	13.97	11230	4.32