

# **Phase-Locked Loop Clock Driver**

#### **Product Features**

- High-Performance, Phase-Locked-Loop Clock Distribution
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter ±100ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3 V V<sub>CC</sub>
- Wide range of Clock Frequencies up to 80 MHz
- Package: Plastic 8-pin SOIC (W)

## **Product Description**

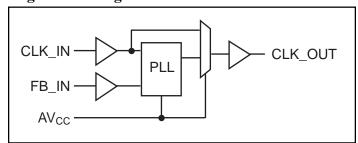
The PI6C2501 features a low-skew, low-jitter, phase-locked loop (PLL) clock driver. By connecting the CLK OUT output to the feedback FB IN input, the propagation delay from the CLK IN input to CLK OUT output will be nearly zero.

## Application

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If a system designer needs more than 16 outputs with the features just described, using two or more zero-delay buffers, such as the PI6C2509Q, or PI6C2510Q, is likely to be impractical. The device-to-device skew introduced can significantly reduce the performance. Pericom recommends using a zero-delay buffer and an eighteen output non-zero-delay buffer. As shown in Figure 1, this combination produces a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, when combined with an eighteen output non-zero delay buffer, a system designer can create a seventeen-output zero-delay buffer.

#### Logic Block Diagram



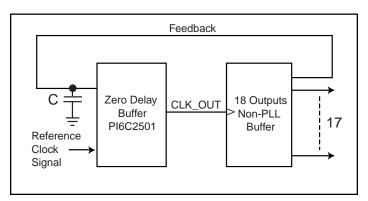
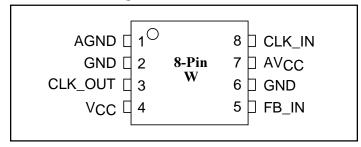


Figure 1. This Combination Provides Zero-Delay Between the Reference Clock Signal and 17 Outputs

### **Product Pin Configuration**





## **Pin Functions**

Pin Name	Pin No.	Type	Description
CLK_IN	8	I	Reference Clock input. CLK_IN allows spread spectrum clock input.
FB_IN	5	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
CLK_OUT	3	О	Clock output. This output provides a low-skew copy of CLK_IN. The output has an embedded series-damping resistor.
AV <sub>CC</sub>	7	Power	Analog power supply. $AV_{CC}$ can be also used to bypass the PLL for test purpose. When $AV_{CC}$ is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V <sub>CC</sub>	4	Power	Power supply.
GND	2, 6	Ground	Ground.

## **DC Specifications** (Absolute maximum ratings over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
$V_{\rm I}$	Input voltage range	0.5	V 105	V
V <sub>O</sub>	Output voltage range	-0.5	V <sub>CC</sub> +0.5	
I <sub>O_DC</sub>	DC output current		100	mA
Power	Maximum power dissipation at $T_A = 55^{o}C$ in still air		1.0	W
T <sub>STG</sub>	Storage temperature	-65	150	°C

#### Note:

Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Parameter	Test Conditions	V <sub>CC</sub>	Min.	Тур.	Max.	Units
$I_{CC}$	$V_I = V_{CC}$ or GND; $I_O = 0^{(1)}$	3.6V			10	μΑ
$C_{\mathrm{I}}$	$V_{I} = V_{CC}$ or GND	3.3V		4		nE
Co	V <sub>O</sub> =V <sub>CC</sub> or GND	3.3 V		6		pF

#### Note:

1. Continuous Output Current

## **Recommended Operating Conditions**

Symbol	Parameter	Min.	Max.	Units
$V_{\rm CC}$	Supply voltage	3.0	3.6	
$ m V_{IH}$	High level input voltage	2.0		V
V <sub>IL</sub>	Low level input voltage		0.8	V
VI	Input voltage	0	V <sub>CC</sub>	
T <sub>A</sub>	Operating free-air temperature	0	70	°C



## Electrical Characteristics (Over Recommended Operating Free-Air Temperature Range

Pull Up/Down Currents of PI6C2501, V<sub>CC</sub> = 3.0V)

Symbol	Parameter	Condition	Min.	Max.	Units	
I	Pull-up current	Vout = 2.4V		-18		
$I_{OH}$	Pull-up current	Vout = 2.0V		-30	A	
$I_{\mathrm{OL}}$	Pull-down current	Vout = 0.8V	25		mA	
	Pull-down current	Vout = 0.55V	17			

### **AC Specifications**

(Timing requirements over recommended ranges of supply voltage and operating free-air temperature)

Symbol	Parameter	Min.	Max.	Units
F <sub>CLK</sub>	Clock frequency PI6C2501	25	80	MHz
$D_{CYI}$	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

### **Switching Characteristics**

(Over recommended ranges of supply voltage and operating free-air temperature, CL = 30pF)

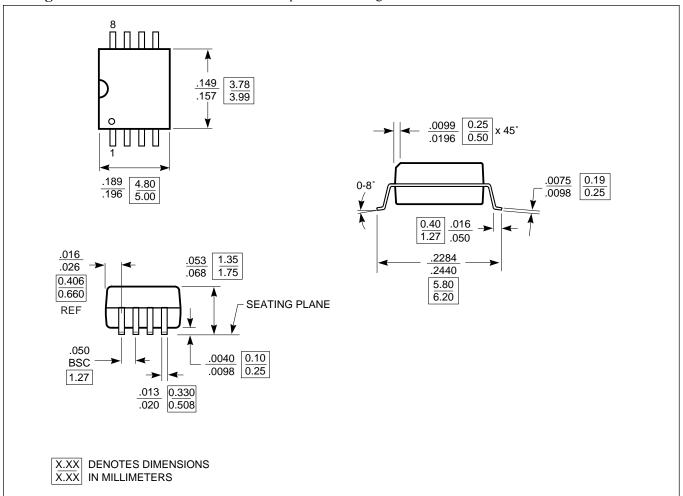
Parameter	From (Input)	To (Output)	$V_{CC} = 3.3V \pm 0.3V, 0-70^{\circ}C$			Units
rarameter			Min.	Тур.	Max.	Units
tphase error without jitter	CLK_IN↑ at 100 & 66 MHz	FB_IN↑	-150		+150	ps
Jitter, cycle-to-cycle	At 100 & 66 MHz		-100		+100	PS
Duty cycle		CLV OUT	45		55	%
tr, rise-time, 0.4V to 2.0V		CLK_OUT		1.0		
tf, fall-time, 2.0V to 0.4V				1.1		ns

#### Note:

These switching parameters are guaranteed by design.



## Package Mechanical Information: Plastic 8-pin SOIC Package.



## **Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
PI6C2501W	W8	8-pin 150-mil SOIC	Commercial