

3-BIT SCANNABLE REGISTER

FEATURES

- Scannable version E112 driver
- Extended 100E VEE range of -4.2V to -5.5V
- 1025ps max. CLK to Output
- Dual differential outputs
- Master Reset
- Internal 75KΩ input pull-down resistors
- Fully compatible with industry standard 10KH, 100K ECL levels
- Fully compatible with Motorola MC10E/100E212
- Available in 28-pin PLCC package

BLOCK DIAGRAM



DESCRIPTION

PIN NAMES

The SY10/100E212 are scannable registered ECL drivers typically used as fan-out memory address drivers for ECL cache driving. In a VLSI array-based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

Pin	Function						
D0 – D2	Data Inputs						
S-IN	Scan Input						
LOAD	LOAD/HOLD Control						
SHIFT	Scan Control						
CLK	Clock						
MR	Master Reset						
S-OUT	Scan Output						
Q[0:2]a, Q[0:2]b	True Outputs						
<u>Q</u> [0:2]a, <u>Q</u> [0:2]b	Inverting Outputs						
Vcco	Vcc to Output						

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E212JC	J28-1	Commercial	SY10E212JC	Sn-Pb
SY10E212JCTR ⁽²⁾	J28-1	Commercial	SY10E212JC	Sn-Pb
SY100E212JC	J28-1	Commercial	SY100E212JC	Sn-Pb
SY100E212JCTR ⁽²⁾	J28-1	Commercial	SY100E212JC	Sn-Pb
SY10E212JZ ⁽³⁾	J28-1	Commercial	SY10E212JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E212JZTR ^(2, 3)	J28-1	Commercial	SY10E212JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E212JZ ⁽³⁾	J28-1	Commercial	SY100E212JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E212JZTR ^(2, 3)	J28-1	Commercial	SY100E212JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^{\circ}C$, DC Electricals only.

2. Tape and Reel.

3. Pb-Free package is recommended for new designs.

TRUTH TABLE

LOAD	SHIFT	MR	Mode
L	L	L	Load
Н	L	L	Hold
Х	Н	L	Shift
Х	Х	Н	Reset

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

		TA = 0°C		TA = +25°C			TA = +85°C					
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
Іін	Input HIGH Current			150			150			150	μA	—
IEE	Power Supply Current 10E 100E		80 80	96 96		80 80	96 96		80 92	96 110	mA	—

AC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

		TA = 0°C		;	TA = +25°C			TA = +85°C				
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
tPD	Propagation Delay to Output CLK MR CLK to S-OUT	575 575 575	800 800 800	1025 1025 1025	575 575 575	800 800 800	1025 1025 1025	575 575 575	800 800 800	1025 1025 1025	ps	_
ts	Set-up Time D SHIFT LOAD S-IN	175 150 225 150	25 50 50 50		175 150 225 150	25 50 50 50		175 150 225 150	25 50 50 50		ps	_
tΗ	Hold Time D SHIFT LOAD S-IN	250 300 225 300	25 100 0 100	 	250 300 225 300	25 100 0 100	 	250 300 225 300	25 100 0 100	 	ps	_
tRR	Reset Recovery	600	350		600	350	—	600	350	_	ps	_
tskew	Within-Device Skew		100			100	_	_	100		ps	1
tskew	Within-Gate Skew		50			50	—	_	50		ps	2
tr tf	Rise/Fall Times 20% to 80%	275	425	650	275	425	650	275	425	650	ps	—

Notes:

1. Within-device skew is defined as identical transitions on similar paths through a device.

2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

28-PIN PLCC (J28-1)



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