

TDA7461

Car radio signal processor

Not For New Design

Features

- High performance signal processor for car radio systems
- Device includes audio processor, stereo decoder, noise blanker and multipath detector
- No external components required
- Fully programmable via I²C bus
- Low distortion
- Low noise

Table 1.

Description

The TDA7461 is a high performance signal processor specifically designed for car radio applications.

Device summary

TDA7461NDTR

E-TDA7461ND⁽¹⁾

E-TDA7461NDTR⁽¹⁾

The device includes a complete audioprocessor and a stereo decoder with noise blanker, stareo blend and all signal processing functions necessary for state-of-the-art as well as future car radio systems.



Switched-capacitors design technique allows to obtain all these relatures without external components or adjustments. This means that higher quality and reliability walks alongside an overall cost saving. The CSP is fully programmable by l^2C bus interface allowing to customize key device parameters and especially filter characteristics.

The BiCMOS process combined with the optimized signal processing assure low noise and low distortion performances.

Packing Tube

Tape and reel

Tube

Tape and reel

Orc'e· code	Package
i DA7461ND	SO-28

1. Device in ECOPACK® package, see Chapter 7: Package information on page 46.

SO-28

SO-28

SO-28

Contents

1	Block	diagrai	n and pin description	6
	1.1	Block di	agram	6
	1.2	Pin desc	cription	6
2	Electr	ical spe	cification	8
	2.1	Absolute	e maximum ratings	8
	2.2	Supply	······	8
	2.3	ESD		8
	2.4	Therma	data	8
	2.5	Audio pi	ocessor part feature	9
		2.5.1	Input multiplexer	9
		2.5.2	Volume control	9
		2.5.3	Bass control	9
		2.5.4	Treble control	9
		2.5.5	Speaker control	
		2.5.6	Mute function	9
	~ ~			~
	2.6	Audio pi	rocessor electrical characteristics 1	0
0	-		GU	
3	Descr	iption a	the audio processor part 1:	3
3	-	iption ວ ີ Program	The audio processor part	3 3
3	Descr	iption a Program 3.1.1	The audio processor part 1 Imable input matrix 1 How to find the right input configuration 1	3 3 4
3	Descr	iption 2 Program 3.1.1 3.1.2	Sthe audio processor part 1 Imable input matrix 1 How to find the right input configuration 1 Input stages 1	3 3 4 4
3	Descr 3.1	iption c Program 3.1.1 3.1.2 3.1.3	Ste audio processor part 1 Immable input matrix 1 How to find the right input configuration 1 Input stages 1 AutoZero 1	3 3 4 4 5
3	Descr 3.1 3.2	iption o Program 3.1.1 3.1.2 3.1.3 Mux out	Ste audio processor part 1 Imable input matrix 1 How to find the right input configuration 1 Input stages 1 AutoZero 1 put 1	3 3 4 5 5
3 005016	Descr 3.1	iption of Program 3.1.1 3.1.2 3.1.3 Mux out Mixing s	Sthe audio processor part 1 Imable input matrix 1 How to find the right input configuration 1 Input stages 1 AutoZero 1 put 1 tage 1	3 3 4 5 5 6
3 005016	Descr 3.1 3.2	iption a Program 3.1.1 3.1.2 3.1.3 Mux out Mixing s 3.3.1	Sthe audio processor part 13 nmable input matrix 1 How to find the right input configuration 1 Input stages 1 AutoZero 1 put 1 tage 1 Loudness 1	3 3 4 5 5 6 6
3 305016	Descr 3.1 3.2	iption a 71 ogram 3.1.1 3.1.2 3.1.3 Mux out Mixing s 3.3.1 3.3.2	Sche audio processor part 1 nmable input matrix 1 How to find the right input configuration 1 Input stages 1 AutoZero 1 put 1 tage 1 Loudness 1 Softmute 1	3 3 4 4 5 6 6 7
3 305016	Descr 3.1 3.2	iption 2 Program 3.1.1 3.1.2 3.1.3 Mux out Mixing s 3.3.1 3.3.2 3.3.3	Sthe audio processor part 13 nmable input matrix 1 How to find the right input configuration 1 Input stages 1 AutoZero 1 put 1 tage 1 Loudness 1 Soft step volume 1	3 3 4 4 5 6 6 7 7
3 3050/f	Descr 3.1 3.2	iption 2 710gram 3.1.1 3.1.2 3.1.3 Mux out Mixing s 3.3.1 3.3.2 3.3.3 3.3.4	Sche audio processor part 13 nmable input matrix 1 How to find the right input configuration 1 Input stages 1 AutoZero 1 put 1 tage 1 Loudness 1 Soft step volume 1 Bass 1	3 3 4 4 5 6 6 7 8
3 305016	Descr 3.1 3.2	iption 2 71 ogram 3.1.1 3.1.2 3.1.3 Mux out Mixing s 3.3.1 3.3.2 3.3.3 3.3.4 3.3.5	Sthe audio processor part 13 nmable input matrix 1 How to find the right input configuration 1 Input stages 1 AutoZero 1 put 1 tage 1 Loudness 1 Soft step volume 1 Bass 1 DC mode 1	3 3 4 4 5 6 6 7 8 8
3 305016	Descr 3.1 3.2	iption 2 710gram 3.1.1 3.1.2 3.1.3 Mux out Mixing s 3.3.1 3.3.2 3.3.3 3.3.4	Sche audio processor part 13 nmable input matrix 1 How to find the right input configuration 1 Input stages 1 AutoZero 1 put 1 tage 1 Loudness 1 Soft step volume 1 Bass 1	3 3 4 4 5 6 6 7 8 8 8

4	Stere	eo deco	der part	20
	4.1	Stereo	decoder feature	20
	4.2	Stereo	decoder electrical characteristics	20
	4.3	Noise	blanker part	23
	4.4	Multipa	ath detector	25
	4.5	Descri	ption of stereo decoder	26
		4.5.1	Stereo decoder mute	
		4.5.2	Input stages	
		4.5.3	Demodulator	
		4.5.4	De-emphasis and high cut	
		4.5.5	PLL and pilot tone detector	27
		4.5.6	Fieldstrength control Level input and gain	
		4.5.7		
		4.5.8	Stereo blend control High cut control	
		4.5.9	High cut control	29
	4.6	FUncti	onal description of the noise blanker	29
		4.6.1	Trigger path	30
		4.6.2	Automatic noise controlled threshold adjustment (ATC)	30
		4.6.3	Automatic threshold control	30
		4.6.4	Over ('aviation detector	31
	4.7	Functio	onal description of the multipath detector	31
	4.8	Test n.	uda	31
		Q^{\prime}		
5	l ² C b	ous inte	rface description	33
	5.1	Interfa	ce protocol	33
S	5.2	Auto ir	crement	33
70-				
6	Data	byte sp	pecification	35
_	. .			10
7	Pack	age info	ormation	
8	Revi	sion his	story	47
-			•	



List of tables

	Table 1.	Device summary	. 1
	Table 2.	Pin description	. 7
	Table 3.	Absolute maximum ratings	. 8
	Table 4.	Supply	. 8
	Table 5.	Thermal data	. 8
	Table 6.	Audio processor electrical characteristics	10
	Table 7.	Input and source programming	14
	Table 8.	Stereo decoder electrical characteristics	20
	Table 9.	Noise blanker electrical characteristics	23
	Table 10.	Multipath detector electrical characteristics	25
	Table 11.	Transmitted data (send mode)	33
	Table 12.	Subaddress (receive mode)	34
	Table 13.	Input selector	35
	Table 14.	Loudness	
	Table 15.	Mute, Beep and Mixing	37
	Table 16.	Volume	38
	Table 17.	Bass and treble attenuation	39
	Table 18.	Bass and treble filter characteristics	40
	Table 19.	Speaker attenuation (LF, LR, RF, RR)	41
	Table 20.	Stereo decoder	42
	Table 21.	Noise blanker	42
	Table 22.	Field strength control	43
	Table 23.	Configuration	43
	Table 24.	Stereo decoder adjustment.	44
	Table 25.	Testing Document revision history	45
	Table 26.	Document revision history	47
C	psole	Testing	



List of figures

Figure 1.	Block diagram	. 6
Figure 2.	Pin connection (top view)	
Figure 3.	Input configuration tree	
Figure 4.	Input stages	
Figure 5.	Loudness attenuation @ fc = 400 Hz (second order)	16
Figure 6.	Loudness center frequency @ Atten. = 15 dB (second order)	16
Figure 7.	Loudness attenuation = 15 dB @ fc = 400 Hz	
Figure 8.	Softmute timing	17
Figure 9.	Soft step timing	18
Figure 10.	Bass control @ fc = 80 Hz, Q = 1	
Figure 11.	Bass center @ Gain = 14 dB, Q = 1	19
Figure 12.	Bass quality factors @ Gain = 14 dB, fc = 80 Hz	19
Figure 13.	Bass normal and DC mode @ Gain = 14 dB, fc = 80 Hz	19
Figure 14.	Treble control @ fc = 17.5 kHz)	
Figure 15.	Treble center frequencies @ Gain = 14 dB	19
Figure 16.	Noise blanker diagram	24
Figure 17.	Trigger threshold vs. VPEAK	24
Figure 18.	Deviation controlled trigger adjustment	24
Figure 19.	Fieldstrength controlled trigger adjustment.	25
Figure 20.	Block diagram of the stereo decoder	26
Figure 21.	Signals during stereo decoder's soft mute	
Figure 22.	Internal stereo blend characteristics	28
Figure 23.	Relation between internal and external LEVEL voltage and setup of Stereo blend	29
Figure 24.	High cut characteristics	29
Figure 25.	Block diagram of the noisebiar kert	30
Figure 26.	Block diagram of the multipath detector	31
Figure 27.	Application exan c'e 1	
Figure 28.	Application example 2	32
Figure 29.	Interface p o'ocol diagram	
Figure 30.	SO-28 mechanical data and package dimensions	46
Figure 30.	40	
16		
5		



1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

	Figure 2. Pin connection (top	view)		
			28 🗖) ACOUTL
26	ACINR	L 2	27 1) ACOUTR
sole	CASSR 🗖	ΙЗ	26 I) CREF
\sim	CASSL	I 4	25) OUTLF
$\mathbf{O}^{\mathbf{r}}$	CDR 🗌	Ι 5	24 I) OUTRF
	CDGND	Γ 6	23 I) OUTLR
	CDL C	Γ7	22 I) OUTRR
	PH GND	Ι 8	21 工) vs
	PHONE	Г 9	20 🗖) GND
	AM 🗖	I 10	19 工) SDA
	MPX C	I 11	18 I) SCL
	LEVEL	I 12	17 工) SMUTE
	MPIN C	I 13	16 I) MUXR
	MPOUT	I 14	15 I) MUXL
		D97AU	U647	

N.	Name	Function	Туре
1	ACINL	Speaker stage input left	I
2	ACINR	Speaker stage input right	I
3	CASSR	Cassette input right	I
4	CASSL	Cassette input left	I
5	CDR	CD right channel input	I
6	CDGND	Ground reference CD	I
7	CDL	CD left channel input	
8	PHGND	Phone ground	I CI
9	PHONE	Phone input	
10	AM	AM input	I
11	MPX	FM input (MPX)	I
12	LEVEL	Level input stereo decoder	I
13	MPIN	Multipath detector input	I
14	MPOUT	Multipath detector output	0
15	MUXL	Multiplexer output left chann ^{al} (stereo decoder output left selectable ⁽¹⁾	0
16	MUXR	Multiplexer output right channel (stereo decoder output right selectable ⁽¹⁾⁾	0
17	SMUTE	Soft mute ur ve	I
18	SCL	I ² C clock line	I/O
19	SDA	2°C data line	I/O
20	GND	Supply ground	S
21	VS	Supply voltage	S
22	OUTRR	Right rear speaker output	0
23	OUTLR	Left rear speaker output	0
24	OUTRF	Right front speaker output	0
25	OUTLF	Left front speaker output	0
26	CREF	Reference capacitor pin	S
27	ACOUTR	Pre-speaker AC output right channel	0
28	ACOUTL	Pre-speaker AC output left channel	0

Table 2.Pin description

1. See data byte specification - speaker attenuator

Pin type:

I = Input O = Output I/O = Input/Output S = Supply



Electrical specification 2

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _S	Operating supply voltage	10.5	V
T _{amb}	Operating ambient temperature range	-40 to 85	°C
T _{stg}	Storage temperature range	-55 to 150	°C

2.2 Supply

Table 4. Supply

.2	Supply		duct(S)			
able 4. Symbol	Supply Parameter	Test condition	Prin.	Тур.	Max.	Unit
V _S	Supply voltage	×0	7.5	9	10	V
I _S	Supply current	V _S = 9V	25	30	35	mA
01/00		Audioprocessor (all (itera fiat)		60		dB
SVRR	Ripple rejection @ 1 kHz	Stereo deccder + Audioprocessor		45		dB

2.3 ESD

All pins are protected against ESD according to the MIL883 standard.

2.4 The mal data 7050

เวเปีย 5.	Thermal data			
Symbol	Parameter		Value	Unit
R _{th j-pins}	Thermal resistance junction to pins	max	85	°C/W



2.5 Audio processor part feature

2.5.1 Input multiplexer

- Fully differential or quasi-differential CD and cassette stereo input
- AM mono or stereo input
- Phone differential or single ended input
- Internal beep with 2 frequencies (selectable)
- Mixable phone and beep signals
- Loudness
- Second order frequency response
- yosolete Product(s) Programmable center frequency and quality factor
- 15 x 1 dB steps
- Selectable flat-mode (constant attenuation)

2.5.2 Volume control

- 1 dB attenuator
- Max. gain 20 dB
- Max. attenuation 79 dB
- Soft-step gain control

2.5.3 **Bass control**

- 2nd order frequency response
- Center frequency programmable in 4 (5) steps
- DC gain programmable
- 7 x 2 dB stap:

2.5.4 Treble control

- 2nd order frequency response
- Center frequency programmable in 4 steps
- 7 x 2 dB steps

2.5.5 Speaker control

4 independent speaker controls (1 dB steps control range 50 dB)

2.5.6 **Mute function**

- Direct mute
- Digitally controlled softmute with 4 programmable time constants



2.6 Audio processor electrical characteristics

Table 6. Audio processor electrical characteristics

 $(V_S = 9 V; T_{amb} = 25 °C; R_L = 10 k\Omega; all gains = 0 dB; f = 1 kHz; unless otherwise specified).$

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
Input selec	tor			•		
R _{in}	Input resistance	all inputs except phone	70	100	130	KΩ
V _{CL}	Clipping level		2.2	2.6		VRMS
S _{IN}	Input separation		80	100		dB
G _{IN MIN}	Min. input gain		-1	0	1,	dB
G _{IN MAX}	Max. input gain		13	14	15 C	ίΒ
G _{STEP}	Step resolution		1	2	3	dB
V	DC Steps	Adjacent gain step	-5	0	+5	mV
V _{DC}	DO Steps	G _{MIN} to G _{MAX}	-5	09	+5	mV
Differentia	I CD stereo input		27			
_		Differential	70	100	130	KΩ
Rin	Input resistance	Common mode	20	30	40	KΩ
CMDD		V _{CM} = 1 V _{RMS} @ (ห่วะ	45	70		dB
CMRR	Common mode rejection ratio	V _{CM} = 1 V _{RMS} ्ग ,0 kHz	45	60		dB
en	Output noise @ speaker output	20 Hz to 20 kHz flat; all stages 0dB		9	15	μV
Differentia	I phone input	51				
		Differential	10	15	20	KΩ
R _{in}	Input resistance	Common mode	20	30	40	KΩ
CMPP		V _{CM} = 1 V _{RMS} @ 1 kHz	45	70		dB
CMRR	Common mode rejection ratio	V _{CM} = 1 V _{RMS} @ 10 kHz	45	60		dB
Beep cont	0]	· · ·				
V _{R.1S}	Beep level		250	350	500	mV
f ^{BWIN}	Lower beep frequency		570	600	630	Hz
f _{BMAX}	Higher beep frequency		1.15	1.2	1.25	KHz
Mixing con	trol			•		
		Source	-1	0	1	dB
		Source	-5	-6	-7	dB
M _{LEVEL}	Mixing level	Source	-10	-12	-14	dB
		Beep/Phone	-1	0	1	dB
Volume co	ntrol			!	.	
G _{MAX}	Max gain		19	20	21	dB
A _{MAX}	Max attenuation		-83	-79	-75	dB



 Table 6.
 Audio processor electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
A _{STEP}	Step resolution		0.5	1	1.5	dB
E	Attenuation set error	G = -20 to 20 dB	-1.25	0	1.25	dB
E _A	Allendalion set enoi	G = -60 to 20 dB	-4	0	3	dB
Ет	Tracking error				2	dB
V.	DC steps	Adjacent attenuation steps	-3	0.1	3	mV
V _{DC}	DC steps	From 0 dB to GMIN	-7	0.5	+7	mV
LOudness	control					
A _{STEP}	Step resolution		0.5	1	1.5	ςB
A _{MAX}	Max. attenuation		-16	-15	-12	dB
f _{CMIN}	Lower center frequency		180	2.76	220	Hz
f _{CMAX}	Higher center frequency		360	400	440	Hz
Soft mute						
A _{MUTE}	Mute attenuation	6	60	100		dB
		T1		0.48	1	ms
_		T2		0.96	2	ms
Τ _D	Delay time	ТЗ	20	40.4	60	ms
		T4	200	324	600	ms
V _{THlow}	Low threshold for SM pin ⁽¹⁾	S			1	V
V _{THhigh}	High threshold for SM pir.		2.5			V
R _{PU}	Internal pull-up resistor		70	100	130	KΩ
V _{PU}	Pull-up voltage			4.7		V
Soft step			1			
T _{SW}	Switch time		5	10	15	ms
Bass conti	ว ไ	I				
CHANGE	Control range		±13	±14	±15	dB
A _{STEP}	Step resolution		1	2	3	dB
		f _{C1}	54	60	66	Hz
		f _{C2}	63	70	77	Hz
f _C	Center frequency	f _{C3}	72	80	88	Hz
		f _{C4}	90	100 ⁽²⁾	110	Hz
		Q ₁	0.9	1	1.1	
0	Quality factor	Q ₂	1.1	1.25	1.4	
Q _{BASS}	Quality factor	Q ₃	1.3	1.5	1.7	
		Q ₄	1.8	2	2.2	



Table 6. Audio processor electrical characteristics (continued)

 $(V_S = 9 V; T_{amb} = 25 °C; R_L = 10 k\Omega; all gains = 0 dB; f = 1 kHz; unless otherwise specified).$

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
DO	Rece DC soin	DC = off	-1	0	+1	dB
DCGAIN	Bass-DC-gain	DC = on	4	4.4	6	dB
Treble cont	trol	· · · · · · · · · · · · · · · · · · ·				
C _{RANGE}	Control range		±13	±14	±15	dB
A _{STEP}	Step resolution		1	2	3	dB
		f _{C1}	8	10	12	KHz
fc	Contor fraguanay	f _{C2}	10	12.5	15	KHz
IC	Center frequency	f _{C3}	12	15	13	KHz
		fC4	14	17.5	21	KHz
Speaker at	tenuator			70		
C _{RANGE}	Control range		53	-50	-47	dB
A _{STEP}	Step resolution		0.5	1	2	dB
A _{MUTE}	Output mute attenuation		80	90		dB
EE	Attenuation set error		-2		2	dB
V _{DC}	DC steps	- 5		0.1	5	mV
Audio outp	outs	00		•		
V _{CLIP}	Clipping level		2.2	2.6		V _{RMS}
RL	Output load resistance	5	2			KΩ
CL	Output load capacitance				10	nF
R _{OUT}	Output Impedance			30	100	W
V _{DC}	DC voltage lavel		3.6	3.8	4.0	V
General						
	<u>K</u> O	BW = 20 Hz to 20 kHz		3	15	μV
e _{NO}	Output noise	output muted		-		
SS		all gain = 0 dB BW = 20 Hz to 20 kHz		6.5	15	μV
S/N	Signal to noise ratio	all gain = 0 dB flat; V_0 = 2 V_{RMS}		106		dB
3/IN	Signal to hoise failo	bass treble at 12 dB; $V_0 = 2.6V_{RMS}$		100		dB
d	Distortion	V_{IN} = 1 V_{RMS} ; all stages 0 dB		0.002	0.1	%
u		V_{IN} = 1 V_{RMS} ; bass & treble = 12 dB		0.05	0.1	%
S _C	Channel separation left/right		80	100		dB
 F_	Total tracking error	A _V = 0 to -20 dB	-1	0	1	dB
E _T		A _V = -20 to -60 dB	-2	0	2	dB

1. The SM pin is active low (Mute = 0)

2. See description of audioprocessor part - bass & treble filter characteristics programming

3 Description of the audio processor part

3.1 **Programmable input matrix**

The programmable input matrix of the TDA7461 offers several possibilities to adapt the audioprocessor to the desired application. In to the standard application we have:

- CD quasi differential
- Cassette stereo
- Phone differential
- AM mono
- Stereo decoder input.

The input matrix can be configured by only 2 bits: bits 3 and 4 of subaddress 0. Be sically the bit of subaddress 13 is fixed by the application and has to be programmed only once at the startup of the IC.

For many configurations the two bits are also fixed during one april at on (e.g. the standard application) and a change of the input source can be done by leading the first three bits of subaddress 0.

In other configurations for some sources a program μ g of bit 3 and 4 of subaddress 0 is necessary in addition to the three source selection bits. In every case only the subaddress 0 has to be changed to switch from one source to another.

The following picture shows the input and source programming flow:



Figure 3. Input configuration tree

1. In AMSTD configuration the AM mono signal is lead through the FM stereo decoder part to use its additional filters.



		Pin ni	umber		Decemen	
Appl. N#	6	8	9	10	Progran	nming ⁽¹⁾
1	CD _{GND}	Phone _{GND}	Phone	AM _{MONO}	Startup	0/xxx11xxx
					Startup	0/xxxx1xxx
0	00	Dhama			FM	0/xxx11100
2	CD _{GND}	Phone _{GND}	AMRIGHT AM _{LEFT}		AM	0/xxx01011
					Phone	0/xxx11010
					Startup	0/xxxx1xxx
0	00	Dhama	Dhama		FM	いんやご1100
3	CD _{GND}	Phone _{GND}	Phone	AMSTD	AM	ર∕x⊼x01100
					Phone	0/xxx11010
4	CDR _{GND}	CDL _{GND}	Phone	AMMON'S	Startup	0/xxxx0xxx
				X	Startup	0/xxxx0xxx
5	CDR _{GND}	CDL _{GND}	AMRIGHT	A. LEFT	FM	0/xxx10100
				0	AM	0/xxx00011
			5		Startup	0/xxxx0xxx
C			Dhama	A.N.4	FM	0/xxx10100
6	CDR _{GND}	CDL _{GND}	Phone	AM _{STD}	AM	0/xxx00100
		51			Phone	0/xxx10010

 Table 7.
 Input and source programming

1. Syntax 0/xxx11100 me ins: SUBADDRESS = 0 - DATA BYTE = xxx11100 (x - don't care).

3.1.1 How to find the right input configuration

The best way to come to the desired configuration may be to go through the application tree from the top to the bottom while making the specific decisions.

This way will lead to one of the six possible applications. Then take the number of the application and go into the pinning table. Here you will find the special pinout as well as the special programming codes for selecting sources.

For example in Appl. 6 the TDA7461 has to be configured while startup with the data byte 0/xxxx0xxx.

To select the FM, AM or phone source the last five significant bits of subaddress 0 have to be changed, for any other source the last three bits are sufficient (see data byte specification).

3.1.2 Input stages

Most of the input circuits are the same as in previous ST audio processors with exception of the CD inputs (see *Figure 4*). In the meantime there are some CD players in the market having a significant high source impedance which affects strongly the common mode rejection of the normal differential input stage. The additional buffer of the CD input avoids this drawback and offers the full common mode rejection even with those CD players.



The TDA7461 can be configured with an additional input; if the AC coupling before the speaker stage is not used (bit 7 in subaddress 5 set to "1") ACINL and ACINR pins can be used as an additional stereo input.





3.1.3 AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain stage would be transferred or even amplified to the output. To avoid that effect a special offset cancellation stage called AutoZero is implemented.

To avoid audible clicks the audioprocessor is muted before the loudness stage during this time. In some cases, for example if the μ P is executing a refresh cycle of the I²C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the TDA7461 could be switched in the "Auto Zero Remain" mode (Bit 6 of the subaddress byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment value remains.

3.2 Mux output

The MUX_L and MUX_R outputs can provide selectively the output of the input multiplexer (Speaker RF register, Byte 8, bit 6=1) or the output of the stereo decoder (Speaker RF register Byte 8 bit 6=0).

If bit D3 byte 10 (Stdec Register) is set to 1, then the stdec signal is automatically muted, when another source is selected at the input multiplexer.



If bit D3 byte 10 (Stdec Register) is set to 0, then the stdec signal will be always available at the Mux out pins, no matter which is the selected source.

The selection of the stereodecoder input, via a special procedure, is recommended.

- 1. Soft Mute or Mute the signal path
- 2. Temporary deselect the stereodec
- 3. Wait 100-200 ms to allow the stdec internal filters to settle
- 4. Select sterodec input (with automatic autozero)

This procedure guarantees an optimum offsetcancellation, avoiding big DC offsets due to the autozero circuitry, which otherwise could try to compensate the signal sourced at the MPX input instead of the stereodecoder intrinsic offset.

3.3 Mixing stage

This stage offers the possibility to mix the internal beep or the phone signal to any other source.

Due to the fact that the mixing stage is also located behind the In-Gain stage fine adjustments of the main source level can be done in this way.

3.3.1 Loudness

There are four parameters programmable in the loudness stage (see Figure 5, 6 and 7):

- Attenuation
- Center frequency
- Loudness Q
- Flat Mode: in this mode ine loudness stage works as a 0 15dB attenuator.

Figure 5.Loudness attenuation @ fc = 400 Hz Figure 6.
(second order)Loudness center frequency @
Atten. = 15 dB (second order)





Figure 7. Loudness attenuation = 15 dB @ fc = 400 Hz

3.3.2 Softmute

The digitally controlled softmute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can either be activated by the softmute pin or by the I^2C bus. The slope is realized in a special S shaped curve to mute slow in the critical regions (see *Figure 8*). For timing purposes the Bit 3 of the I^2C bus output register is set to 1 from the start of muting until the end of demuting.



1. Please notice that a started Mute action is always terminated and could not be interrupted by a change of the mute signal.

3.3.3 Soft step volume

When volume level is changed often an audible click appears at the output. The root cause of those clicks could be either a DC offset before the volume stage or the sudden change of the envelope of the audio signal. With the Soft step feature both kinds of clicks could be reduced to a minimum and are no more audible (see *Figure 9*).



Figure 9. Soft step timing



1. For steps more than 1dB the soft step mode should be deactivated because it could generate a 1dB error during the blend-time.

3.3.4 Bass

There are three parameters programmable in the bass stage (see Figure 10, 11, 12, 13):

- Attenuation
- Center Frequency (60, 70, 80 and 100 Hz)
- Quality Factors (1, 1.25, 1.5 and 2)

3.3.5 DC mode

In this mode the DC gain is increased $57 \cdot .4 \text{ dB}$. In addition the programmed center frequency and quality factor is decreased by 25 % which can be used to reach alternative center frequencies or quality factors.

ete

3.3.6 Treble

There are two parameters programmable in the treble stage (see Figure 14, 15):

- Attenuation
- Cen.e. frequency (10, 12.5, 15 and 17.5 kHz).

3.3.7 Speaker attenuator

Due to practical aspects the steps in the speaker attenuator are not linear over the full range. At attenuations more than 24 dB the steps increase from 1.5 dB to 10 dB (please see data byte specification).









Figure 10. Bass control @ fc = 80 Hz, Q = 1

Figure 11. Bass center @ Gain = 14 dB, Q = 1

(1) In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx1111xx) where the center frequency is set to 150Hz instead of 100 Hz.



57

4 Stereo decoder part

4.1 Stereo decoder feature

- No external components necessary
- PLL with adjustment free fully integrated VCO •
- Automatic pilot dependent mono/stereo switching
- Very high suppression of intermodulation and interference
- Programmable roll-off compensation
- **Dedicated RDS Softmute**
- roductle High cut and stereo blend characteristics programmable in a wide range
- Internal Noise blanker with threshold controls
- Multipath detector with programmable internal/external influence
- I²C bus control of all necessary functions

Stereo decoder electrical characteristics 4.2

Table 8. Stereo decoder electrical characteristics

(V_S = 9 V; de-emphasis time constant = 50 μ s. V_{wirX} = 500 mV, 75 kHz deviation, f = 1 kHz. G_I = 6 dB, T_{amb} = 25 °C; unless otherwice specified)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{IN}	MPX input level	Input gain = 3.5 dB		0.5	1.25	VRMS
R _{in}	Input resistance		70	100	130	KΩ
G _{min}	Minimum input gain		1.5	3.5	4.5	dB
G _{max}	Max input ya'ı.		8.5	11	12.5	dB
G _{STEP}	Step resclution		1.75	2.5	3.25	dB
SVRR	Supply voltage ripple rejection	V _{ripple} = 100 mV, f = 1 kHz		55		dB
a	Max channel separation		30	50		dB
(THI)	Total harmonic distortion			0.02	0.3	%
$\frac{S+N}{N}$	Signal plus noise to noise ratio	S = 2 V _{rms}	80	91		dB
Mono/stereo s	witch					
V _{PTHST1}	Pilot threshold voltage	for Stereo, PTH = 1	10	15	25	mV
V _{PTHST0}	Pilot threshold voltage	for Stereo, PTH = 0	15	25	35	mV
V _{PTHMO1}	Pilot threshold voltage	for Mono, PTH = 1	7	12	17	mV
V _{PTHMO0}	Pilot threshold voltage	for Stereo, PTH = 0	10	19	25	mV
PLL						
Δf/f	Capture range		0.5			%

 Table 8.
 Stereo decoder electrical characteristics (continued)

 $(V_S = 9 \text{ V}; \text{ de-emphasis time constant} = 50 \ \mu\text{s}, V_{MPX} = 500 \text{ mV}, 75 \text{ kHz deviation}, f = 1 \text{ kHz}.$ $G_I = 6 \text{ dB}, T_{amb} = 25 \ ^\circ\text{C}; \text{ unless otherwise specified})$

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
De-emphasis	and high cut ⁽¹⁾					
τHC50	De-emphasis time constant	Bit = 7, Subadr. 10 = 0 $V_{LEVEL} >> V_{HCH}$	25	50	75	μs
τHC75	De-emphasis time constant	Bit = 7, Subadr. 10 = 1 $V_{LEVEL} >> V_{HCH}$	50	75	100	μS
τHC50	High cut time constant	Bit = 7, Subadr. $10 = 0$ V _{LEVEL} >> V _{HCL}	100	150	200	μS
τHC75	High cut time constant	Bit = 7, Subadr. 10 = 1 $V_{LEVEL} >> V_{HCL}$	150	225	300	μs
Stereo blend a	and high cut-control			-0	0	
REF5V	Internal reference voltage		1.7	T CS	5.3	V
TC _{REF5V}	Temperature coefficient			3300		ppm
L _{Gmin}	Min. level gain		-1	0	+1	dB
L _{Gmax}	Max. level gain	010	8	10	12	dB
L _{Gstep}	Level gain step resolution	05	0.3	0.67	1.0	dB
V _{SBLmin}	Min. voltage for mono	0,	29	33	37	%REF5V
V _{SBLmax}	Max. voltage for mono	1	54	58	62	%REF5V
V _{SBLstep}	Step resolution 5		5.0	8.4	12	%REF5V
VHCH _{min}	Min.voltage for no high out		36	42	46	%REF5V
VHCH _{max}	Max. voltage for הי nigh cut		62	66	70	%REF5V
VHCH _{step}	Step rosplution		5	8.4	12	%REF5V
VHCL _{min}	Min. voltage for full high cut		13	17	21	%VHCH
VHC ^I .m _{IX}	Iviax. voltage for full high cut		29	33	37	%VHCH
Carrier and ha	armonic suppression at the outp	ut	•	•		
α19	Pilot signal	f = 19 kHz	40	50		dB
α38	Sub carrier	f = 38 kHz		75		dB
α57	Sub carrier	f = 57 kHz		62		dB
α76	Sub carrier	f = 76 kHz		90		dB
Intermodulatio	on ⁽²⁾)	1	1	1		1
α2	Dilateignal	f _{mod} = 10 kHz f _{spur} = 1 kHz;		65		dB
α3	— Pilot signal	f _{mod} = 13 kHz; f _{spur} = 1 kHz;		75		dB



Table 8. Stereo decoder electrical characteristics (continued)

(V_S = 9 V; de-emphasis time constant = 50 μ s, V_{MPX} = 500 mV, 75 kHz deviation, f = 1 kHz. G_I = 6 dB, T_{amb} = 25 °C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
Traffic radio ⁽³⁾						
α57	Signal	f = 57 kHz		70		dB
SCA - Subsidia	ry communications authorization	on ⁽⁴⁾				
α67	Signal	f = 67 kHz		75		dB
ACI - Adjacent	channel interference ⁽⁵⁾					
α114	Signal	f = 114 kHz		95		dr3
α190	Signal	f = 190 kHz		84		dB

1. By design/characterization but functionally guaranteed through dedicated test mode structure

2. Intermodulation Suppression: measured with: 91% pilot signal; fm = 10kHz or 13kHz.

Traffic radio (V.F.) suppression: measured with: 91 % stereo signal; 9 % pilot signal; fm= 1 k lz, 5% sub carrier (f = 57 kHz, fm = 23 Hz AM, m = 60 %)

4. SCA (subsidiary communications authorization) measured with: 81% mono signer; 3% pilot signal; fm = 1 kHz; 1 0% SCA sub carrier (fs = 6 7 kHz, unmodulated).

5. ACI (adjacent channel interference) measured with: 90% mono signal; 9% ollo: signal; fm = 1 kHz; 1% spurious signal (fs = 110 kHz or 186 kHz, unmodulated).



4.3 Noise blanker part

- internal 2nd order 140 kHz high pass filter
- programmable trigger threshold
- additional circuits for trigger adjustment (deviation, field-strength)
- very low offset current during hold time
- four selectable pulse suppression times

able 9.	Noise blanker elect	trical characteristics					
Symbol	Parameter	Test condition	l	Min.	Тур.	Max.	Unit
			NBT = 111		30		mV _O
			NBT = 110		35	19	m / _O
			NBT = 101		40	775	mV _O
V _{TR}	Trigger threshold ^{(1), (2)}	meas. with V _{PEAK} = 0.9V	NBT = 100		45		mV _O
∨ TR	mgger intestiola conce	meas. With $v_{\text{PEAK}} = 0.5v$	NBT = 011	5	.:0		mV _O
			NBT = 010		55		mV _O
			NBT = 061	0	60		m۷ _O
			NET = 200		65		mV _O
			1 ICT = 00		260		mV _C
V	Noise Controlled	maga with V	NCT = 01		220		mV _C
V _{TRNOISE}	RNOISE Trigger Threshold ⁽³⁾	meas. with V _{PEAK} - 1.5V	NCT = 10		180		mV _C
		.(5)	NCT = 11		140		mV _O
		V _{MFX} ≃ CmV		0.5	0.9	1.3	V
V _{RECT}	Rectifier Voltage	V _{MPX} = 50mV; f = 150KHz		1.5	1.7	2.1	V
		V _{MPX} = 100mV; f = 150KHz		2.2	2.5	2.9	V
	N I		OVD = 11	0.5	0.9(off)	1.3	mV _O
V	ວະຫັສແດກ dependent ⁽⁴⁾	means. with V _{MPX} = 800mV	OVD = 10	0.9	1.2	1.5	mV _C
V _{RECT DEV}	rectifier voltage	(75KHz dev.)	OVD = 01	1.7	2.0	2.3	mV _C
S			OVD = 00	2.5	2.8	3.1	mV _C
		means. with	FSC = 11	0.5	0.9(off)	1.3	V
	Fieldstrength controlled ⁽⁵⁾	$V_{MPX} = 0mV$	FSC = 10	1.0	1.3	1.6	V
VRECT FS	rectifier voltage	V _{LEVEL} << V _{SBL}	FSC = 01	1.5	1.8	2.1	V
	-	(fully mono)	FSC = 00	2.0	2.3	2.6	V

 Table 9.
 Noise blanker electrical characteristics

1. All thresholds are measured using a pulse with T_R = 2 $\mu s,\,T_{HIGH}$ = 2 μs and T_F = 10 $\mu s.$

2. NBT represents the Noise blanker-Byte bits D2; D0 for the noise blanker trigger threshold

3. NAT represents the Noise blanker-Byte bit pair D4,D3 for the noise controlled trigger adjustment

4. OVD represents the Noise blanker-Byte bit pair D7,D6 for the over deviation detector

5. FSC represents the Fieldstrength-Byte bit pair D1,D0 for the fieldstrength control











Figure 13. Deviation controlled trigger adjustment





Figure 19. Fieldstrength controlled trigger adjustment

Multipath detector 4.4

- Internal 19 kHz bandpass filter
- Programmable bandpass and rectifier gain
- Two pin solution fully independent usable for external programming
- Selectable internal influence on Stereo devid

Table 10.	Multipath detector electrical characteristics
-----------	---

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
f _{CMP}	Center frequency of multipath- bandpass	stereo decoder locked on pilot tone		19		KHz
	.00.	bits D_2 , D_1 configuration byte = 00		6		dB
G	Bandp. ss gain	bits D_2 , D_1 configuration byte = 01		16		dB
G _{BPMP}	Banup iss gain	bits D_2 , D_1 configuration byte = 10		12		dB
10		bits D_2 , D_1 configuration byte = 11		18		dB
601		bits D_7 , D_6 configuration byte = 00		7.6		dB
RECTMP	Rectifier gain	bits D_7 , D_6 configuration byte = 01		4.6		dB
		bits D_7 , D_6 configuration byte = 10		0		dB
Існмр	Rectifier charge current			1		μA
IDISMP	Rectifier discharge current			1.5		mA



4.5 Description of stereo decoder

The stereo decoder part of the TDA7461 (see *Figure 20*) contains all functions necessary to demodulate the MPX signal like pilot tone dependent mono/stereo switching as well as "stereo blend" and "high cut" functions. Adaptations like programmable input gain, roll-off compensation, selectable de-emphasis time constant and a programmable fieldstrength input allow to use different IF devices.





4.5.1 Stereo decoder mute

The TDA7461 has a frast and easy to control RDS mute function which is a combination of the audioprocessor spinnute and the high-ohmic mute of the stereo decoder. If the stereo decoder is selected and a softmute command is sent (or activated through the SM pin) the stereo decoder will be set automatically to the high-ohmic mute condition after the audio signal bas been soft muted.

Hence a checking of alternate frequencies could be performed. To release the system from the mute condition simply the unmute command must be sent: the stereo decoder is unmuted immediately and the audioprocessor is softly unmuted. *Figure 21* shows the output signal V_0 as well as the internal stereo decoder mute signal. This influence of Softmute on the stereo decoder mute can be switched off by setting bit 3 of the Softmute byte to "0". A stereo decoder mute command (bit 0, stereo decoder byte set to "1") will set the stereo decoder in any case independently to the high-ohmic mute state.

If any other source than the stereo decoder is selected the decoder remains muted and the MPX pin is connected to Vref to avoid any discharge of the coupling capacitor through leakage currents.

4.5.2 Input stages

The In gain stage allows to adjust the MPX signal to a magnitude of about 1Vrms internally which is the recommended value. The 4th order input filter has a corner frequency of 80 kHz and is used to attenuate spikes and noise and acts as an anti aliasing filter for the following switch capacitor filters.



4.5.3 Demodulator

In the demodulator block the left and the right channel are separated from the MPX signal. In this stage also the 19 kHz pilot tone is cancelled. For reaching a high channel separation the TDA7461 offers an I²C bus programmable roll off adjustment which is able to compensate the lowpass behavior of the tuner section.

If the tuner attenuation at 38 kHz is in a range from 20.2 % to 31 % the TDA7461 needs no external network before the MPX pin. Within this range an adjustment to obtain at least 40 dB channel separation is possible. The bits for this adjustment are located together with the fieldstrength adjustment in one byte. This gives the possibility to perform an optimization step during the production of the carradio where the channel separation and the fieldstrength control are trimmed.



Figure 21. Signals during stereo decoder's soft mute

4.5.4 De-emphasis and high cut

The lovpass filter for the de-emphasis allows to choose between a time constant of 50 µs and 75 us (bit D7, Stereo decoder byte).

The high cut control range will be in both cases t_{HC} = 2 * t_{Deemp}. Inside the high cut control range (between VHCH and VHCL) the LEVEL signal is converted into a 5 bit word which controls the lowpass time constant between t_{Deemp} ...3 × t_{Deemp} .

There by the resolution will remain always 5 bits independently of the absolute voltage range between the VHCH and VHCL values. The high cut function can be switched off by I²C bus (bit D7, Fieldstrength byte set to "0").

4.5.5 PLL and pilot tone detector

The PLL has the task to lock on the 19 kHz pilotone during a stereo transmission to allow a correct demodulation. The included detector enables the demodulation if the pilot tone reaches the selected pilottone threshold VPTHST. Two different thresholds are available. The detector output (signal stereo, see block diagram) can be checked by reading the status byte of the TDA7461 via I²C bus.



4.5.6 Fieldstrength control

The fieldstrength input is used to control the high cut and the stereo blend function. In addition the signal can be also used to control the noise blanker thresholds.

4.5.7 Level input and gain

To suppress undesired high frequency modulation on the high cut and stereo blend function the LEVEL signal is lowpass filtered firstly. The filter is a combination of a 1st order RC lowpass at 53 kHz (working as anti-aliasing filter) and a 1storder switched capacitor lowpass at 2.2 kHz. The second stage is a programmable gain stage to adapt the LEVEL signal internally to different IF.

The gain is widely programmable in 16 steps from 0 dB to 10 dB (step = 0.67 dB). These 4 bits are located together with the Roll-Off bits in the "Stereo decoder Adjustment" byte to simplify a possible adaptation during the production of the carradio.





4.5.8 Stere blend control

The stereo blend control block converts the internal LEVEL voltage (LEVEL INTERN) into an demodulator compatible analog signal which is used to control the channel separation between 0dB and the maximum separation. Internally this control range has a fixed upper limit which is the internal reference voltage REF5V. The lower limit can be programmed to be 33%, 42%, 50% or 58% of REF5V (see *Figure 23*).

To adjust the external LEVEL voltage to the internal range two values must be defined: the LEVEL gain L_G and VSBL. To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain LG has to be defined. The following equation can be used to estimate the gain:

L_G = REF5V Field strength voltage[STEREO]

The gain can be programmed through 4 bits in the "Stereo decoder-Adjustment" byte.

The MONO voltage VMO (0 dB channel separation) can be chosen selecting 33, 42, 50 or 58 % of REF5V.



All necessary internal reference voltages like REF5V are derived from a band gap circuit. Therefore they have a temperature coefficient near zero. This is useful if the fieldstrength signal is also temperature compensated.

But most IF devices apply a LEVEL voltage with a TC of 3300 ppm. The TDA7461 offers this TC for the reference voltages, too. The TC is selectable with bit D7 of the "stereo decoder adjustment" byte.

Figure 23. Relation between internal and external LEVEL voltage and setup of Stereo blend



4.5.9 High cut control

The high cut control setup is similar to the steried bend control setup: the starting point VHCH can be set with 2 bits to be 42, 50, ∞ cr 66% of REF5V whereas the range can be set to be 17 or 33% of VHCH (see *Figure* 24).





4.6

FUnctional description of the noise blanker

In the automotive environment the MPX signal is disturbed by spikes produced by the ignition and for example the wiper motor. The aim of the noise blanker part is to cancel the audible influence of the spikes. Therefore the output of the stereo decoder is held at the actual voltage for 40 μ s.

In a first stage the spikes must be detected but to avoid a wrong triggering on high frequency (white) noise a complex trigger control is implemented. Behind the trigger stage a pulse former generates the "blanking" pulse. To avoid any crosstalk to the signal path the noise blanker is supplied by his own biasing circuit.



4.6.1 Trigger path

The incoming MPX signal is highpass filtered, amplified and rectified. This second order highpass-filter has a corner frequency of 140 kHz. The rectified signal, RECT, is lowpass filtered to generate a signal called PEAK. Also noise with a frequency 140 kHz increases the PEAK voltage. The PEAK voltage is fed to a threshold generator, which adds to the PEAK voltage a DC dependent threshold VTH. Both signals, RECT and PEAK+VTH are fed to a comparator which triggers a re-triggerable monoflop. The monoflop's output activates the sample-and-hold circuits in the signalpath for 40 µs.

The block diagram of the noiseblanker is given in Figure 25.

4.6.2 Automatic noise controlled threshold adjustment (ATC)

There are mainly two independent possibilities for programming the trigger threshold

the low threshold in 8 steps (bits D0 to D2 of the noiseblanker byte)

the noise adjusted threshold in 4 steps (bits D3 and D4 of the noiseblanirer byte, see fig. 18).

The low threshold is active in combination with a good MPX signal without any noise; the PEAK voltage is less than 1V. The sensitivity in this operation is high.

If the MPX signal is noisy the PEAK voltage increases due to the higher noise, which is also rectified. With increasing of the PEAK voltage the ingger threshold increases, too. This particular gain is programmable in 4 steps (see Figure 17).



Figure 25. Block diagram of the noise blankert

4.6.3 Automatic threshold control

Besides the noise controlled threshold adjustment there is an additional possibility for influencing the trigger threshold. It is depending on the stereo blend control.

The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise-controlled trigger adjustment is fixed (*Figure 19*). In some cases the behavior of the noise blanker can be improved by increasing the threshold even in a region of higher fieldstrength. Sometimes a wrong triggering occurs for the MPX signal often shows distortion in this range which can be avoided even if using a low threshold.



Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by stereo blend. This threshold increase is programmable in 3 steps or switched off with bits D0 and D1 of the fieldstrength control byte.

4.6.4 Over deviation detector

If the system is tuned to stations with a high deviation the noise blanker can trigger on the higher frequencies of the modulation. To avoid this wrong behavior, which causes noise in the output signal, the noise blanker offers a deviation dependent threshold adjustment. By rectifying the MPX signal a further signal representing the actual deviation is obtained. It is used to increase the PEAK voltage. Offset and gain of this circuit are programmable in 3 steps with the bits D6 and D7 of the stereo decoder byte (the first step turns off the detector, see *Figure 18*).

4.7 Functional description of the multipath detector

Using the internal detector the audible effects of a multipath condition can be minimized. A multipath condition is detected by rectifying the 19 kHz spectrum in the fieldstrength signal.

Selecting the "internal influence" in the configuration byte, the channel separation is automatically reduced during a multipath condition according to the voltage appearing at the MPOUT pin.

To obtain a optimal performance an adaptation is necessary. Therefore the gain of the 19 kHz bandpass is programmable in four stops as well as the rectifier gain. The attack and decay times can be set by the external capacitor value.

4.8 Test mode

During the test nocle which can be activated by setting bit D0 of the testing byte and bit D5 of the subaddress byte to "1" several internal signals are available at the CASSR pin. During this mode in put resistance of 100 k Ω is disconnected from the pin. The internal signals available are shown in the software specification.

Figure 26. Block diagram of the multipath detector



57

5



Figure 27. Application example 1

5 I²C bus interface description

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read/ write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

Figure 29. Interface protocol diagram



,50

S = Start ACK = Acknowledge AZ = AutoZero-Remain T = Testing I = Auto increment P = Stop Max. clock speed: 500 kbits/s

The transmitted data is a nomatically updated after each ACK.

Transmission car up repeated without new chip address.

5.2 Auto increment

It but I in the subaddress byte is set to "1", the auto increment of the subaddress is enabled.

Table 11. Transmitted data (send mode)

MSB							LSB
Х	Х	Х	Х	ST	SM	Х	Х

SM = Soft mute activated

ST = Stereo

X = Not used



MSB							LSB	FUNCTION
х	AZ	т	I	A3	A2	A1	A0	FUNCTION
				0	0	0	0	Input selector
				0	0	0	1	Loudness / Auto-Zero
				0	0	1	0	Volume
				0	0	1	1	Softmute / Beep
				0	1	0	0	Bass / Treble Attenuator
				0	1	0	1	Bass / Treble Configuration
				0	1	1	0	Speaker attenuator LF
				0	1	1	1	Speaker attenuator L'1
				1	0	0	0	Speaker attentiator FiF
				1	0	0	1	Speaker attenuator RR / Blank time adjust
				1	0	1	0	Siereo decoder
				1	0	1		Noise blanker
				1	1	υ	D o	Fieldstrength Control
				1	1	0	1	Configuration
				1		1	0	Stereo decoder Adjustment
					1	1	1	Testing

Table 12. Subaddress (receive mode)

T = Testmode

I = Auto increase at

AZ = At to Zero Remain

N

X = not used



Data byte specification 6

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Source selector
					0	0	0	CD
					0	0	1	Cassette
					0	1	0	Phone
					0	1	1	AM
					1	0	0	Stereo Decoder
					1	0	1	Input FM
					1	1	0	Mute
					1	1	1	AC inputs
								CE m Ja ?
				0				CD Full-differential
				1			Å	CD Quasi-diff
							-0-	AM/FM mode
			1		0	a	1	AM mono
			0		U	1	1	AM stereo
			0			0	0	AM through Stereo decoder
			1	~ ^	1	0	0	FM- Stereo decoder
				5				In-gain
0	0	0						14 dB
0	0	1						12 dB
:	: _							:
1	220	0						2 dB
	1	1						0 dB

Table 13. Input selector



MSB LS							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Attenuation
				0	0	0	0	0 dB
				0	0	0	1	-1 dB
				:	:	:	:	:
				1	1	1	0	-14 dB
				1	1	1	1	-15 dB
								Filter
			0					on
			1					off (flat)
								Center frequency
		0						200 Hz
		1						400 Hz
								Lou iness Q
	0						5	P.cw (1 ^s t order)
	1						0	normal (2 nd order)
1						cC		must be "1"

Table 14. Loudness

Note: The attenuation is specified at high frequencies. Around the center frequency the value is different depending on the programmed attenuation (cee Loudness frequency response).


MSB							LSB	Function	
D7	D6	D5	D4	D3	D2	D1	D0	1 diletion	
				0	0 0 1 1	0 1 0 1	0	Mute Enable Softmute Disable Softmute Mute time =0.48 ms Mute time =0.96 ms Mute time =40.4 ms Mute time =324 ms Stereo decoder softmute influence = off Stereo decoder softmute influence = on	
			0 1					Beep Bc∋p Fr⊳quency = 600 Hz Bee⊾ Frequency = 1.2 kHz	
0 0 1 1	0 1 0 1	0 1		5	0%	50	et	Mixing Mix-Source = Beep Mix-Source = Phone Full Mix Signal Source -12 dB + Mix-Signal -2.5 dB Source -6 dB + Mix-Signal -6 dB Full Source	

Table 15. Mute, Beep and Mixing

Note: for more information on the Stereo decoder-Softmute-Influence please refer to the stereo decoder description.

57

Table I	•. •	olume							
MSB							LSB	Function	
D7	D6	D5	D4	D3	D2	D1	D0	Function	
								Gain/Attenuation	
	0	0	0	0	0	0	0	+32 dB	
	0	0	0	0	0	0	1	+31 dB	
	:	:	:	:	:	:	:	:	
	0	0	0	1	1	0	0	+20 dB	
	0	0	0	1	1	0	1	+19 dB	
	0	0	0	1	1	1	0	+18 dB	
	:	:	:	:	:	:	:	:	
	0	0	1	1	1	1	1	+1 dB	
	0	1	0	0	0	0	0	0 dB	
	0	1	0	0	0	0	1	- 1 dB	
	:	:	:	:	:	:	:		
	1	1	0	1	1	1	0	-78 33	
	1	1	0	1	1	1	1	-79 1B	
							X	Soft step	
0							10,	Soft step volume = off	
1						CC C		Soft step volume = on	

Table 16. Volume

Note: It is not recommended to use a gain mole than 20dB for system performance reason. In general, the max. gain should be limited by software to the maximum value, which is needed for the system.



MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Treble steps
				0	0	0	0	-14 dB
				0	0	0	1	-12 dB
				:	:	:	:	:
				0	1	1	0	-2 dB
				0	1	1	1	0 dB
				1	1	1	1	0 dB
				1	1	1	0	+2 dB
				:	:	:	:	: .(5)
				1	0	0	1	+12 dB
				1	0	0	0	+14 dB
								Bass steries
0	0	0	0					-1-(dF)
0	0	0	1					-12 c'B
:	:	:	:				X	S
0	1	1	0				6	-2 dB
0	1	1	1			C C		0 dB
1	1	1	1		N	5		0 dB
1	1	1	0		()			+2 dB
:	:	:	:					:
1	0	0	1					+12 dB
1	0	0	0	01				+14 dB

Table 17. Bass and treble attenuation

For example 12dB T: ble and -8dB Bass give the following data byte: 0 0 1 1 1 0 0 1.

57

MSB							LSB	Function	
D7	D6	D5	D4	D3	D2	D1	D0	Tunction	
								Treble	
						0	0	Center Frequency = 10 kHz	
						0	1	Center Frequency = 12.5 kHz	
						1	0	Center Frequency = 15 kHz	
						1	1	Center Frequency = 17.5 kHz	
								Bass	
				0	0			Center Frequency = 60 Hz	
				0	1			Center Frequency = 70 Hz	
				1	0			Center Frequency = 80 Hz	
				1	1			Center Frequency = 100 Hz	
		1	1	1	1			Center Freque: cy = 150 Hz	
		0	0					Quality factor 1	
		0	1					QL alit / $actor = 1.25$	
		1	0					Quality factor = 1.5	
		1	1				X	Cuality factor = 2	
	0						6	DC-Gain = 0 dB	
	1					c		DC-Gain = ±4.4 dB	
						0		AC Coupling ⁽¹⁾	
0					U)	Ĺ		For External Connection	
1								Internally Connection	

Table 18. Bass and treble filter characteristics

1. For deeper information see opplier tic n examples *Figure 27* and *28*.

For example Treble cente: 1:ec,uency = 15kHz, Bass center frequency = 100Hz, Bass Q = 1 and DC = 0dB give the following DA: 4 3Y TE: 1 0 0 0 1 1 1 0



MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Attenuation
		0	0	0	0	0	0	0 dB
		0	0	0	0	0	1	-1 dB
		:	:	:	:	:	:	:
		0	1	0	1	1	1	-23 dB
		0	1	1	0	0	0	-24.5 dB
		0	1	1	0	0	1	-26 dB
		0	1	1	0	1	0	-28 dB
		0	1	1	0	1	1	-28 dB -30 dB -32 dB -35 dB -40 dB
		0	1	1	1	0	0	-32 dB
		0	1	1	1	0	1	-35 dB
		0	1	1	1	1	0	-40 dB
		0	1	1	1	1	1	-50 dB
		1						Speaker 1 ute
1	1							N'มะ : o э "1" (except RF, RR speaker; s
								(below)
							10	Blank Time adj. (subaddress speaker
0	0							RR)
0	1							38 μs
1	0							25.5 μs
1	1		1	G				32 μs
								22 μs
			$\langle \mathcal{O} \rangle$					Output selector for pins 15 and 16.
			5					subaddress speaker RF)
	0	\mathbf{D}						Stereo decoder output selected
e								Input multiplexer output selected

 Table 19.
 Speaker attenuation (LF, LR, RF, RR)



57

MSB							LSB	Function	
D7	D6	D5	D4	D3	D2	D1	D0	Function	
							0	STD unmuted	
							1	STD muted	
					0	0		IN-Gain 11 dB	
					0	1		IN-Gain 8.5 dB	
					1	0		IN-Gain 6 dB	
					1	1		IN-Gain 3.5 dB	
				1				Stereo decoder Unmuted with Stdeo Input selected and automatically Muted at the selection of any other source.	
				0				Stereo decoder Urin utba whicheve is the selected source.	
		1 0	1					Forsed mono Moi o/stereo switch automatically	
	0 1						e	Pilot threshold high Pilot threshold low	
0						S		De-emphasis 50 µs	
1						D		De-emphasis 75 μs	

Table 20. Stereo decoder

Table	21.	Noise	blanker	

Table			anner					
MSB			.19	51			LSB	Function
D7	D6	D5	D.1	D3	D2	D1	D0	Function
		77			0	0	0	Low threshold 65 mV
	5				0	0	1	Low threshold 60 mV
4	\mathbf{D}	Í .			0	1	0	Low threshold 55 mV
0					0	1	1	Low threshold 50 mV
					1	0	0	Low threshold 45 mV
					1	0	1	Low threshold 40 mV
					1	1	0	Low threshold 35 mV
					1	1	1	Low threshold 30 mV
			0	0				Noise controlled threshold 320 mV
			0	1				Noise controlled threshold 260 mV
			1	0				Noise controlled threshold 200 mV
			1	1				Noise controlled threshold 140 mV
		0						Noise blanker off
		1						Noise blanker on
0	0							Over deviation adjust 2.8 V
0	1							Over deviation adjust 2.0 V
1	0							Over deviation adjust 1.2 V
1	1							Over deviation detector off

MSB							LSB	Function	
D7	D6	D5	D4	D3	D2	D1	D0	Function	
						0	0	Noise blanker Field strength Adj 2.3 V	
						0	1	Noise blanker Field strength Adj 1.8 V	
						1	0	Noise blanker Field strength Adj 1.3 V	
						1	1	Noise blanker Field strength Adj Off	
				0	0			VSBL at 33 % REF 5 V	
				0	1			VSBL at 42 % REF 5 V	
				1	0			VSBL at 50 % REF 5 V	
				1	1			VSBL at 58 % REF 5 V	
		0	0					VHCH at 42 % REF 5 V	
		0	1					VHCH at 50 % REF 5 V	
		1	0					VHCH at 58 % ₽Er 5 V	
		1	1					VHCH at 66 % FEF 5 V	
	1							VHCL a' 17 % VHCH	
	0							VHUL at 33 % VHCH	
0							X	H,gh cut OFF	
1							10,	High cut ON	
Table 2	23. C	onfigu	ration			S			

Table 22. Field strength control



	MSB					O	2	LSB	Function
	D7	D6	D5	D4	D3	D2	D1	D0	Tunction
					5				Noise rectifier discharge resistor
				\sim	~		0	0	R = infinite
			ΔO				0	1	R = 56 kΩ
		. (\mathbf{O}				1	0	R = 33 kΩ
		220					1	1	R =18 kΩ
									Multipath detector bandpass gain
	KO				0	0			6 dB
16	l)				0	1			16 dB
cO'					1	0			12 dB
obsole					1	1			18 dB
O P									Multipath detector internal
									influence
				0					On
				1					Off
			1						Mute be "1"
									Multipath detector reflection gain
	0	0							Gain = 7.6 dB
	0	1							Gain = 4.6 dB
	1	0							Gain = 0 dB
	1	1							Off



\mathbf{N}
5
at leve
`
)
e

Table 24. Stereo decoder adjustment





MSB							LSB	Eurotion
D7	D6	D5	D4	D3	D2	D1	D0	Function
							0 1	Stereo decoder test signals OFF Test signals enabled if bit D5 of the subaddress (test mode bit) is set to "1", too
						0 1		External Clock Internal Clock
		0 0 0 0 0 0 1 1 1 1 1 1 1	0 0 0 1 1 1 1 0 0 0 0 1 1 1	0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 1 0 0 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1 0 1 0 1 0 1	50	et	Test signals at CASS_R VHCCH Level intern Pilot magnitu æ VCOCCN: V CO Control Voltage Pilot threshold HOLDN NB threshold F228 VHCCL VSBL not used not used PEAK not used REF5V not used
xe	0 1							VCO Off On
0								Audio processor test mode Only if bit D5 of the subaddress (tes mode bit) is set to "1" Off

Table 25. Testing

Note: This byte is used for testing or evaluation purposes only and must not be set to other values than the default "11111110" in the application!



57

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: <u>www.st.com</u>.

ECOPACK[®] is an ST trademark.



Figure 30. SO-28 mechanical data and package dimensions

8 Revision history

Table 26.Document revision history

	Date	Revision	Changes
	20-Oct-2003	6	Initial release.
	13-Jan-2009	7	Document reformatted. Document status changed from datasheet to "not for new design". Removed all refences to DIP28 package. Added <i>Table 1: Device summary on page 1.</i> Updated <i>Section 7: Package information on page 46.</i>
Added Table 1: Device summary on page 1. Updated Section 7: Package information on page 48.			



Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidia. ie: (ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and ser ices doscribed herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and solvices described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property Liq. is is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a License grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a tria ranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein or considered as a tria ranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained to the trian the trian trian.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR BALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNE'S FOP A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN VIRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRCD JC 'S OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PF OP IN TY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of S. p. or ucts with provisions different from the statements and/or technical features set forth in this document shall immediately void any war any granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability, or of.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2009 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

