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APPLICATION NOTE 5292

External Filters for the Analog Inputs of Metering ICs

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Abstract: This application note examines ways to reduce adverse side effects, such as crosstalk and inaccuracies, in the Maxim portfolio of Teridian™ energy metering ICs. After briefly reviewing the ADC inputs, this article discusses the effect of different capacitors and resistors on metering ICs, as well as the use of ferrite beads to reduce RF susceptibility.

Introduction

This application note discusses the design of external filters connected to the analog inputs of the Maxim portfolio of Teridian energy metering ICs. In most cases, these external filters will be lowpass filters that help reject high-frequency signals, such as noise from photovoltaic inverters. Precautions for filter design and component selections are discussed. Following these guidelines will ensure that unwanted side effects such as crosstalk, inaccuracy over temperature, or phase shift with load currents are avoided.

Basic ADC Input Concepts

The ADC inputs of the Teridian 71M6531/71M6532/71M6533/71M6534 family of ICs are multiplexed to an unbuffered, switched capacitor network. **Figure 1** shows an ideal simplified equivalent circuit of this network when the multiplexed switches are closed on one input. There are two clocks (θ_1 and θ_2) driving the switches (P1 and P2) that are 180 degrees out of phase.

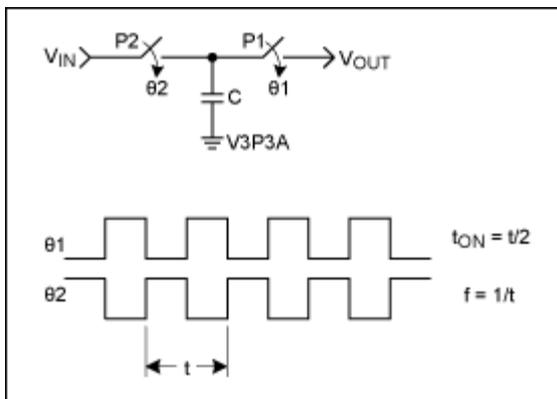
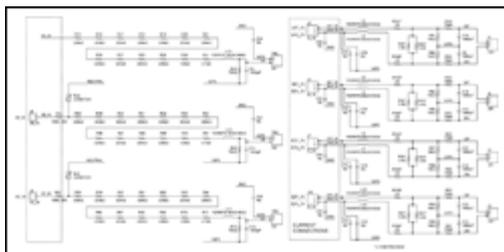


Figure 1. Simplified equivalent circuit of a switched capacitor input network.

When P2 closes, P1 opens and the capacitor (C) charges to the input level of V_{IN} . The converse occurs when P2 opens and P1 closes, namely the capacitance charge is transferred to the FIR filter represented as V_{OUT} . Because the frequency of the clocks is approximately 5MHz, the transfer ideally should occur within approximately $2/(5\text{MHz})$. Maxim recommends using a 1000pF capacitor at the ADC inputs to act as a "charge" reservoir to facilitate this transfer. In addition, Maxim recommends using a series resistor on the phase current ADC inputs to balance the 750Ω termination resistor on the divider string of the phase voltage resistor. Maxim uses 750Ω resistors in demo boards as illustrated in **Figure 2**.



[More detailed image.](#) (PDF, 304kB)

Figure 2. Circuits of demo board voltage and current input.

Figure 3 shows the effects of the components on the switched capacitor equivalent circuit. It includes the impedance of the input multiplexer and P2 switches.

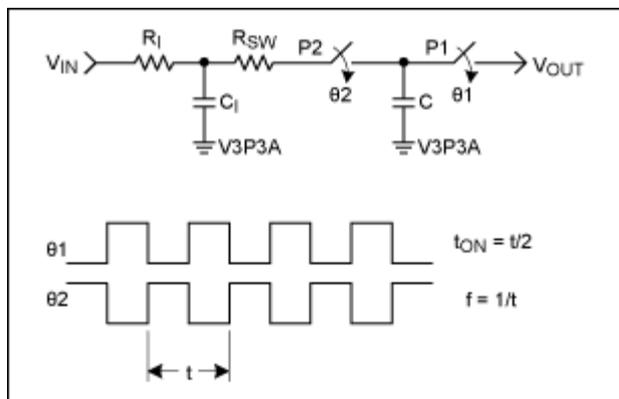


Figure 3. Switched capacitor network with RC Input.

See Equation 1 for the voltage on the switched capacitor (C) when P2 is closed and P1 is open. The design goal is for VC to settle by approximately 5 tau before the switch P1 closes. If it does not settle, the effect becomes a gain offset in the A/D channel. This gain offset can be compensated for by magnitude calibration as long as the offset does not exceed a factor of two (i.e., the range of the CAL_Ix and CAL_Vx).

$$V_C(t) = V_{IN} \left(1 - e^{-\frac{t}{2f(R_I + R_{SW})(C + C_I)}} \right) \quad (\text{Eq. 1})$$

A lowpass filter, if needed or desired, can replace the balance resistor and reservoir capacitor. The concepts of the switched capacitor network ADC input discussed above contribute to understanding the selection of this resistor and the capacitor values for ADC accuracy.

Selecting the Type of Capacitor

Depending on the use of the component, the type of capacitor selected can be an important factor. If the capacitor performs as a reservoir capacitor to facilitate the charge transfer in the switched capacitor network, then using an X7R-type capacitor is acceptable. This reservoir capacitor, which uses the recommended Maxim values (1000pF and 750Ω), and the impedance-balancing resistor comprise the lowpass filter. This lowpass filter forms a 212kHz, 3dB frequency point that has extremely small influence on the frequency response of interest, typically up to the 20th harmonic of the fundamental frequency.

If an anti-aliasing filter or a filter to reject higher frequency noise is being used (generally a low pass filter), these filter types typically form a lower 3dB frequency point that affects the fundamental frequency gain and phase. In these cases, selection of the circuit components is more critical.

Because of its characteristics, an NPO-type capacitor would be a better choice for the capacitor. It is more stable over temperatures than an X7R-type capacitor, typically $\pm 30\text{ppm}/^\circ\text{C}$ vs. $\pm 15\%$ ($\pm 883\text{ppm}/^\circ\text{C}$ over -55°C to $+125^\circ\text{C}$). Additionally, the low AC frequency and voltage characteristics of the NPO-type capacitor are better than the X7R-type capacitor.

Figure 4 shows the effect of a 50Hz, small amplitude signal on both the NPO-type and X7R-type capacitors. The NPO-type capacitors that were tested have nearly identical responses, but the X7R-type capacitors show a voltage coefficient. This change of capacitance is a source of inaccuracy in Wh over phase as meter load current changes.

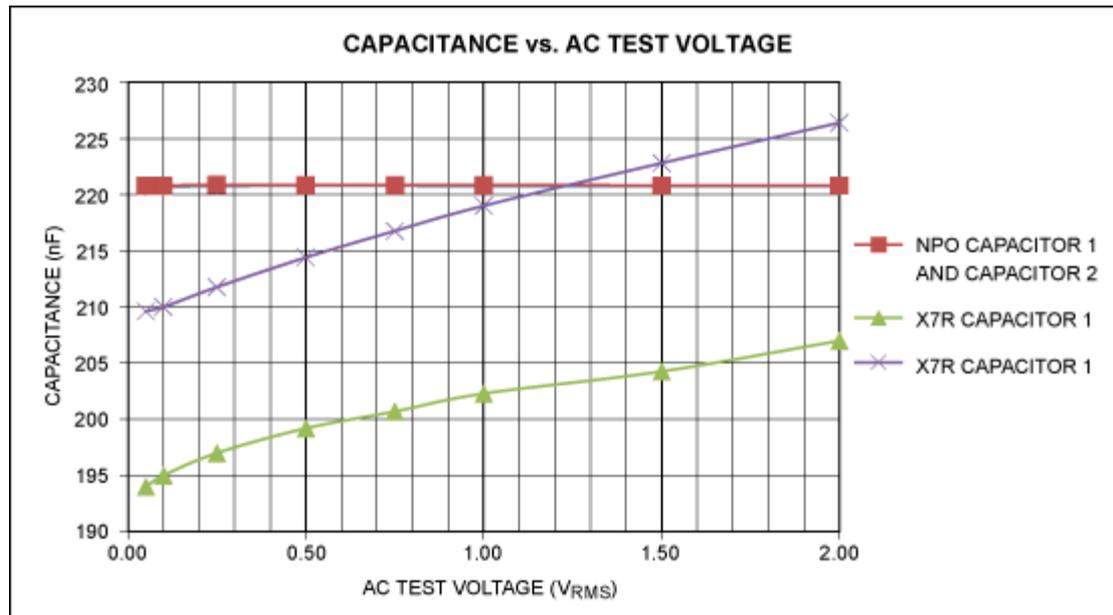


Figure 4. The effect of a 50Hz amplitude signal on NPO-type and X7R-type capacitors.

Figure 5 shows this inaccuracy as a percent change of capacitance. To illustrate this effect, consider a typical 200A_{RMS} meter using current transformers (CTs) that is calibrated at 30A_{RMS} for magnitude and phase at room temperature. If the AC voltage from a CT sensor with a burden resistor at the current ADC input is 0.177V_{RMS} at 200A_{RMS}, then the AC voltage of a 200A_{RMS} meter calibrated at 30A_{RMS} is 0.027V_{RMS}. The change of capacitance is approximately 1.5%. This difference becomes an uncompensated phase shift on the current channels and a source of inaccuracy in Wh readings when the power factor (PF) changes from 1.0 to 0.5.

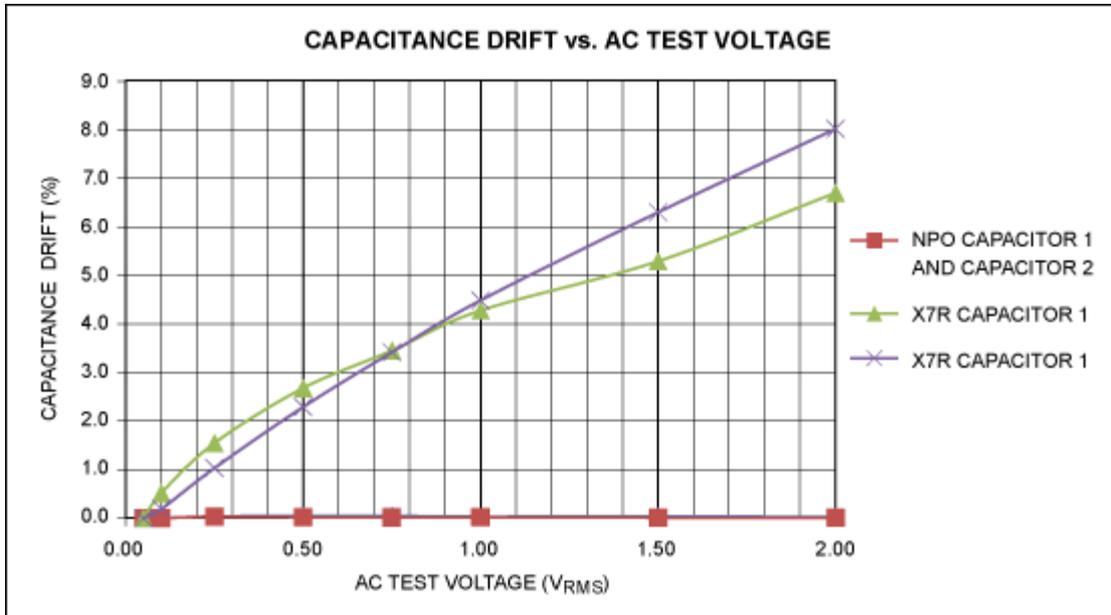


Figure 5. Inaccuracy due to capacitance drift.

Finally, the NPO-type capacitor has better aging characteristics than the X7R-type capacitor. **Figure 6** shows that the X7R capacitance decreases over time. This decrease is caused by the relaxation or realignment of the electrical dipoles within the capacitor. The NPO-type capacitor does not experience this phenomenon.

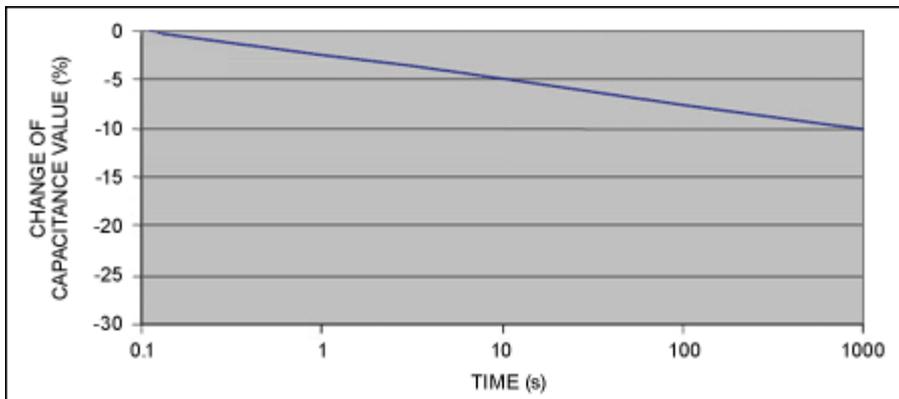


Figure 6. The effects of aging capacitors.

Selecting the Type of Resistor

The type of resistor selected for either the balance resistor or the lowpass filter is not as critical as the type of capacitor selected. A 1% resistor can be used for both the balance resistor and the lowpass filter since these are generally low cost and their tolerances are compensated during magnitude calibration. Care should be made to select the best temperature coefficient for the lowpass filter to reduce inaccuracies in Wh accuracy over temperature.

RF Rejection Filters

One of the biggest challenges facing meter design is RF susceptibility. With the advent of more powerful radio devices for automatic meter reading (AMR) within the power meter, RF fields in the proximity of the metering ICs have increased beyond the levels listed in metering standards. To reject these RF fields, many meter designers use ferrite beads to essentially "burn off" this RF energy.

The typical approach is to place ferrite beads at the points where the phase voltage and phase currents enter the printed circuit boards (PCBs) to "burn off" the RF energy before it can enter any circuitry. However, there seems to be a design trend of placing ferrite beads further down line and in some cases, right at the ADC input of the metering ICs. This trend may be due to RF energy still entering into the circuitry of the PCB because of the antenna position.

Maxim has found that placing the ferrite bead directly in series with the ADC input of the 71M653X causes inaccuracies in Wh readings over temperature. These inaccuracies are caused by the interaction of the ferrite bead inductance with the switched capacitor network. The ferrite bead is modeled as an inductance and a resistance. **Figure 7** shows the simplified equivalent circuit of the switched capacitor network, which includes a ferrite bead model.

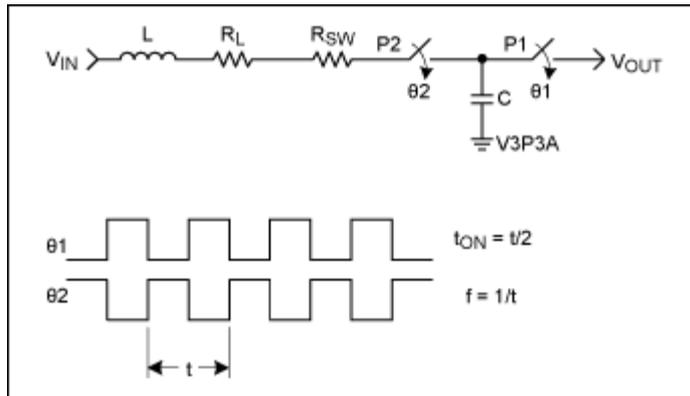


Figure 7. Simplified equivalent circuit of the switched capacitor network with ferrite bead.

When P2 is closed and P1 is open, the model becomes a classic RLC circuit. Equations 2, 3, and 4 show the current loop calculations for this circuit.

$$\frac{d^2i(t)}{dt^2} + 2\alpha \frac{di}{dt} + \omega_0^2 i(t) = 0 \quad (\text{Eq. 2})$$

Where

$$\alpha = \frac{R_{EQ}}{2L} \quad \omega_0 = \frac{1}{\sqrt{LC}} \quad (\text{Eq. 3})$$

And the damping factor is

$$\delta = \frac{R_{EQ}}{2} \sqrt{\frac{C}{L}} \quad (\text{Eq. 4})$$

The value of the damping factor determines the behavior of the current.

If $\delta > 1$, i.e., over damped, then calculate

$$i(t) = A_1 e^{-\omega_0(\delta + \sqrt{\delta^2 - 1})t} + A_2 e^{-\omega_0(\delta - \sqrt{\delta^2 - 1})t} \quad (\text{Eq. 5})$$

If $\delta = 1$, i.e., critical damped, then calculate

$$i(t) = D_1 t e^{-\alpha t} + D_2 e^{-\alpha t} \quad (\text{Eq. 6})$$

If $\delta < 1$, i.e., under damped, then calculate

$$i(t) = B_1 e^{-\alpha t} (\cos \omega_d t) + B_2 e^{-\alpha t} (\sin \omega_d t) \quad (\text{Eq. 7})$$

And

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \quad (\text{Eq. 8})$$

To calculate the damping factor value, the L and R of the ferrite at the signal frequency need to be determined.

Figure 8 shows the characteristics of the Murata BLM15HD102SN1D as an example. The L is approximately $1\mu\text{H}$ and $R = 0.1\Omega$ (use DC resistance for this discussion) in the 50Hz to 60Hz range.

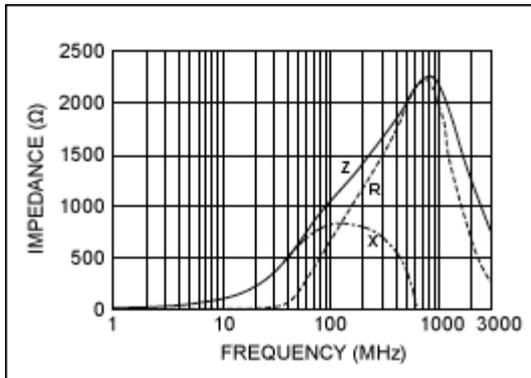


Figure 8. Example characteristics to calculate the dampening factor value.

With these values and $R_{SW} = 50\Omega$, the damping factor is 0.08, i.e., under damped. Figure 9 shows the decaying oscillatory response of this under damped response in the bottom signal.

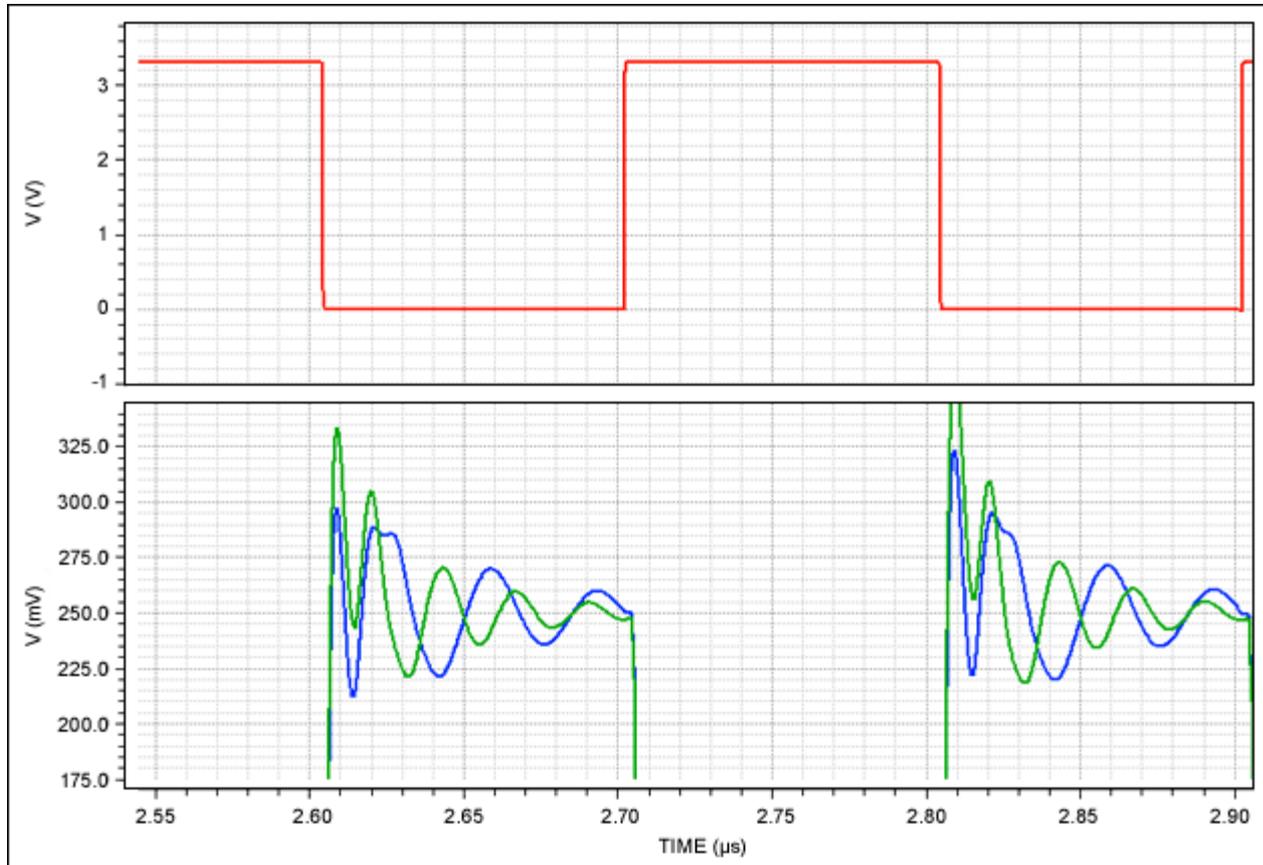


Figure 9. Switched capacitor voltage with ferrite bead at ADC input.

In **Figure 9**, the single-ended ADC input is 0.25V. The **red** signal is P1. The **blue** signal is the voltage across the switched capacitor (C) with $L = 1\mu\text{H}$, $R = 0.1\Omega$, $R_{\text{SW}} = 50\Omega$, and $C = 10\text{pF}$. The **green** signal is the voltage across the switched capacitor (C) with $L = 2\mu\text{H}$, $R = 0.1\Omega$, $R_{\text{SW}} = 50\Omega$, and $C = 10\text{pF}$.

Note that when the L value changes over temperature from $1\mu\text{H}$ to $2\mu\text{H}$, the response changes. The resultant offset value is different from what was magnitude compensated at room temperature and produces an inaccuracy in the Wh readings even at $\text{PF} = 1$. Because of this effect, Maxim recommends not placing ferrite beads directly in series with the ADC input.

If using a ferrite bead near the metering IC, Maxim recommends placing it before the balance resistor and reservoir capacitor (see **Figure 10**).

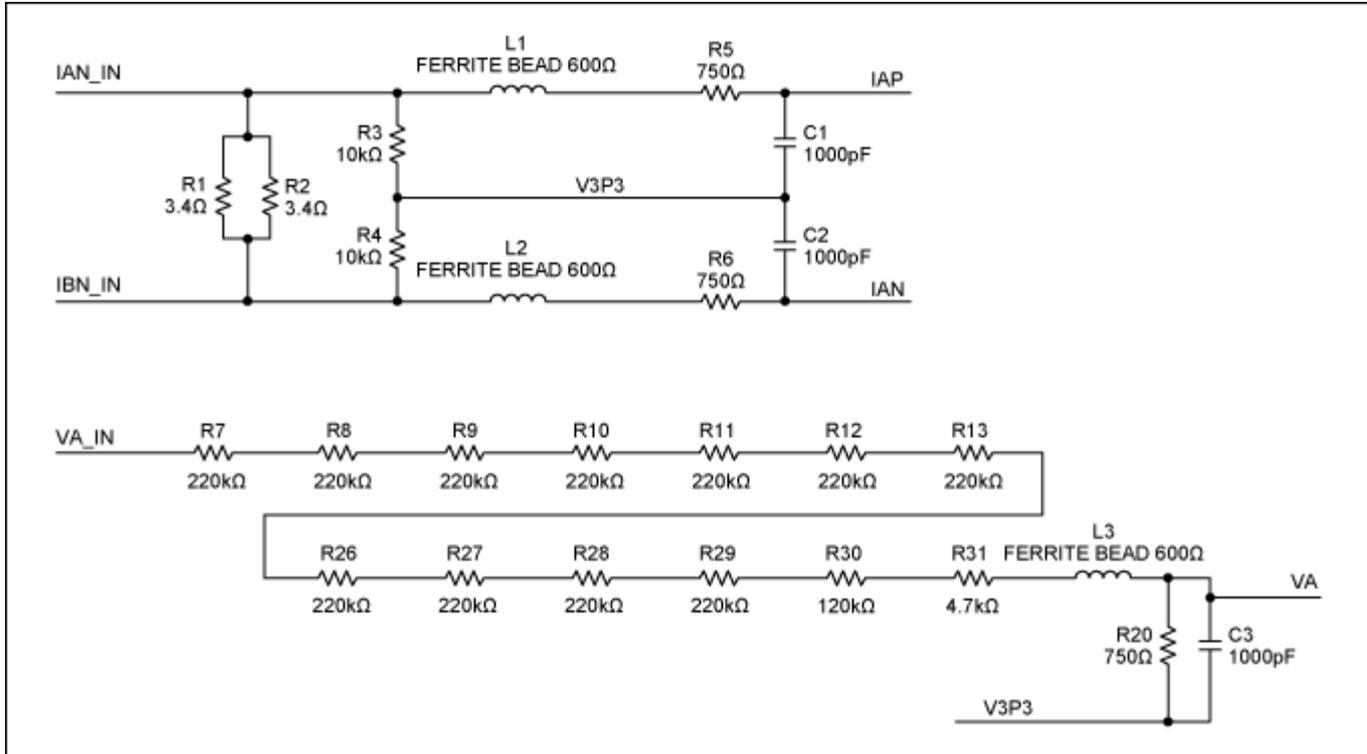


Figure 10. Recommended ferrite bead placement near ADC input.

Figure 11 shows the effect of this placement in the top signal. The response dampens quickly before P1 is closed. An alternative method would be to place a resistor between the ferrite bead and the ADC input and to change the damping factor.

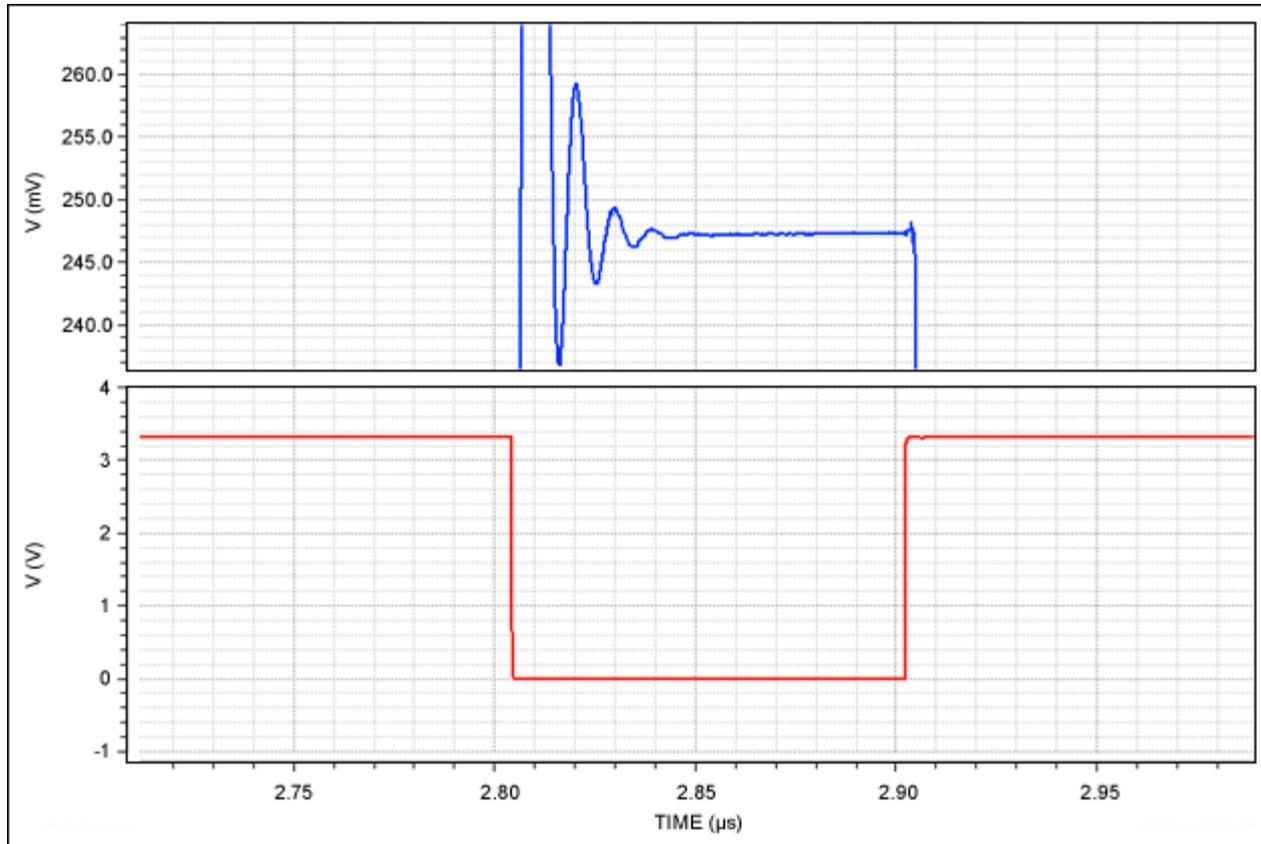


Figure 11. Switched capacitor voltage with ferrite bead and RC at ADC input.

In Figure 11, the single-ended ADC input is 0.25V. The red signal is P2. The blue signal is the voltage across the switched capacitor (C) with $L = 1\mu\text{H}$, $R = 750\Omega$, and $C = 1000\text{pF}$.

Conclusion

Because of the unbuffered switched capacitor network, care must be taken when selecting components for filters that interface with the ADC inputs of the Maxim portfolio of the Teridian energy metering ICs. Proper selection will avoid side effects such as crosstalk, inaccuracy over temperature, or inaccuracy due to additional phase shift over load currents.

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Related Parts		
71M6531D	Energy Meter ICs	Free Samples
71M6531F	Energy Meter ICs	Free Samples
71M6532D	Energy Meter ICs	Free Samples
71M6532F	Energy Meter ICs	Free Samples

71M6533	Energy Meter ICs	Free Samples
71M6533H	Energy Meter ICs	Free Samples
71M6534	Energy Meter ICs	Free Samples
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