# SC453
# Portable, VID Programmed Single Phase Power Supply Controller

**POWER MANAGEMENT**

## Description

The SC453 IC is a single chip high-performance Hysteretic PWM controller. With its integrated SmartDrive™ it powers advanced graphics and core processors. It provides sleep mode and boot voltage support. Automatic power-save is present to prevent negative current flow in the low-side FET during light loading conditions saving even more power. The high side driver initially turns on with a weak drive to reduce ringing, EMI, and capacitive turn-on of the low side.

A 6-bit DAC (accurate to 0.85%) sets the output voltage reference and implements the 0.700V to 1.708V range required by the processor. The hysteretic converter uses a comparator without an error amplifier to provide fast transient response while avoiding the stability issues inherent to classical PWM controllers. The DAC is externally slew rate limited to minimize transient currents and audible noise.

The SC453 operates from a 5V supply and also features soft-start, an open-drain power good signal with $V_{CORE}$ transition blanking, and an enable input. Programmable current limiting shuts down the SC453 after 32 current limit pulses.

## Features

- High Speed Hysteretic Controller
- Single Phase Operation
- Selectable Analog or VID Controlled Sleep Setting
- 6 Bit VID programmable Output
- Integrated Drivers with SmartDrive™
- Programmable Soft-Start
- Programmable Boot Voltage
- Programmable Sleep Voltage with Sleep Mode
- Under-Voltage Lockout on $V_{CCA}$ and $V_5$
- Over-voltage Protection on $V_{CORE}$
- Current Limit Protection on $V_{CORE}$
- Thermal Protection
- Power Good Flag with Blanking During $V_{CORE}$ Changes
- Automatic Power Save at Light Load
- Package Types — TSSOP-28, MLPQ-32

## Applications

- Low Power Notebook and Laptop Computers
- Embedded Applications

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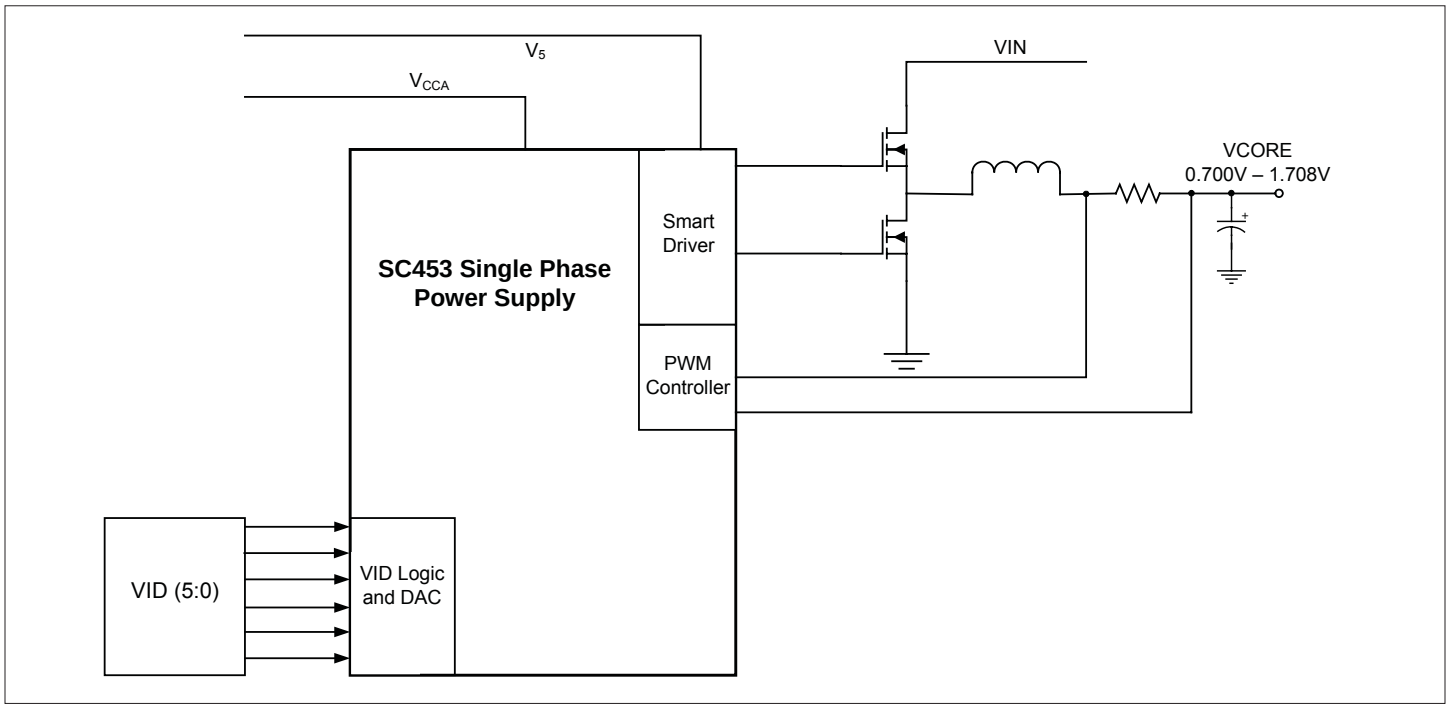
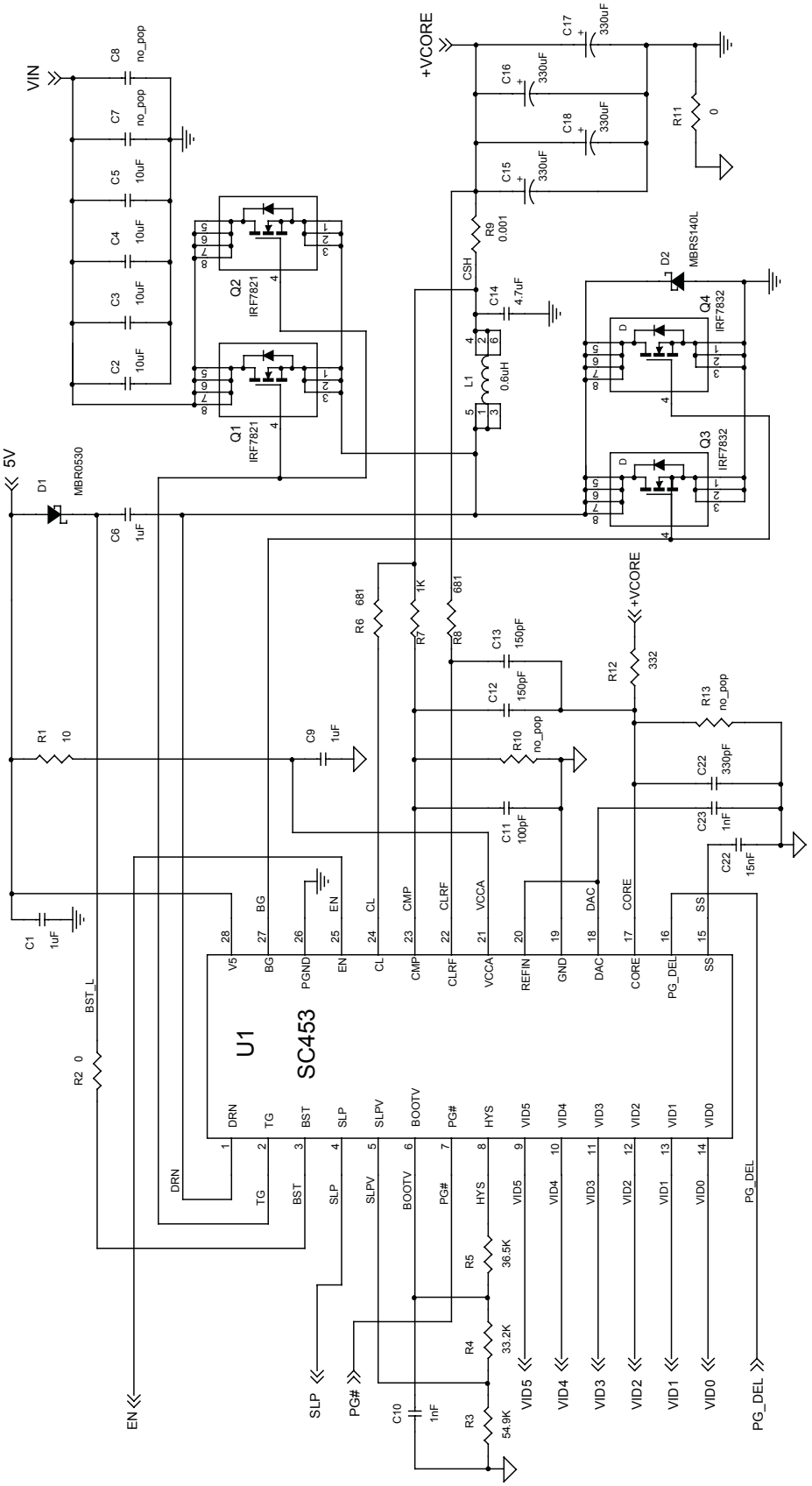
## Typical Application Circuit



## Reference Design



## Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

| Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Supply Voltages | $V_{CCA,}$ $V_5$ | | -0.3 | 7 | V |
| Input and Output Voltages | $V_{SLPV,}$ $V_{SLP}$, $V_{VID\ [0..5]}$, $V_{DAC}$, $V_{REFIN}$, $V_{CMP}$, $V_{HYS}$, $V_{CORE}$, $V_{CL}$, $V_{CLRF}$, $V_{PG\#}$, $V_{BOOTV}$, $V_{SS}$, $V_{BG}$, $V_{CLSET}$ | to GND | -0.3 | $V_{CCA}$ +0.3 | V |
| EN to GND | $V_{EN}$ | | -0.3 | 7 | V |
| BST to PGND | | Static<br>Transient < 100ns | -0.3 | 36<br>40 | V<br>V |
| BST to DRN | | | -0.3 | 7 | V |
| DRN to PGND | | Static<br>Transient < 100ns<br>Transient < 10ns | -2<br>-5<br>-7.5 | 30<br>34<br>34 | V<br>V<br>V |
| TG to BST | | | -0.3 | BST +0.3 | V |
| PGND to GND | | | -0.3 | 0.3 | V |
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | TSSOP-28(1) | | 70 | °C/W |
| | | MLPQ-32 | | 26 | |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | TSSOP-28 | | 20 | °C/W |
| Lead Temperature (Soldering) 10s | $T_{LEAD}$ | TSSOP-28 | | 300 | °C |
| Peak IR Reflow Temperature 10 - 40s | $T_{PKG}$ | TSSOP-28 | | 260 | °C |
| | | MLPQ-32 | | 260 | |

NOTES:
(1) Calculated from package in still air, mounted to 3 x 4.5(in), 4 layer FR4 PCB.
(2) Tested according to JEDEC standard JESD22-A114.

## Electrical Characteristics

Unless otherwise specified: $V_{IN}$ = 15V, $V_{CCA}$ = 5V, and V5 = 5V.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply ($V_{IN}$, $V_{CCA}$, $V_5$)** | | | | | | |
| $V_{IN}$ Supply Voltage Range | $V_{IN}$ | | 3.0 | | 25 | V |
| $V_5$ Supply Voltage Range | $V_5$ | | 4.3 | 5.0 | 6.0 | V |
| $V_{CCA}$ Voltage Range | $V_{CCA}$ | | 4.5 | 5.0 | 6.0 | V |

## Electrical Characteristics (Cont.)

| Parameter | Symbol | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ Quiescent Current | $I_{CCQ}$ | EN is low | | | | 10 | µA |
| | | EN is high, $V_{CCA}$ or $V_5$ in UVLO | | | 400 | | µA |
| $V_{CCA}$ Operating Current | $I_{CC}$ | | | | 5 | | mA |
| **Under-Voltage Lockout Circuits ($V_{CCA}$, $V_5$)** | | | | | | | |
| Threshold ($V_{CCA}$ falling) | $V_{HCCA}$ | | | 3.47 | 3.70 | 3.93 | V |
| $V_{CCA}$ Hysteresis | $V_{HYST\ CCA}$ | | | | 190 | | mV |
| Threshold ($V_5$ falling) | $V_{HV5}$ | | | 3.85 | 4.00 | 4.25 | V |
| $V_5$ Hysteresis | $V_{HYST\ V5}$ | | | | 210 | | mV |
| **Fixed Over-Voltage Protection (CORE)** | | | | | | | |
| Threshold (CORE Rising) | $V_{TH\ CORE\ FIXED}$ | Not dependent on DAC setting | | 1.95 | 2.00 | 2.05 | V |
| **Enable Input (EN)** | | | | | | | |
| Input High | $V_{iH\ (EN)}$ | | | 2 | | | V |
| Input Low | $V_{iL\ (EN)}$ | | | | | 0.8 | V |
| **$V_{CORE}$ Power Good Generator (PG_DEL, PG#)** | | | | | | | |
| Core Input Threshold | $V_{TH\ CORE}$ | $V_{DAC}$ = 0.6 - 1.75V<br>Note: during UVLO, the output level of this signal is undefined | Upper Threshold | 1.1× $V_{DAC}$ | | 1.15× $V_{DAC}$ | V |
| | | | Lower Threshold | 0.86× $V_{DAC}$ | | 0.9× $V_{DAC}$ | |
| | | | Hysteresis | | 1 | | % |
| PG# Output Voltage | $V_{PG\#}$ | Pulled up with external 680Ω resistor to $V_{PULL-UP}$ | $V_{CORE}$ = $V_{DAC}$ | | | 0.4 | V |
| | | | Either $V_{CORE}$ < 0.88*$V_{DAC}$, or, $V_{CORE}$ > 1.12*$V_{DAC}$ | 0.95× $V_{PULL-UP}$ | | | |
| | | | $V_{CCA}$ or $V_5$ in UVLO | 0.95× $V_{PULL-UP}$ | | | |
| PG_DEL Output Voltage | $V_{PG_DEL}$ | $V_{CORE}$ = $V_{DAC}$, PG_DEL pulled-up with external 680Ω resistor to $V_{PULL-UP}$ | | 0.95× $V_{PULL-UP}$ | | | V |
| | | $V_{CORE}$ < 0.88*$V_{DAC}$ or $V_{CORE}$ > 1.12*$V_{DAC}$ | | | | 0.4 | |
| | | $V_{CCA}$ or $V_5$ in UVLO | | | | 0.8 | |
| PG_DEL Delay (at start-up) | | Measured from PG# assertion | | | 1007 | | Clocks |

## Electrical Characteristics (Cont.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Soft-Start & DAC Slew (SS)** | | | | | | |
| Soft-Start/DAC Slew Current<br><br>Note:<br>SS cap is not discharged until EN goes low or UVLO cuts in. To enable the converter, SS has to drop below $V_{SS_EN}$. | $I_{SS}$ | Discharge (sink) Current | 5 | 10 | | mA |
| | | Soft-Start transition $0 < T_A < 85°C$, $-40 < T_A < 85° C$ | 7.5 | 10.5 | 16 | µA |
| | | Sleep Exit, $0 < T_A < 85°C$ | 204 | 256 | 310 | |
| | | Sleep Exit, $-40 < T_A < 85°C$ | 180 | 240 | 320 | |
| | | VID Transition, $0 < T_A < 85°C$ | 102 | 128 | 155 | |
| | | VID Transition, $-40 < T_A < 85°C$ | 90 | 120 | 160 | |
| Soft-Start Enable Threshold | $V_{SS_EN}$ | | | 40 | 100 | mV |
| **DAC (VID [5:0])** | | | | | | |
| VID Input Threshold | $V_{iH_VID}$ | | 0.55 | | | V |
| | $V_{iL_VID}$ | | | | 0.45 | |
| DAC Output Voltage Accuracy | $V_{DAC_ERR}$ | $0° < T_A < 85°C$, VID [5:0] = 000000 - 111111(1.708V - 0.812V) | -0.85 | | +0.85 | % |
| | | $-25°C < T_A < 85°C$, VID [5:0] = 000000 - 111111 (1.708V - 0.700V) | -2.0 | | +2.0 | % |
| **Boot Voltage (BOOTV)** | | | | | | |
| Input Voltage Offset | $V_{BOOTV}$-$V_{DAC}$ | BOOTV = 1.2V | | | \|±3\| | % |
| BOOT Delay Time(1) | TBOOT | | 10 | 35 | | µs |
| **Sleep (SLP, SLPV)** | | | | | | |
| Input Voltage Offset | $V_{SLPV}$ - $V_{DAC}$ | SLPV = 0.8V | | | \|±3\| | % |
| SLP Logic Threshold | $V_{iH_SLP}$ | | 2 | | | V |
| | $V_{iL_SLP}$ | | | | 0.8 | |
| **CORE Comparator (CMP, REFIN, HYS)** | | | | | | |
| Input Bias Current | $I_{REFIN}$ | $V_{REFIN}$ = 1.3V | | | \|±2\| | µA |
| Input Voltage Offset | $V_{CMP}$ - $V_{REFIN}$ | | | \|±1.5\| | \|±3\| | mV |

## Electrical Characteristics (Cont.)

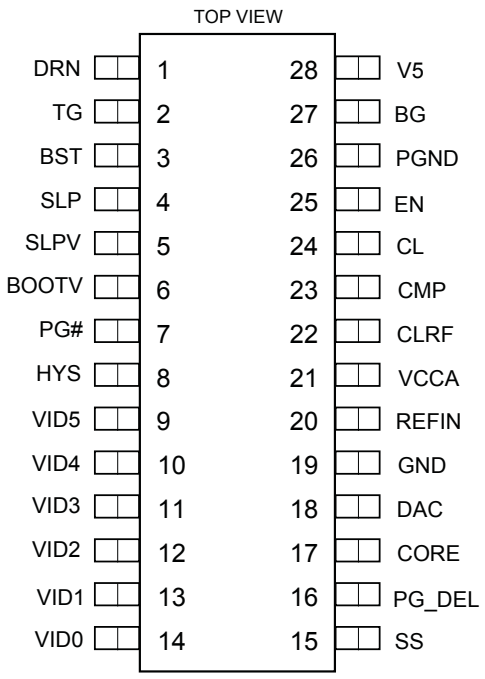
| Parameter | Symbol | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **CORE Comparator (CMP, REFIN, HYS) (Cont.)** | | | | | | | |
| Hysteresis Setting Current SLP = low | $I_{CMP}$ | $R_{HYS}$ = 17K | $V_{CMP} < V_{REFIN}$ | -110 | -100 | -90 | µA |
| | | | $V_{CMP} > V_{REFIN}$ | 90 | 100 | 110 | |
| | | $R_{HYS}$ = 170K | $V_{CMP} < V_{REFIN}$ | -7 | -10 | -13 | |
| | | | $V_{CMP} > V_{REFIN}$ | 7 | 10 | 13 | |
| Hysteresis Setting Current SLP = high | $I_{SLP_}I_{CMP}$ | $R_{HYS}$ = 17K | $V_{CMP} < V_{REFIN}$ | -83 | -73 | -63 | µA |
| | | | $V_{CMP} > V_{REFIN}$ | 63 | 73 | 83 | |
| **Current Limit Comparator (CL, CLRF, HYS)** | | | | | | | |
| Input Bias Current | $I_{CL}$ | $V_{CL1,2}$ = 1.3V | | | | \|±2\| | µA |
| Input Voltage Offset | $V_{CL}$-$V_{CLRF}$ | | | | \|±3\| | \|±5\| | mV |
| Current Limit Setting Current SLP = low | $I_{CLRF}$ | $R_{HYS}$ = 17K | $V_{CL} < V_{CLRF}$ | 150 | 200 | 250 | µA |
| | | | $V_{CL} > V_{CLRF}$ | 250 | 300 | 350 | |
| | | $R_{HYS}$ = 170K | $V_{CL} < V_{CLRF}$ | 15 | 20 | 25 | |
| | | | $V_{CL} > V_{CLRF}$ | 25 | 30 | 35 | |
| Current Limit Setting Current SLP = high | $I_{SLP_CLRF}$ | $R_{HYS}$ = 17K | $V_{CL} < V_{CLRF}$ | 120 | 150 | 180 | µA |
| | | | $V_{CL} > V_{CLRF}$ | 195 | 230 | 265 | |
| **Zero-Crossing (Powersave) Comparators (CL, CORE)** | | | | | | | |
| Offset | $V_{CL}$-$V_{CORE}$ | | | | | \|±5\| | mV |
| **High Side Driver (TG)** | | | | | | | |
| Peak Output Current(1) | $I_{pkh}$ | | | | 1.5 | | A |
| Output Resistance | $R_{SRC_TG}$ | I = 100mA, $V_{BST}$-$V_{DRN}$ = 5V | $V_{DRN}$ < 1V | | 4.2 | | Ω |
| | | | $V_{DRN}$ > 1V | | 1 | 4 | |
| | $R_{SINK_TG}$ | I = 100mA, $V_{BST}$-$V_{DRN}$ = 5V | | | 0.7 | 1.4 | Ω |
| Rise Time(1) | $tr_{TG}$ | $C_{TG}$ = 3nF, $V_{BST}$-$V_{DRN}$ = 5V | | | 60 | | ns |
| Fall Time(1) | $tf_{TG}$ | $C_{TG}$ = 3nF, $V_{BST}$-$V_{DRN}$ = 5V | | | 36 | | ns |

## Electrical Characteristics (Cont.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **High Side Driver (Cont.)** | | | | | | |
| Propagation Delay TG Going High(1) | $tpdh_{TG}$ | CMP crossing REFIN to 10% point of TG, $C_{TG}$ = 3nF, BG = 0V | | 45 | | ns |
| Propagation Delay TG Going Low(1) | $tpdl_{TG}$ | CMP crossing REFIN to 90% point of TG, $C_{TG}$ = 3nF | | 45 | | ns |
| Shoot-thru Protection Delay Time(1) | tspd | | 21 | 30 | 39 | ns |
| **Low Side Driver (BG)** | | | | | | |
| Peak Output Current(1) | $I_{pkl}$ | | | 3 | | A |
| Output Resistance | $R_{SRC_BG}$ | I = 100mA, V5 = 5V | | 1.0 | 2.6 | Ω |
| | $R_{SINK_BG}$ | | | 0.5 | 1.2 | |
| Rise Time(1) | $tr_{BG}$ | $C_{BG}$ = 3nF, V5 = 5V | | 25 | | ns |
| Fall Time(1) | $tf_{BG}$ | $C_{TG}$ = 3nF, V = 5V | | 15 | | ns |
| Propagation Delay TG Going High(1) | $tpdh_{BG}$ | CMP crossing REFIN to 10% point of BG, $C_{BG}$ = 3nF, DRN = 0V | | 35 | | ns |
| Propagation Delay TG Going Low(1) | $tpdl_{BG}$ | CMP crossing REFIN to 90% point of TG, $C_{TG}$ = 3nF, DRN = 0V | | 35 | | ns |

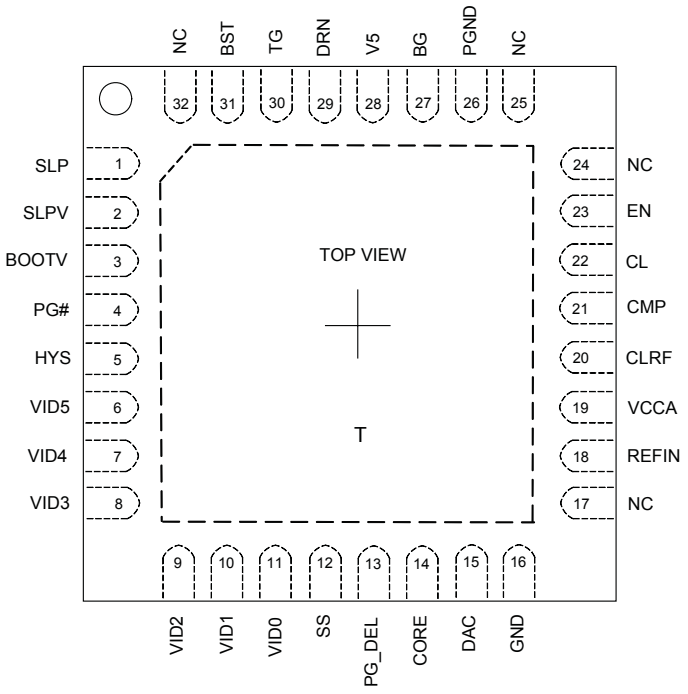
Notes:
1) Guaranteed by design.

## Pin Configurations




**TSSOP-28 Package**

**$\theta_{JA}$ = 70°C/W**




**MLPQ-32 Package**

**$\theta_{JA}$ = 29°C/W**

## Ordering Information

| Device | Package |
|---|---|
| SC453TSTRT(1)(2)(3) | TSSOP-28 |
| SC453EVB | EVALUATION BOARD |
| SC453MLTRT(1)(2)(4) | MLPQ-32 |

Notes:
1. This device is ESD sensitive. Use of standard ESD handling precautions is required.
2. Lead-free package only. Qualified to support maximum IR reflow temperature of 260°C for 30 seconds.
3. Available in tape and reel only. A reel contains 2500 devices.
4. Available in tape and reel only. A reel contains 3000 devices.

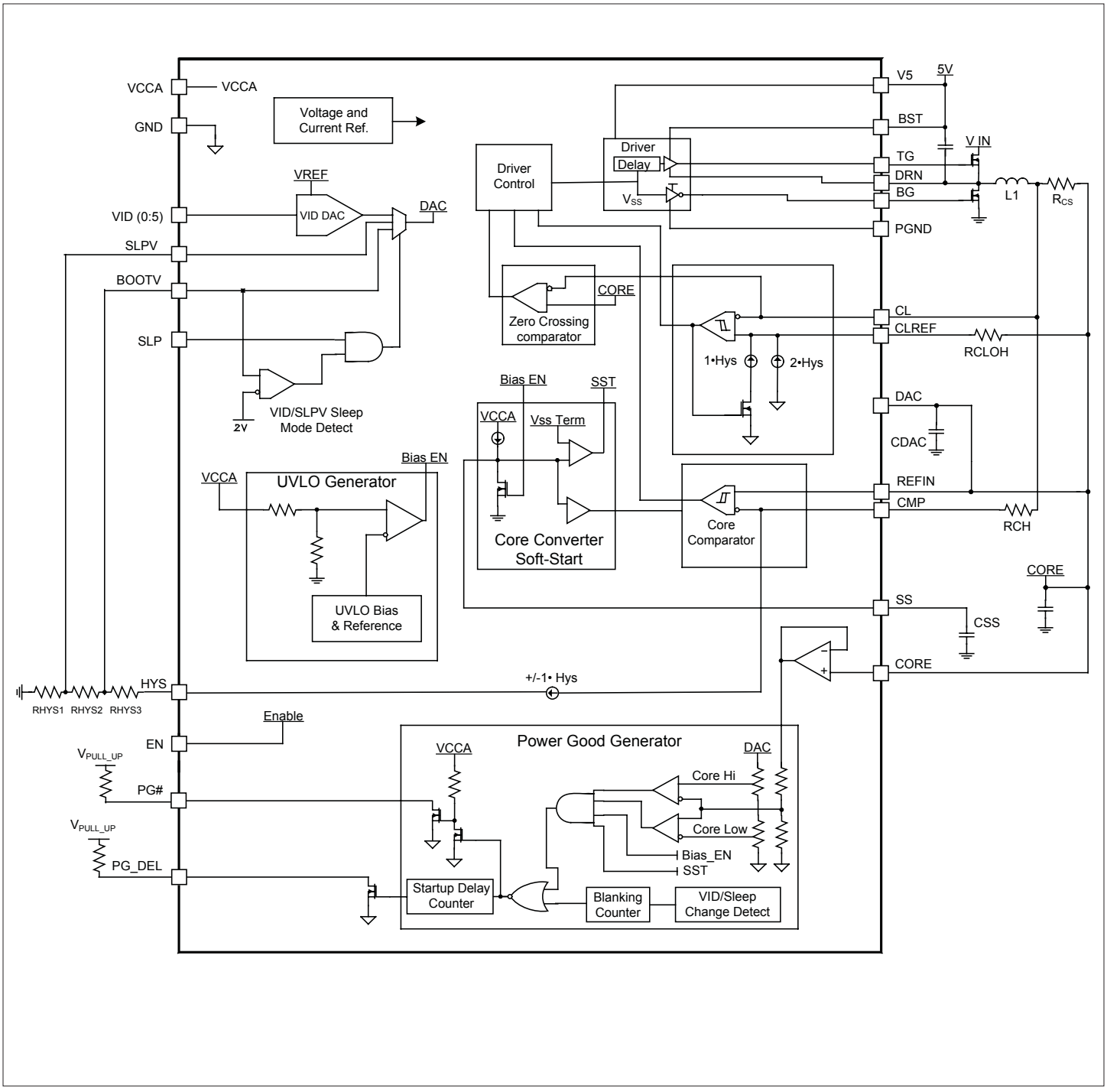
## Pin Descriptions

| Pin# TSSOP-28 | Pin# MLPQ-32 | Pin Name | Pin Function |
|---|---|---|---|
| 1 | 29 | DRN | This pin connects to the junction of the switching and synchronous MOSFETs. |
| 2 | 30 | TG | Gate drive for the switching (high-side) MOSFET. |
| 3 | 31 | BST | Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET gate drive. |
| 4 | 1 | SLP | Sleep logic input signal. |
| 5 | 2 | SLPV | Connect this pin to $V_{CCA}$ to select VID Sleep Mode. Otherwise, SLPV Sleep Mode is selected and the voltage on this pin sets the DAC output during sleep. |
| 6 | 3 | BOOTV | The voltage on this pin sets the Boot-Up voltage. |
| 7 | 4 | PG# | Start clock indicator open drain output — Active low |
| 8 | 5 | HYS | Core Comparator Hysteresis — Connect to ground through an external resistor. Hysteresis current is established by the internal $V_{REF}$ voltage, 1.7V, divided by the total HYS resistance ($R_{HYS}$). |
| 9 | 6 | VID5 | VID input, most significant bit of the voltage programming DAC input |
| 10 | 7 | VID4 | VID input |
| 11 | 8 | VID3 | VID input |
| 12 | 9 | VID2 | VID input |
| 13 | 10 | VID1 | VID input |
| 14 | 11 | VID0 | VID input, least significant bit of the voltage programming DAC input |
| 15 | 12 | SS | Soft-start — an external cap defines the soft-start ramp. |
| 16 | 13 | PG_DEL | Delayed Power Good — open drain output. After the $V_{CORE}$ output is within ± 14% of the VID_DAC setting, and the $t_{CPU_PWRGD}$ period has terminated, this internal pull-down MOSFET opens and the pin is pulled high by an external resistor. |
| 17 | 14 | CORE | Feedback input for the $V_{CORE}$ output. A small RC filter should be used to filter out high frequency noise to prevent false or faulty trip conditions. |
| 18 | 15 | DAC | Main controller digital-to-analog output |
| 19 | 16 | GND | Analog ground |
| 20 | 18 | REFIN | Core Comparator reference input pin — connect to DAC. |
| 21 | 19 | VCCA | 5V supply for precision analog circuitry |
| 22 | 20 | CLRF | Current limit reference input |
| 23 | 21 | CMP | Core Comparator input |
| 24 | 22 | CL | Current limit input |

## Pin Descriptions (Cont.)

| Pin# TSSOP-28 | Pin# MLPQ-32 | Pin Name | Pin Function |
|---|---|---|---|
| 25 | 23 | EN | Enable input — active high |
| 26 | 26 | PGND | Power ground — connect to the low-side MOSFET power ground |
| 27 | 27 | BG | Gate drive output for the synchronous (low-side) MOSFET |
| 28 | 28 | V5 | 5V supply input for the gate drive outputs — a 1µF minimum capacitor should be connected from V5 to GND |
| — | 17 | NC | No connection |
| — | 24 | NC | No connection |
| — | 25 | NC | No connection |
| — | 32 | NC | No connection |
| — | T | T | Thermal pad — No internal connection. Connect to GND. |

## Block Diagram



## Applications Information (Cont.)

SUPPLY, BIAS, UVLO, POWER GOOD GENERATOR

### Supply

The chip is optimized to operate from a 5V ± 5% rail but also designed to work up to 6V maximum supply voltage.

### Under-Voltage Lock-Out Circuit

The Under-Voltage Lock-Out (UVLO) circuitry monitors both the VCCA and V5 voltage levels. The SC453 is in UVLO mode while either supply has not ramped above the upper threshold or has dropped below the lower threshold. During UVLO, the external FETs are held off.

### Over-Voltage Protection

If the CORE voltage is greater than +14% of the DAC (i.e., out of the power good window), the SC453 will latch off and hold the low-side driver on permanently. Either of the 5V supplies or the EN pin must be cycled to clear the latch. The latch is disabled during soft-start and VID/Sleep transitions. For safety, the latch is enabled if the CORE voltage exceeds 2V even during VID/Sleep transitions.

### Thermal Shutdown

The device will be disabled and latched off when the internal junction temperature reaches approximately 160°C. Either the power or EN must be recycled to clear the latch.

### Band Gap Reference

A ± 0.85% precision band gap reference acts as the internal reference voltage standard of the chip, which all critical biasing voltages and currents are derived from. All references to $V_{REF}$ in the equations to follow will assume $V_{REF}$ = 1.7V.

### Precision DAC

This 6-bit digital-to-analog converter (DAC) serves as the programmable reference source of the core comparator. Programming is accomplished by logic voltage levels applied to the DAC inputs. The VID code vs. the DAC output is shown in the following table. The accuracy of the VID /DAC is maintained on the same level as the band gap reference.

| VID | | | | | | $V_{DAC}$ | VID | | | | | | $V_{DAC}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | 0 | V | 5 | 4 | 3 | 2 | 1 | 0 | V |
| 0 | 0 | 0 | 0 | 0 | 0 | 1.708 | 1 | 0 | 0 | 0 | 0 | 0 | 1.196 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.692 | 1 | 0 | 0 | 0 | 0 | 1 | 1.180 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.676 | 1 | 0 | 0 | 0 | 1 | 0 | 1.164 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.660 | 1 | 0 | 0 | 0 | 1 | 1 | 1.148 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.644 | 1 | 0 | 0 | 1 | 0 | 0 | 1.132 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.628 | 1 | 0 | 0 | 1 | 0 | 1 | 1.116 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.612 | 1 | 0 | 0 | 1 | 1 | 0 | 1.100 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.596 | 1 | 0 | 0 | 1 | 1 | 1 | 1.084 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1.580 | 1 | 0 | 1 | 0 | 0 | 0 | 1.068 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1.564 | 1 | 0 | 1 | 0 | 0 | 1 | 1.052 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1.548 | 1 | 0 | 1 | 0 | 1 | 0 | 1.036 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1.532 | 1 | 0 | 1 | 0 | 1 | 1 | 1.020 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1.516 | 1 | 0 | 1 | 1 | 0 | 0 | 1.004 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1.500 | 1 | 0 | 1 | 1 | 0 | 1 | 0.988 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1.484 | 1 | 0 | 1 | 1 | 1 | 0 | 0.972 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1.468 | 1 | 0 | 1 | 1 | 1 | 1 | 0.956 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1.452 | 1 | 1 | 0 | 0 | 0 | 0 | 0.940 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1.436 | 1 | 1 | 0 | 0 | 0 | 1 | 0.924 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1.420 | 1 | 1 | 0 | 0 | 1 | 0 | 0.908 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1.404 | 1 | 1 | 0 | 0 | 1 | 1 | 0.892 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1.388 | 1 | 1 | 0 | 1 | 0 | 0 | 0.876 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.372 | 1 | 1 | 0 | 1 | 0 | 1 | 0.860 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.356 | 1 | 1 | 0 | 1 | 1 | 0 | 0.844 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1.340 | 1 | 1 | 0 | 1 | 1 | 1 | 0.828 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1.324 | 1 | 1 | 1 | 0 | 0 | 0 | 0.812 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1.308 | 1 | 1 | 1 | 0 | 0 | 1 | 0.796 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1.292 | 1 | 1 | 1 | 0 | 1 | 0 | 0.780 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1.276 | 1 | 1 | 1 | 0 | 1 | 1 | 0.764 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1.260 | 1 | 1 | 1 | 1 | 0 | 0 | 0.748 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1.244 | 1 | 1 | 1 | 1 | 0 | 1 | 0.732 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1.228 | 1 | 1 | 1 | 1 | 1 | 0 | 0.716 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1.212 | 1 | 1 | 1 | 1 | 1 | 1 | 0.700 |

## Applications Information (Cont.)

CORE CONVERTER CONTROLLER

Core Comparator

This is an ultra-fast hysteretic comparator with a typical propagation delay of 20ns for 20mV overdrive. Hysteresis is generated by the current set at the HYS pin impressed upon an external resistor connected to the CMP pin.

Current Limit Comparator

The Current Limit Comparator compares the voltage between the CL and CLREF pins. The CL pin monitors the inductor current using the voltage drop across a resistor connected in series with the inductor. The CLREF voltage determines the upper limit for the Current Limit Comparator. The upper limit is equal to the (3 x HYS) current multiplied by the resistance connected to the CLREF pin.

A current limit condition occurs when the CL voltage exceeds the CLREF voltage, at which point the high side FETs are turned off. The high side FETs will not be enabled again until the inductor current drops below the lower current limit threshold. The upper and lower current limit thresholds are programmed by the voltage drop impressed upon an external resistor connected to the CLRF pin. The voltage drop is equal to the HYS current multiplied by the

Current Limit Latch

If the CORE voltage goes lower than 14% below the VID (i.e., out of the power good window), then sustained current limiting (32 current limit pulses) will cause the part to permanently latch off. The latch is inhibited during soft-start.

Core Converter Soft-Start Timer

This block controls the start-up ramp time of the CORE voltage up to the boot voltage. The primary purpose is to reduce the initial in-rush current on the core input voltage (battery) rail.

Cycle-by-Cycle Power-Save

A zero crossing comparator detects when the currents through the external sense resistor reduces to zero. When the current in the external sense resistor reaches zero, the bottom FET is latched off. The latch is reset when the controller decides to switch on the top FET. This prevents excessive switching at light loads and hence saves switching power losses.

DAC Slew Control

The output of the DAC will slew at a rate defined by the current in the SS pin and the capacitor applied externally to the SS pin. The slew rate (charge current) applied depends on which mode (soft-start, VID or sleep transition) is in effect. A 1nF capacitor is recommended for the DAC pin.

Blanking During VID Changes

On any VID change or Sleep change, the PG# and PG_DEL signals are blanked for 62 switching cycles to prevent glitching during the transition.

Sleep Function and SLPV/VID Sleep Mode

By default, the controller is in SLPV controlled sleep mode. In this mode, the voltage applied to the SLPV pin appears at the DAC output when SLP is asserted high. This mode is selected by connecting the SLPV to a resistor divider from the HYS pin,

VID sleep mode is selected by connecting the SLPV pin to VCCA during startup. In this mode, the DAC output continues to be set by the VID inputs even when SLP is asserted high.

During sleep mode, the hysteresis current used for PWM switching and for current limit are reduced to 70% of their nominal values.

## Applications Information (Cont.)

PG# Output

This is an open-drain output and should be pulled up externally. This signal is asserted (pulled low) by the SC453 whenever the core voltage is within ±14% of the VID programmed value. If the chip is disabled by the EN input or by 5V UVLO, then the PG# pin is de-asserted. During start-up PG# remains de-asserted until the core voltage has reached the defined boot voltage and remains there for the BOOT period (10µS minimum). This signal is forced low (asserted) during VID and sleep transitions.

PG_DEL Output

This signal is delayed a minimum of 3mS from first assertion of the PG# signal. This is an open drain output and should be pulled up externally. This signal is asserted (open drain) by the SC453 whenever the core is within ±14% of the VID programmed value. If the chip is disabled or enabled in UVLO, then PG_DEL is de-asserted. The signal is forced high (open drain) during VID and sleep transitions.

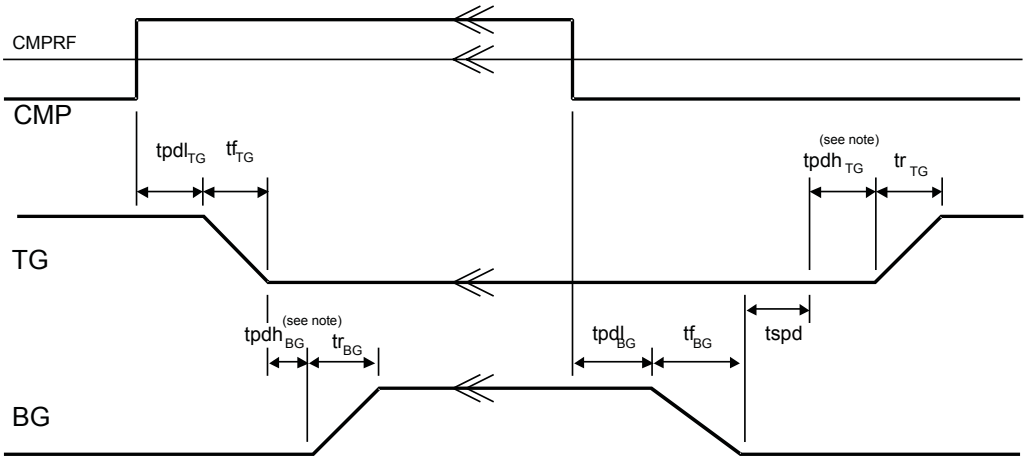
Start-Up and Sequencing

On start-up, $V_{CORE}$ ramps to the boot voltage set by the BOOTV pin irrespective of the status of the VID pins. After a minimum of 10µs, PG# asserts, and $V_{CORE}$ will then respond to the VID inputs. The controller will then count 1007 switching cycles before asserting PG_DEL.

Summary of Fault Conditions

| Protection Mode | Latched? | When Active | Driver Status | SS Pin Status |
|---|---|---|---|---|
| Supply UVLO (VCCA, V5) | No | Always | All low | Low |
| 32 Cycle Current Limit | Yes | SS has terminated and PGDEL is low | TG low | Sawtooth |
| 114% $V_{CORE}$ OVP | Yes | SS has terminated and PGDEL is low | BG high | High |
| 2.0$V_{CORE}$ OVP | Yes | Always | BG high | High |
| Thermal Shutdown | Yes | Always | BG, TG low | High |

Driver Timing Diagram




NOTE: Subtract 20ns (typical) for the core comparator delay since this parameter is specified from a CMP edge.

## Applications Information (Cont.)

DESIGN PROCEDURE

Step 1 — Define Constants

| | |
|---|---|
| $V_{INMAX} := 20\,V$ | Maximum input voltage |
| $V_{INMIN} := 8\,V$ | Minimum input voltage |
| $I_{MAX_FL} := 20\,A$ | Maximum load current, highest output voltage |
| $I_{LKGMAX} := 5\,A$ | Leakage current, highest output voltage |
| $V_{MAX_NL} := 1.212\ V$ | The highest $V_{CORE}$ voltage |
| $V_{MIN_NL} := 0.956 \cdot V$ | The lowest $V_{CORE}$ voltage |
| $V_{REF} := 1.7\,V$ | SC453 Internal reference voltage |
| $C_{OUT} := 330 \cdot \mu F$ | Output capacitance per cap |
| $R_{ESR} := 6\,m \cdot \Omega$ | ESR per cap |
| $R_{CS} := 1\,m \cdot \Omega$ | Current sense resistor |
| $R_{CU} := 0.5\ m \cdot \Omega$ | Parasitic resistance from the current sense resistor to the processor |
| $V_{POS_TRANS} := 50\ mV$ | Voltage droop allowed for a low current to high current transient |
| $V_{NEG_TRANS} := 50\ mV$ | Voltage rise allowed for a high current to low current transient |
| $V_{RIPPLE} := 20\,m\,V$ | Desired maximum output ripple |

Step 2 — Output Inductor and Capacitor Selection

The SC453 has passive droop. The voltage at full load is less than the DAC voltage by the voltage drop across the current sense resistor and any PCB copper losses from the sense resistor to the processor socket. The steady-state voltage at full load is as follows.

$$V_{MAX_FL} := V_{MAX_NL} - (R_{CS} + R_{CU}) I_{MAX_FL}$$

$$V_{MAX_FL} = 1.182\ V$$

Output capacitance and ESR values are a function of transient requirements and output inductor value. Figure 1 illustrates the response of a hysteretic converter to a positive transient. In a hysteretic converter with passive droop, like the SC453, two conditions determine if you meet the positive transient requirements.

$$ESR \le \frac{V_{POS_TRANS}}{(I_{MAX_FL} - I_{LKGMAX})}$$

$$V_{NEG_TRANS} \ge deltaV(C_{OUT})$$

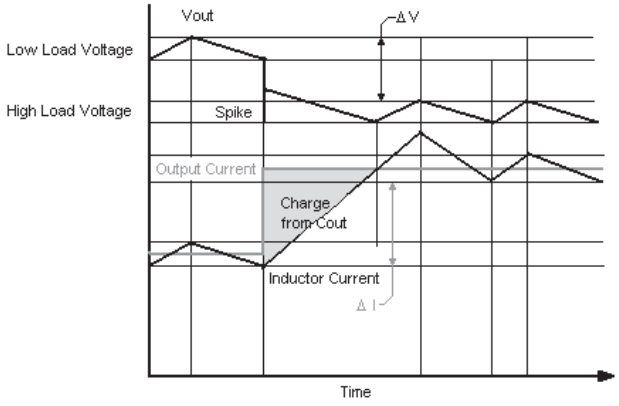



Figure 1 — Hysteretic Converter Response to a Positive Transient

The first condition is easy to see; if the ESR is too high, the instantaneous I•ESR drop seen at the output will be larger than the allowed limit.

## Applications Information (Cont.)

The second condition occurs later after the initial transient. Due to the fast response of the hysteretic converters, less then < 100ns, the capacitor voltage does not droop very far before the inductor current starts ramping up. Once the inductor current starts to rise, the I•ESR comp onent of the capacitor voltage start to move upward. At the same time, the capacitive discharging causes the capacitor voltage to move downward. The lowest output voltage is reached when the inductor current reaches the load current (note the shaded area on the graph). If this voltage is higher than the lower limit (VPOS_TRANS), then the transient response passes.

Since the highest output voltage has the most severe requirements, any other modes are satisfied by a design optimized for the highest output voltage.

$$ESR_{MAX} := \frac{V_{POS_TRANS}}{(I_{MAX_FL} - I_{LKGMAX})}$$

$$ESR_{MAX} = 3.333 \times 10^{-3}\ \Omega$$

For the second condition, the inductor value is determined, which is a function of the highest desired switching frequency. The maximum frequency occurs at the highest input voltage. As a reasonable compromise between efficiency and component size, a maximum switching frequency of 350kHz is desired.

$$F_S := 350\ K \cdot Hz$$

$$d_{MIN} := \frac{V_{MAX_NL}}{V_{INMAX}}$$

$$L_{MIN} := d_{MIN} \cdot \frac{(V_{INMAX} - V_{MAX_NL})(ESR_{MAX} + R_{CS})}{F_S \cdot V_{RIPPLE} \cdot \left(\frac{ESR_{MAX} + R_{CS}}{ESR_{MAX}}\right)}$$

$$L_{MIN} = 5.422 \times 10^{-7}\ H$$

The design is based on the following three factors: 1) minimum inductance requirement; 2) low DCR; 3) height and package size consideration. The design choice is made based upon the requirement of the converter design, including minimum inductance, minimum saturation current, efficiency, foot area, maximum allowable height, and device availability. In the current demo board design,

$$L_1 := 0.60 \cdot \mu H$$

This value of inductance is required up to maximum load. Inductors with a swinging choke characteristic, where the zero current value of inductance is much less than the full load current inductance can be used, as long as the above restriction is met. Then, the worst-case (low input voltage) response time (the time for the current to reach the new transient value) is:

$$dT := \frac{L_1 \cdot (I_{MAX_FL} - I_{LKGMAX})}{V_{INMIN} - V_{MAX_NL}}$$

$$dT = 1.326 \times 10^{-6}\ s$$

Add 100ns for the typical propagation delay from a change at the output to the MOSFET switch turning on in reaction. Since the shaded area is, the total charge taken out of the capacitor is $\Delta Q = C / dV = (dI/dt)/2$. This is calculated using the following equation.

$$C_{MINP} := \frac{(I_{MAX_FL} - I_{LKGMAX})(dT + 1 \cdot 10^{-7} \cdot sec)}{V_{POS_TRANS}}$$

$$C_{MINP} = 4.278 \times 10^{-4}\ F$$

This condition applies only to the positive transient.

## Applications Information (Cont.)

LOAD RELEASE

The worst-case for the transient load release is when the hysteresis has just reached the maximum, (i.e. the high-side switch has just turned of). At this time the inductor has reached its peak current as calculated below.

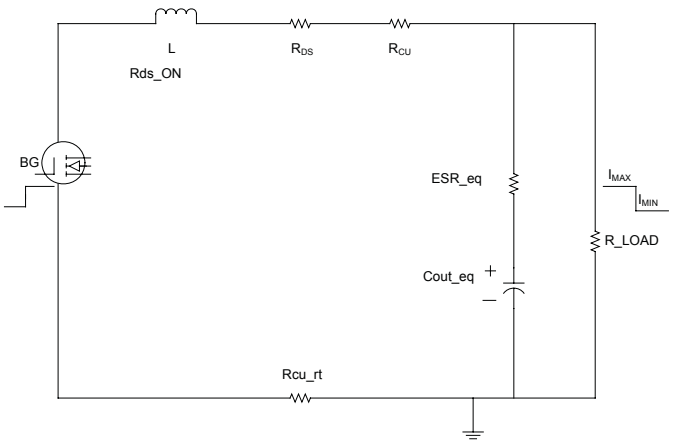
$$I_{RIPPLE} := \frac{(V_{INMAX} - V_{MAX_F}}{L_1 \cdot F_S}$$

$$_{RIPPLE} = 6.01 \quad A$$

$$I_{t0} := I_{MA\rangle}$$

$$I_{t0} = 23.005 \quad A$$

The load is stepping from high to low.




Immediately after the load steps down from $I_{MAX}$ to $I_{MIN}$, the high side FET is turned off, and the bottom FET is turned on after the dead time. It is assumed for the worst-case condition that at t = 0, the inductor current is initially at its maximum;. After t = 0, the inductor discharges at a rate equal to $V_{FL}$ / L (ignoring secondary order effects such as Rds_on drop, current sense resistor and copper losses). The energy released from the output inductor during load step-down, charges the output capacitors and is dissipated through the following means: Rds_on, Rcs, Rcu, Rcu_rt, ESR of the output capacitors and load.

$$t := 0, 10\,n \cdot s .. 10\,\mu \cdot s$$

$$I_L(t) := \left( I_{t0} - \frac{V_{MAX_FL} \cdot t}{L_1} \right)$$

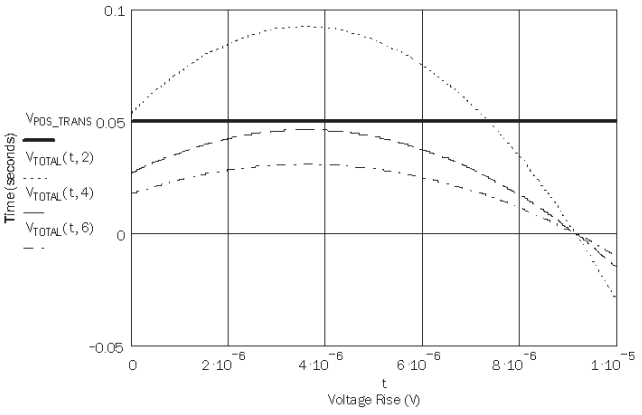
$$I_{CAP}(t) := I_L(t) - I_{LKGMAX}$$

Since the output inductor is discharging at a fixed rate, there are two terms contributing to the increase of the voltage on the output capacitors: 1) is due to the ESR of the output capacitor; 2) is due to the added charge contributed by the inductor current.

$$V_{ESR}(t, N_{CAP}) := I_{CAP}(t) \cdot \frac{R_{ESR}}{N_{CAP}}$$

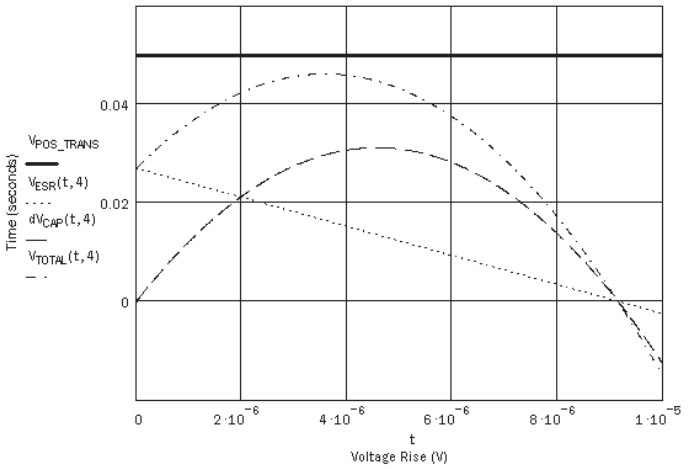
$$dV_{CAP}(t, N_{CAP}) := \frac{I_{CAP}(t) \cdot t}{C_{OUT} \cdot N_{CAP}}$$

$$V_{TOTAL}(t, N_{CAP}) := V_{ESR}(t, N_{CAP}) + dV_{CAP}(t, N_{CAP})$$




The chart above shows the system response for the capacitors defined in Step 1 and the chart to follow shows the details of the response for the chosen number of output capacitors.

## Applications Information (Cont.)




Step 3 — Setting RHYS

The next step is to calculate $R_{HYS}$. Since the SC453 is a hysteretic controller, it regulates the amount of output ripple according to a hysteresis value set by $R_{HYS}$. The designer must therefore decide upon the amount of desired output ripple, and then set $R_{HYS}$ accordingly.

The hysteresis controls the amount of ripple voltage at the point of regulation, which is the point between the inductor and the current sense resistor. The amount of ripple at the output is defined by the current sense resistor and the output capacitor ESR. This factor is taken into account in the equation shown below relating $V_{RIPPLE}$ to $V_{HYS}$.

To achieve tight accuracy, it is recommended that the output ripple be set to 20mV peak-to-peak.

$$ESR := \frac{R_{ESR}}{N_{CAP}} \qquad ESR = 1.5 \times 10^{-3}\ \Omega$$

$$V_{RIPPLE} = 0.02\ V$$

$$V_{HYS} := V_{RIPPLE} \cdot \frac{(R_{CS} + ESR)}{ESR}$$

$$V_{HYS} = 0.033\ V$$

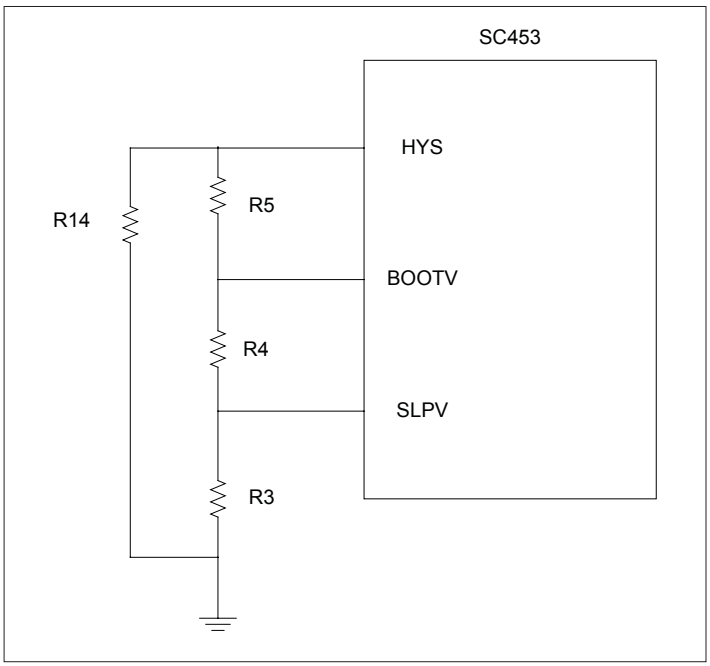
$V_{HYS}$ is created by switching a current source ($I_{HYS}$) through a resistor in series with the CMP pin. The $I_{HYS}$ value is controlled via $R_{HYS}$. For simplicity it is easier to select a value for CMP resistor (R7, see Typical Application Circuit on page 2) and then calculate $R_{HYS}$, as follows.

$$R_7 := 1K\cdot\Omega$$

$$R_{HYS} := \frac{2\cdot V_{REF}}{\left(\frac{V_{HYS}}{R_7}\right)} \qquad R_{HYS} = 102.0\ K\Omega$$

.

In the SC453 application circuit, $R_{HYS}$ consists of three resistors (R3, R4 and R5) in parallel with R14. These resistors also form the dividers for BOOTV and SLPV. Note also that depending on circuit layout and parasitics, $R_{HYS}$ may have to be adjusted slightly to obtain optimum performance. (The above resistors will be calculated after the PBOOT and deeper sleep voltages are set later in this procedure). To increase hysteresis without having to change the divider resistors, a fourth resistor (R14), can be added. Additional hysteresis is needed when inductances in the current sense paths cause additional signal that adds to the resistive signal, limiting the accuracy of the calculations.



## Applications Information (Cont.)

Step 4 — BOOTV Design

The boot-up voltage for $V_{CORE}$ is set at 1.2V. For the SC453 typical application circuit, R3, R4, and R5 form a voltage divider off $V_{REF}$ and are used to set the boot voltage. For simplicity $R_{BOOT} := R3 + R4$.

$$V_{BOOT} := 1.2\ V$$

$$R_{HYS} := \frac{1}{\frac{1}{R_{25}} + \frac{1}{R_{BOOT} + R_5}}$$

$$R_{BOOT} := \frac{V_{BOOT} \cdot R_5}{V_{REF} - V_{BOOT}}$$

Step 5 — Sleep Voltage Design

The sleep voltage is set at 0.750V nominally using the R3 - R4 - R5 divider.

$$V_{SLP} := 0.750\ V$$

$$R_3 := V_{SLP} \cdot \frac{(R_4 + R_5)}{V_{REF} - V_{SLP}}$$

R3, R4, and R5 are calculated using a matrix to solve the simultaneous equations. R14 is set at 1MΩ as a placeholder:

$$R_{14} := 1000\ K\Omega$$

$$M_x := \begin{pmatrix} 1 & 1 & 1 \\ 1 & 1 & -\frac{V_{BOOT}}{V_{REF} - V_{BOOT}} \\ 1 & V_{SLP} \cdot \frac{-1}{V_{REF} - V_{SLP}} & V_{SLP} \cdot \frac{-1}{V_{REF} - V_{SLP}} \end{pmatrix}$$

$$v := \begin{pmatrix} \frac{R_{14} \cdot R_{HYS}}{R_{14} - R_{HYS}} \\ 0 \\ 0 \end{pmatrix}$$

$$soln := lsolve(M_x, v) \qquad soln = \begin{pmatrix} 5.011 \times 10^4 \\ 3.007 \times 10^4 \\ 3.341 \times 10^4 \end{pmatrix} \Omega$$

$$R_3 := (1\ \ 0\ \ 0) \cdot soln \qquad R_3 = 5.011 \times 10^4\ \Omega$$

$$R_4 := (0\ \ 1\ \ 0) \cdot soln \qquad R_4 = 3.007 \times 10^4\ \Omega$$

$$R_5 := (0\ \ 0\ \ 1) \cdot soln \qquad R_5 = 3.341 \times 10^4\ \Omega$$

From the standard 1% resistor value table, the following values are chosen according to the calculation results.

R5 = 33.2KΩ.
R4 = 30.1KΩ
R3 = 49.9KΩ

Step 6 — Current Limit Calculation

Setting the threshold for current limit is a relatively straightforward process. To do this the peak current calculation is based on the maximum DC value plus the worst-case ripple current. The following calculations apply for a single phase. Worst-case ripple occurs at the highest input voltage. Since ripple is also inversely proportional to inductance, it is recommended that the minimum inductance value be used based on the manufacturer's specified tolerance:

$$L_{LOW} := L_1 \cdot (1 - 20\,\%) \qquad L_{LOW} = 4.8 \times 10^{-7}\ H$$

$$I_{RIPPLE_MAX} := \frac{(V_{INMAX} - V_{MAX_NL}) \cdot d_{MIN}}{L_{LOW} \cdot F_S}$$

$$I_{RIPPLE_MAX} = 6.777\ A$$

## Applications Information (Cont.)

To calculate the maximum DC value of current the maximum DC current must be added to the maximum ripple value to obtain peak current:

$$I_{PEAK} := I_{MAX_FL} + \frac{I_{RIPPLE_MAX}}{2}$$

$$I_{PEAK} = 23.389 \quad A$$

It is recommended that the current limit be set at 120% of the peak value to allow for inductor current overshoot during load transients.

$$I_{CLIM} := 120\ \% \cdot I_{PEAK}$$

$$I_{CLIM} = 28.066 \quad A$$

The Current Limit Comparator internal to the SC453 monitors the output current and turns the high side switch off when the current exceeds the upper current limit threshold, $I_{CLMAX}$ and re-enables only if the load current drops below the lower current limit threshold, $I_{CLMIN}$. The current is sensed by monitoring the voltage drop across the current sense resistor $R_{CS}$.

Current limiting will cycle from $I_{CLMAX}$ to $I_{CLMIN}$ for 32 switching cycles to allow for short term transients, then the converter is latched off. $I_{CLMAX}$ and $I_{CLMIN}$ are set according to the following equations.

$$I_{CLMAX} := 3 \cdot V_{REF} \cdot \frac{R_{CL}}{R_{HYS} \cdot R_{CS}}$$

$$I_{CLMIN} := 2 \cdot V_{REF} \cdot \frac{R_{CL}}{R_{HYS} \cdot R_{CS}}$$

The current limit is set at $I_{CLIM}$ = ICLMAX, and then solve for $R_{CL}$, which is R6 in the typical applications circuit. For balance, R8, in series with the CLRF pin is kept the same value as R6.

$$R_{CL} := \frac{I_{CLIM} \cdot R_{HYS} \cdot R_{CS}}{2.5 \cdot V_{REF}}$$

$$R_{CL} = 673.59 \ \Omega \qquad R_6 := 681 \ \Omega$$

$$R_8 := R_6 \qquad R_8 = 681 \ \Omega$$

Step 7 — Small Capacitors/Resistor Selection

Several small capacitors are required for signal filtering. Refer to the Typical Application Circuit on page 2. Use SMT ceramic capacitors with an X7R or better temperature coefficient. COG is preferred.

C11 and R7 are used to filter the hysteretic ripple signal. The components are sized to provide filtering above the 5th harmonic of the fundamental.

$$C11 := \frac{1}{2 \cdot \Pi \cdot R_7 \cdot F_S \cdot 5}$$

$$C11 = 9.095 \times 10^{-11} \ F$$

In the evaluation board design a 100pF ceramic capacitor is used for C11. The DAC output requires a 1nF capacitor (C23) for high frequency noise filtering. The values for C12 and C13 are calculated in a similar manner, though they are returned to the CORE pin because that is the reference point for the current limit comparator.

$$C_{12} := \frac{1}{2 \cdot \Pi \cdot R_6 \cdot F_S \cdot 5} \qquad C_{13} := C_{12}$$

$$C_{12} = 1.335 \times 10^{-10} \ F \qquad C_{13} = 1.335 \times 10^{-10} \ F$$

## Applications Information (Cont.)

Step 8 — Calculate Input RMS Current

In order to calculate the worst-case RMS current for the input capacitors, the efficiency at $V_{IN_MIN}$ and full load. is conservatively set at 80%. The actual converter efficiency depends on component selection, layout, airflow, etc.

$P_{OUT} := I_{MAX_FL} \cdot V_{MAX_FL}$ $P_{OUT} = 23.64$ W

$$P_{IN} := \frac{P_{OUT}}{85\,\%}$$

$$I_{IN_DC} := \frac{P_{IN}}{V_{INMIN}} \qquad D := \frac{V_{MAX_FL}}{V_{INMIN}} \qquad I_{IN_DC} = 3.476 \text{ A}$$

$$I_{RMS} := \sqrt{\left[\left(I_{MAX_FL}\right) - I_{IN_DC}\right]^2 \cdot D + \left[I_{IN_DC}^2 \cdot (1 - D)\right]}$$

$I_{RMS} = 7.116$ A

$C_{I_RMS} := 2\,A$

Using an RMS current rating of 2A, typical of 10µF, 25V MLCC capacitors, the number of required capacitors is calculated as shown below.

$$C_{I_NUM} := \text{ceil}\left(\frac{I_{RMS}}{C_{I_RMS}}\right) \qquad C_{I_NUM} = 4$$

The calculation indicates that four capacitors are needed to satisfy the worst-case RMS current requirement.

Input Capacitance Calculation Using Ripple Voltage

The allowable input ripple voltage seen at input capacitance is denoted dVin. For this example 250mV is used as the maximum allowable input ripple voltage. The actual ripple voltage varies with duty cycle (D). The maximum value occurs at D = 0.5.

$dVin := 250$ mV

$D_{MAX} := 0.5$

$$T_{in} := \frac{1}{F_S}$$

$$C_{IN_MIN} := \frac{I_{PEAK}}{2} \cdot \left(D_{MAX} - D_{MAX}^2\right) \cdot \frac{T_{in}}{dVin}$$

$C_{IN_MIN} = 3.341 \times 10^{-5}$ F

$C_{IN} := 10\,\mu F$

$$N_{IN_MIN_RIPPLE} := \text{ceil}\left(\frac{C_{IN_MIN}}{C_{IN}}\right)$$

$N_{IN_MIN_RIPPLE} = 4$

Based on the above calculations, four capacitors are needed to satisfy the input ripple voltage requirement.

Step 9 — OVP

No calculations are necessary for Over-Voltage Protection. If $V_{CORE}$ is greater than +14% of the DAC (i.e., out of the power good window), the SC453 will latch off and hold the low-side driver on permanently (for each phase). Either the power or EN must be recycled to clear the latch. The latch is disabled during soft-start and VID/Deeper Sleep transitions. The latch is enabled if $V_{CORE}$ exceeds 2V even during VID/Deeper Sleep transitions to ensure that the processor maximum is not exceeded. The table on Page 13 is a summary of fault conditions using SC453.

Step 10 — Soft-Start/DAC Slew Control

The soft-start cap C21 in the SC453 design serves three conditions.

1) Define the start-up ramp.

2) Define the DAC slew rate during sleep and VID transitions. During VID transitions the SS current is nominally +/- 120µA; during sleep transitions the SS current increases to +/-240µA);

3) During start-up, the SS current is normally +/- 6.5µA.

## Applications Information (Cont.)

Three soft-start examples are based on the previous three conditions for SC453 application.

1. Start-Up

$I_{SS} := 6.5\ \mu A$

$dt_{SU} := 3\ m\,s$

$dV_{dacSU} := V_{MAX_NL}$

$$C_{SS_max_startup} := \frac{I_{SS} \cdot dt_{SU}}{dV_{dacSU}}$$

$C_{SS_max_startup} = 1.609 \times 10^{-8}\ F$

2. VID Change:

$I_{SSV} := 120\ \mu A$

$dt_V := 100\ \mu s$

$dV_{dacV} := V_{MAX_NL} - V_{MIN_NL}$

$$C_{SS_max_VID} := \frac{I_{SSV} \cdot dt_V}{dV_{dacV}}$$

$C_{SS_max_VID} = 4.687 \times 10^{-8}\ F$

3. Sleep Entry/Exit:

$I_{SSS} := 240\ \mu A$

$dt_S := 33\ \mu s$

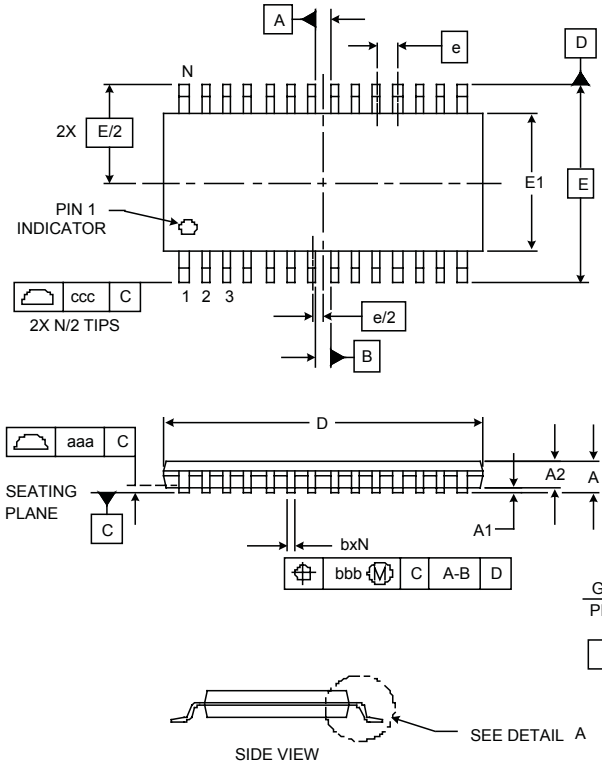
$dV_{dacS} := V_{MAX_NL} - V_{SLP}$

$$C_{SS_max_drs} := \frac{I_{SSS} \cdot dt_S}{dV_{dacS}}$$

$C_{SS_max_drs} = 1.714 \times 10^{-8}\ F$

Example 1 predicts the maximum capacitance allowed.
In order to allow tolerance C22 = 15nF is chosen.

## Outline Drawing - TSSOP-28

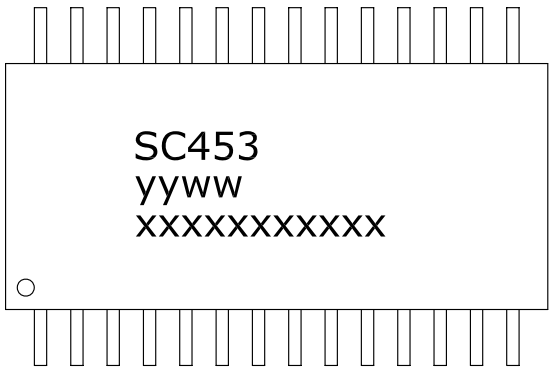



| DIM | DIMENSIONS | | | | | |
|---|---|---|---|---|---|---|
| | INCHES | | | MILLIMETERS | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | - | - | .047 | - | - | 1.20 |
| A1 | .002 | - | .006 | 0.05 | - | 0.15 |
| A2 | .031 | - | .042 | 0.80 | - | 1.05 |
| b | .007 | - | .012 | 0.19 | - | 0.30 |
| c | .003 | - | .007 | 0.09 | - | 0.20 |
| D | .378 | .382 | .386 | 9.60 | 9.70 | 9.80 |
| E1 | .169 | .173 | .177 | 4.30 | 4.40 | 4.50 |
| E | .252 BSC | | | 6.40 BSC | | |
| e | .026 BSC | | | 0.65 BSC | | |
| L | .018 | .024 | .030 | 0.45 | 0.60 | 0.75 |
| L1 | (.039) | | | (1.0) | | |
| N | 28 | | | 28 | | |
| θ1 | 0° | - | 8° | 0° | - | 8° |
| aaa | .004 | | | 0.10 | | |
| bbb | .004 | | | 0.10 | | |
| ccc | .008 | | | 0.20 | | |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AE.

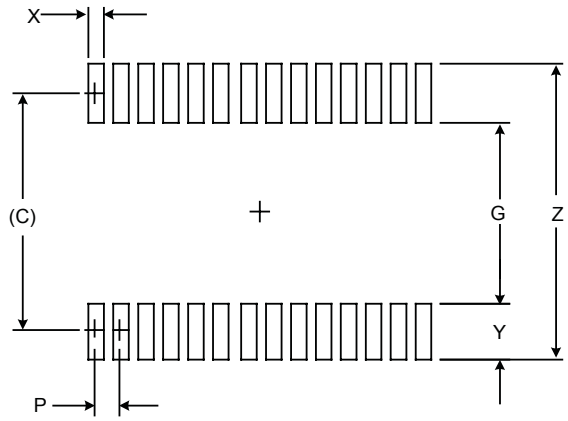
## Marking Information TSSOP-28




**yyww = Date code**

**xxxxxxxxxxx = Semtech lot number**

## Land Pattern - TSSOP-28

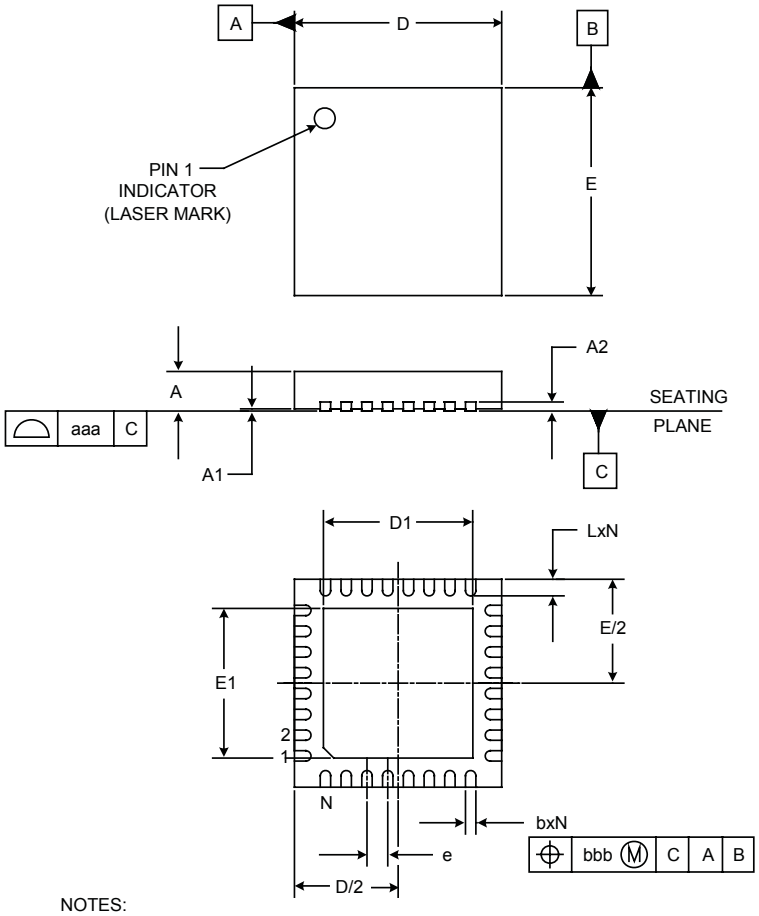



| DIMENSIONS | | |
|---|---|---|
| DIM | INCHES | MILLIMETERS |
| C | (.222) | (5.65) |
| G | .161 | 4.10 |
| P | .026 | 0.65 |
| X | .016 | 0.40 |
| Y | .061 | 1.55 |
| Z | .283 | 7.20 |

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

## Outline Drawing - MLPQ-32

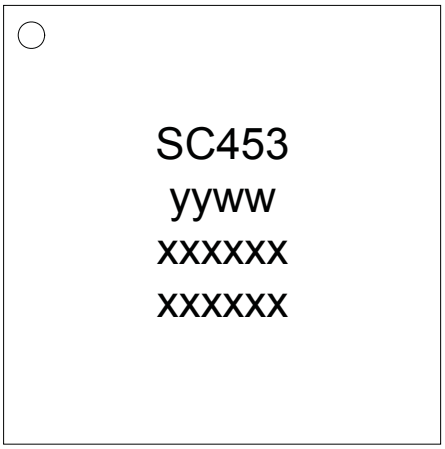



| DIM | DIMENSIONS | | | | | |
|---|---|---|---|---|---|---|
| | INCHES | | | MILLIMETERS | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | .031 | - | .039 | 0.80 | - | 1.00 |
| A1 | .000 | - | .002 | 0.00 | - | 0.05 |
| A2 | - | (.008) | - | - | (0.20) | - |
| b | .007 | .010 | .012 | 0.18 | 0.25 | 0.30 |
| D | .193 | .197 | .201 | 4.90 | 5.00 | 5.10 |
| D1 | .140 | .146 | .150 | 3.30 | 3.70 | 3.80 |
| E | .193 | .197 | .201 | 4.90 | 5.00 | 5.10 |
| E1 | .140 | .146 | .150 | 3.30 | 3.70 | 3.80 |
| e | .020 BSC | | | 0.50 BSC | | |
| L | .012 | .016 | .020 | 0.30 | 0.40 | 0.50 |
| N | 32 | | | 32 | | |
| aaa | .003 | | | 0.08 | | |
| bbb | .004 | | | 0.10 | | |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

## Marking Information MLPQ-32

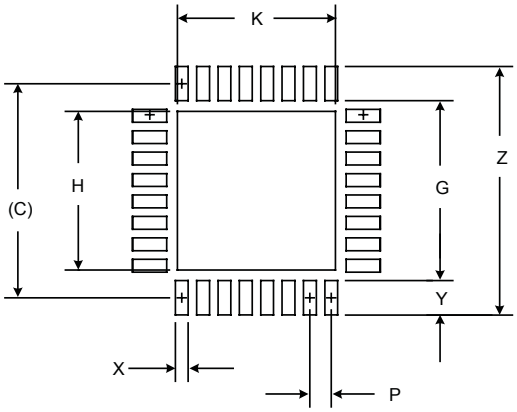



**yyww = Date code**

**xxxxxx = Semtech lot number**

**xxxxxx = Semtech lot number**

## Land Pattern - MLPQ-32




| DIMENSIONS | | |
|---|---|---|
| DIM | INCHES | MILLIMETERS |
| C | (.197) | (5.00) |
| G | .165 | 4.20 |
| H | .146 | 3.70 |
| K | .146 | 3.70 |
| P | .020 | 0.50 |
| X | .012 | 0.30 |
| Y | .031 | 0.80 |
| Z | .228 | 5.80 |

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
3. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

## Contact Information

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