Introduction

The ACS8947T JAM PLL is a general pupose, Integer N, jitter-attenuating, differential phase-locked loop for generating low jitter output clocks. Frequency translation, reference switching between clock inputs and resynchronization features are provided also. Typical application areas include Ethernet, SONET/SDH, PCI, 3G and wireless systems.

Typical output jitter generation in a SONET/SDH OC-12 system is 2.8 ps RMS, making the ACS8947T an ideal dejittering solution for use with Semtech clock and line card parts ACS8510, ACS8520, ACS8525, ACS8522, ACS8530 and ACS9510.

The ACS8947T has two differential frequency-programmable LVPECL reference inputs and one differential synchronization input. The device is capable of locking across a wide input frequency range of 580 kHz to 180 MHz. Four independently-supplied differential outputs are available, programmable as LVPECL or CML. Each output supports a maximum output frequency rate of up to 625 MHz. All device settings are fully hardwire configured. An external microprocessor is not required to program the PLL.

Features

- Highly configurable high performance Integer N PLL with integrated VCO.
- VCO frequency range 2.35 GHz to 2.9 GHz.
- Configurable closed loop bandwidth from 2 kHz upwards.
- PLL fully configured by hardwired configuration matrix: no requirement for an external microprocessor.
- Full control over internal dividers allows the device to be configured for a wide range of frequency translation and jitter cleaning applications.
- Meets RMS jitter requirements for OC3 and OC12 telecommunications systems.
- Wide input frequency range of 580 kHz to 180 MHz.
- Wide output frequency range of 1.23 MHz to 625 MHz.
- Input activity monitors and lock detector.
- Automatic or manual control of reference selection.
- External feedback option.
- Wide tracking range of 200 ppm.
- Powerful evaluation board and GUI tool for configuration and device assessment.
- 3.3 V operation: temperature range - 40°C to +85°C.
- Small outline, leadless, 7 mm x 7 mm QFN48 package.

Block Diagram

Figure 1 Simplified Block Diagram of the ACS8947T JAM PLL

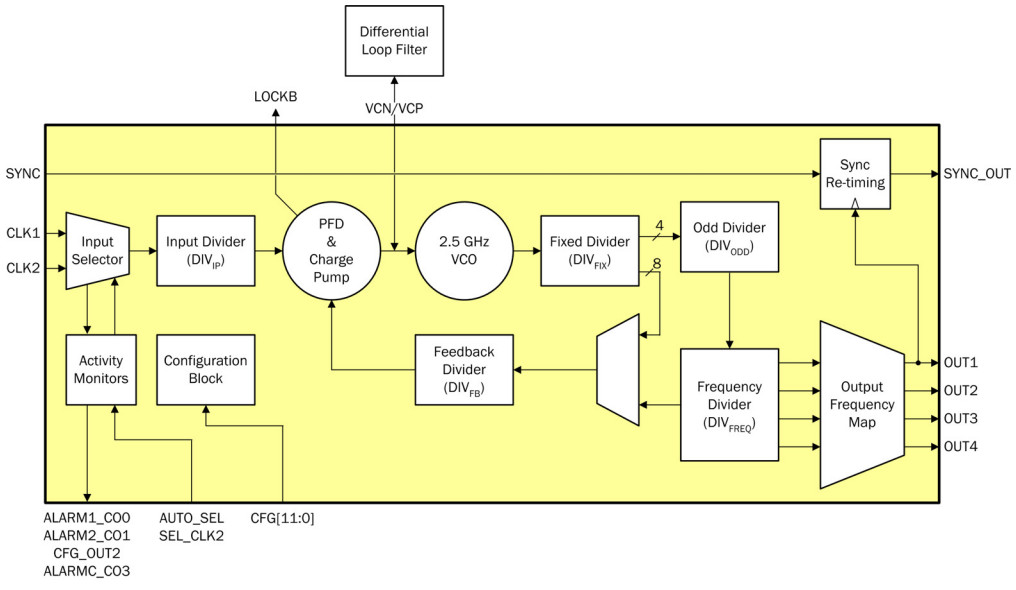
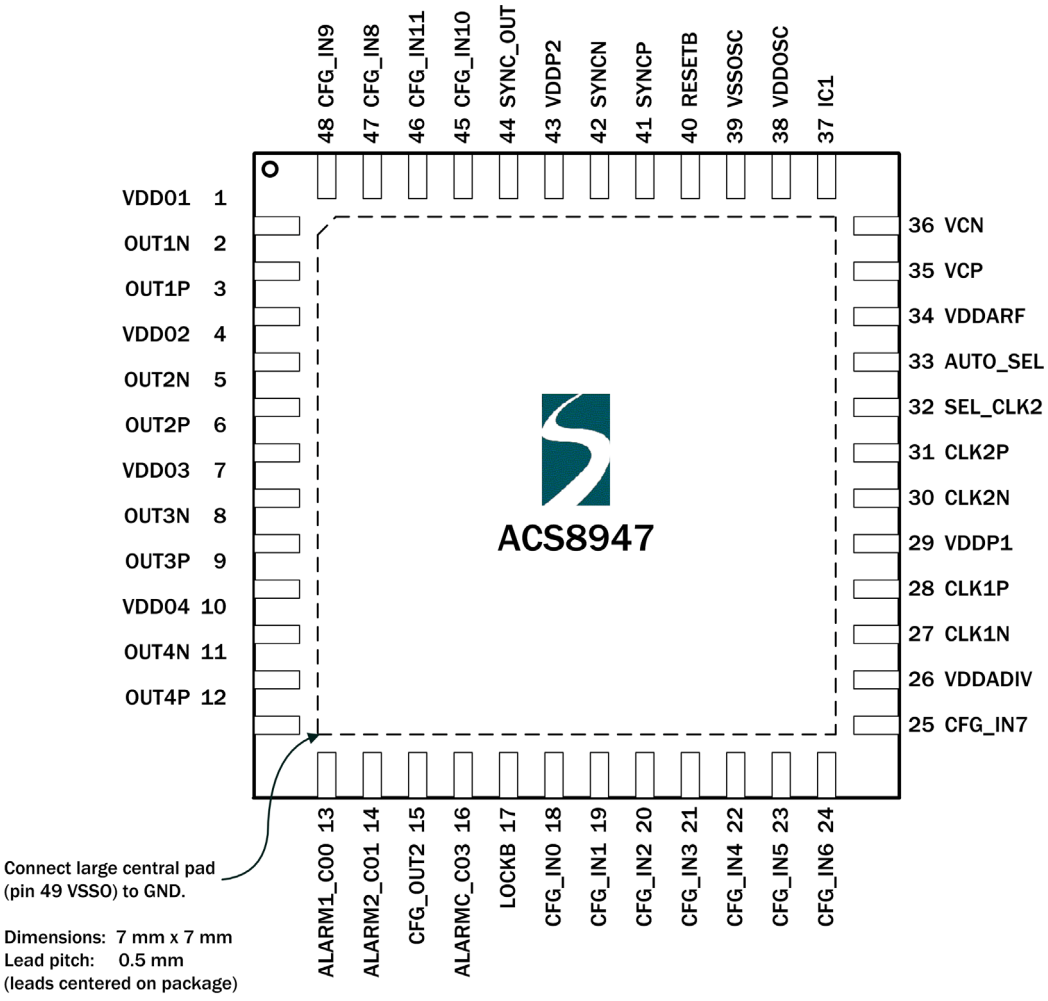


Table of Contents

Pin Diagram

Figure 2 ACS8947T Pin Diagram



Pin Descriptions

In the **I/O** column of the pin description tables that follow:

I = input
O = output
I/O = bi-directional
P = power
A = analog

In the **Type** column:

LVTTL/LVCMOS^{U} = LVTTL/LVCMOS input with pull-up resistor

LVTTL/LVCMOS$_{D}$ = LVTTL/LVCMOS input with pull down resistor

Table 1 Power pins

Pin No.	Symbol	I/O	Type	Description
1, 4, 7, 10	VDD01, VDD02, VDD03, VDD04	P	-	Independent voltage supplies to power each clock output (differential pair of pins) OUT1N/P to OUT4N/P respectively. +3.3 V (±5%). To disable an output and save power, tie associated VDD to 0V.
26	VDDADIV	P	-	Supply voltage for internal dividers in VCO loop, kept as an isolated supply to allow for low supply noise for the output divider stages. +3.3 V (±5%).
29	VDDP1	P	-	Supply voltage to differential inputs, alarm and configuration pins. +3.3 V (±5%).
43	VDDP2	P	-	Supply voltage to SYNC input and output pins, rate selection pins, input selection pins and reset pin. +3.3 V (±5%).
34	VDDARF	P	-	Supply voltage for phase and frequency detector (PFD), kept as an isolated supply to allow for low supply noise. +3.3 V (±5%).
38	VDDOSC	P	-	Supply voltage to the internal VCO. +3.3 V (+5%/-10%).
39	VSSOSC	P	-	Supply ground 0 V for the internal VCO.
49	VSS0	P	-	Common supply ground 0 V. This is the central leadframe pad on the underside of the package.

Table 2 Internally connected pins

Pin No.	Symbol	I/O	Type	Description
37	IC1	-	-	Connect to ground.

Table 3 Functional Pins

Pin No.	Symbol	I/O	Type	Description
2	OUT1N	O	CML or LVPECL	One of four CML or LVPECL differential outputs, partnered with pin 3. Programmable at spot frequencies from 1.23 MHz to 625 MHz. The output frequency is defined by the configuration pin settings at power up or when RESETB is asserted (logic 0). See PLL Configuration. The output is ON when VDD01 is supplied with 3.3 V, or OFF when VDD01 is tied to zero volts. If VDD01 is connected to 0 V, remove the external biasing resistors.
3	OUT1P	O	CML or LVPECL	CML or LVPECL differential output partnered with pin 2. See pin 2 description for more detail.

Table 3 Functional Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
5	OUT2N	O	CML or LVPECL	One of four CML or LVPECL differential outputs, partnered with pin 6. Programmable at spot frequencies from 1.23 MHz up to 625 MHz. The output frequency is defined by the configuration pin settings at power up or when RESETB is asserted (logic 0). See PLL Configuration. The output is ON when VDD02 is supplied with 3.3 V, or OFF when VDD02 is tied to zero volts. If VDD02 is connected to 0 V, remove the external biasing resistors.
6	OUT2P	O	CML or LVPECL	CML or LVPECL differential output partnered with pin 5. See OUT2_N (pin 5) for more detail.
8	OUT3N	O	CML or LVPECL	One of four CML or LVPECL differential outputs, partnered with pin 9. Programmable at spot frequencies from 1.23 MHz up to 625 MHz. The output frequency is defined by the configuration pin settings at power up or when RESETB is asserted (logic 0). See PLL Configuration. The output is ON when VDD03 is supplied with 3.3 V, or OFF when VDD03 is tied to zero volts. If VDD03 is connected to 0 V, remove the external biasing resistors.
9	OUT3P	O	CML or LVPECL	CML or LVPECL differential output partnered with pin 8. See pin 8 description for more detail.
11	OUT4N	O	CML or LVPECL	One of four CML or LVPECL differential outputs, partnered with pin 12. Programmable at spot frequencies from 1.23 MHz up to 625 MHz. The output frequency is defined by the configuration pin settings at power up or when RESETB is asserted (logic 0). See PLL Configuration. The output is ON when VDD04 is supplied with 3.3 V, or OFF when VDD04 is tied to zero volts. If VDD04 is connected to 0 V, remove the external biasing resistors.
12	OUT4P	O	CML or LVPECL	CML or LVPECL differential output partnered with pin 11. See pin 11 description for more detail.
13	ALARM1_CO0	O	LVTTL/ LVCMOS	Activity alarm output for the CLK1P/CLK1N input reference clock. Active high; high indicating clock failure. It is also used to configure the device at power-up, where it is used as a configuration output pin, that may be connected to CFG_IN[11:0] input pins as required. See PLL Configuration.
14	ALARM2_CO1	O	LVTTL/ LVCMOS	Activity alarm output for the CLK2P/CLK2N input reference clock. Active high; high indicating clock failure. It is also used to configure the device at power-up time, where it is used as a configuration output pin, that may be connected to CFG_IN[11:0] input pins as required. See PLL Configuration.
15	CFG_OUT2	O	LVTTL/ LVCMOS	Configuration pin, used in the configuration on power-up of expected input clock frequency and Resync selection, by connecting to appropriate pin from the CFG_IN[11:0] pins as required. See PLL Configuration.
16	ALARMC_CO3	O	LVTTL/ LVCMOS	Activity alarm output for the currently selected input reference clock. Active high; high indicating clock failure. It is also used to configure the device at power-up, where it is used as a configuration output pin that may be connected to CFG_IN[11:0] input pins as required. See PLL Configuration.
17	LOCKB	O	Analog	Lock detect output. This is a pulse-width modulated output current, with each pulse typically +10 µA. The output produces a pulse with a width in proportion to the phase error seen at the internal phase detector. This pin should be connected via an external parallel capacitor and resistor to ground. The pin voltage will then give an indication of phase lock: When low, the device is phase locked; when high the device has frequent large phase errors and so is not phase locked. The value of the RC components used determines the time and level of consistency required for lock indication. If LOCKB is disabled by configuration the LOCKB output is held low.

Table 3 Functional Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
18	CFG_IN0	I	LVTTL/ $LVCMOS_D$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
19	CFG_IN1	I	LVTTL/ $LVCMOS_D$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
20	CFG_IN2	I	LVTTL/ $LVCMOS_D$ Schmitt Trigger	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
21	CFG_IN3	I	LVTTL/ $LVCMOS_D$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
22	CFG_IN4	I	LVTTL/ $LVCMOS_D$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
23	CFG_IN5	I	LVTTL/ $LVCMOS_D$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
24	CFG_IN6	I	LVTTL/ $LVCMOS_D$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
25	CFG_IN7	I	LVTTL/ $LVCMOS_D$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
27	CLK1N	I	LVPECL	Negative differential input reference clock partnered with pin 28. Accepts a wide range of input frequencies from 580 kHz to 180 MHz. Accepts LVPECL, LVDS or CML inputs given suitable external interface components (see Input and Output Interface Terminations). Selection between CLK1 and CLK2 is configurable between manual or automatic. See Table 5.
28	CLK1P	I	LVPECL	Positive differential input reference clock partnered with pin 27. Accepts a wide range of input frequencies from 580 kHz to 180 MHz. Accepts LVPECL, LVDS or CML inputs given suitable external interface components (see Input and Output Interface Terminations). Selection between CLK1 and CLK2 is configurable between manual or automatic. See Table 5.
30	CLK2N	I	LVPECL	Negative differential input reference clock partnered with pin 31. Accepts a wide range of input frequencies from 580 kHz to 180 MHz. Accepts LVPECL, LVDS or CML inputs given suitable external interface components (see Input and Output Interface Terminations). Selection between CLK1 and CLK2 is configurable between manual or automatic. See Table 5.
31	CLK2P	I	LVPECL	Positive differential input reference clock partnered with pin 30. Accepts a wide range of input frequencies from 580 kHz to 180 MHz. Accepts LVPECL, LVDS or CML inputs given suitable external interface components (see Input and Output Interface Terminations). Selection between CLK1 and CLK2 is configurable between manual or automatic. See Table 5.
32	SEL_CLK2	I	LVTTL/ $LVCMOS_D$	Used in combination with AUTO_SEL (pin 33) to select the CLK1 input (low) or CLK2 input (high) in manual control mode, or to select automatic switching mode as described in Table 5.
33	AUTO_SEL	I	LVTTL/ $LVCMOS_D$	Used in combination with SEL_CLK2 (pin 32) to select automatic switching mode as described in Table 5.

Table 3 Functional Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
35	VCP	A	Analog	Connection for external loop filter components. This is the differential control voltage input to the internal VCO and the internal differential charge pump output up to a level of 210 µA.
36	VCN	A	Analog	Connection for external loop filter components. This is the differential control voltage input to the internal VCO and the internal differential charge pump output up to a level of 210 µA.
40	RESETB	I	LVTTL/ LVCMOS^{U} Schmitt Trigger	Active low reset signal with pull up and Schmitt type input. Used to apply an active-low Power-on Reset (POR) signal during system initialization. Should be connected via a capacitor to ground or, if reset control by a microcontroller is required, via a 3.3 V control line.
41	SYNCP	I	LVPECL	Differential input (typically 8 kHz) where the SYNC signal on this input is sampled and resynchronized to the rising edge of the OUT1 clock signal. Paired with pin 42 (SYNCN). Maximum input frequency is 40 MHz. Will accept LVDS, CML or LVPECL signals when suitable external biasing components are used. See Input and Output Interface Terminations.
42	SYNCN	I	LVPECL	Differential input (typically 8 kHz) where the SYNC signal on this input is sampled and resynchronized to the rising edge of the OUT1 clock signal. Paired with pin 41 (SYNCP). Maximum input frequency is 40 MHz. Will accept LVDS, CML or LVPECL signals when suitable external biasing components are used. See Input and Output Interface Terminations.
44	SYNC_OUT	O	LVTTL/ LVCMOS	A sampled and resynchronized version of the SYNC signal present on SYNCP (pin 41) and SYNCN (pin 42). The SYNC_OUT signal is synchronized to the rising edge of the output clock present on OUT1. If the SYNC function is used, the output frequency on OUT1 should be at least double the frequency of the SYNCP/SYNCN input and restricted to a maximum of 80 MHz. This restriction affects the OUT1 signal only.
45	CFG_IN10	I	LVTTL/ LVCMOS$_{D}$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
46	CFG_IN11	I	LVTTL/ LVCMOS$_{D}$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
47	CFG_IN8	I	LVTTL/ LVCMOS$_{D}$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.
48	CFG_IN9	I	LVTTL/ LVCMOS$_{D}$	Configuration input pin. Connection to this pin is defined by the ACS8947T evaluation software GUI. See PLL Configuration.

Description

The ACS8947T is a highly configurable general purpose Integer-N, low-jitter integrated PLL for signal cleaning, dejittering and frequency translation. The PLL is built around an integrated voltage controlled oscillator(VCO) and can be used in a wide range of applications including OC12 clock cleaning for SONET, SDH, Ethernet, PCI, RapidIO, 3G and wireless systems.

The device can be fully programmed, without the need for a microprocessor, by hardwiring the configuration input pins CFG_IN[11:0] to ALARM1_CO0, ALARM2_CO1, CFG_OUT2, ALARMC_CO3, VDD and GND as defined by the ACS8947T evaluation software GUI.

The PLL has a fully differential external loop filter, allowing the closed loop bandwidth and damping factor to be customized according to target system requirements. The tables below show typical loop filter component values and divider settings for various applications.

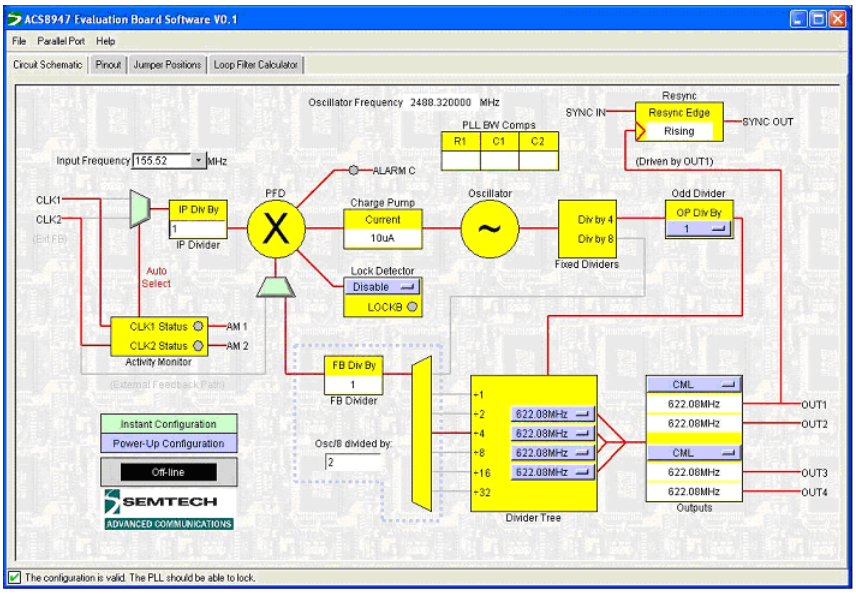
Table 4 Typical Loop Filter Component Values and Divider Settings

Application	I/P (MHz)	O/P (MHz)	VCO (MHz/V)	PFD (MHz)	OSC/8	DIV_{IP}	DIV_{ODD}	Closed Loop Bandwidth (kHz)	Damping Factor	I_{CP} (µA)	C_P (nF)	C_s (µF)	R_s (Ω)
					Divided By								
E1	2.048	65.536	2883	2.048	176	1	11	2	3.8	210	1.5	22	470
DS1	1.544	49.408	2767	1.544	224	1	7	2	3.8	210	1.2	15	680
E3	34.368	68.736	2749	34.37	10	1	5	10	1.2	160	0.56	0.068	2700
DS3	44.736	44.736	2863	44.74	8	1	1	2	1.2	40	82	6.8	82
SONET	19.44	622.08	2488	19.44	16	1	1	2	1.2	160	150	15	56
Ethernet	25	625	2500	12.5	25	2	1	2	1.2	210	120	15	68
Ethernet	62.5	125	2500	62.5	5	1	5	2	1.2	40	82	15	82
Ethernet	10	100	2800	10	35	1	7	100	3.8	210	0.56	0.68	2700
PCI	133	133	2660	66.5	5	2	5	2	1.2	40	120	15	68
Memory	167	167	2672	167	2	1	1	2	3.8	10	4.7	68	150
3G	3.84	61.44	2457	3.84	80	1	5	30	1.7	210	0.18	0.68	1500
Wireless	153.6	153.6	2457	153.6	2	1	1	2	3.8	10	3.9	47	150

The ACS8947T is available in a small form factor QFN48 package of outer dimensions 7 mm x 7 mm x 0.9 mm.

An evaluation board and GUI software for calculating the required loop filter component values and configuration wiring connections, and for hands-on device assessment, are available on request.

Figure 3 Example of EVB GUI



Inputs

Clock Inputs

The ACS8947T has two LVPECL differential clock inputs (CLK1N/P and CLK2N/P) and is capable of locking across a wide frequency range of 580 kHz to 180 MHz. If both input clocks are being used, the frequency difference between the signals presented to CLK1N/P and CLK2N/P must be within ±100 ppm. Unused positive differential inputs should be wired to GND and unused negative differential inputs should be wired to VDD.

The clock inputs are designed to accept LVDS, LVPECLor CML inputs, given suitable passive resistive and capacitive interface components.

On device reset, the configuration protocol presets the internal divider ratios and enables a fast frequency tuning algorithm that temporarily forces PLL bandwidth and locking range to be wide. This enables the PLL to automatically scan and lock to the target reference frequency present on the selected input channel.Once lock is acquired, the PLL bandwidth is reduced and frequency tracking range limited to ±200 ppm. It is therefore important to ensure that the correct input frequency is present on CLK1N/P and CLK2N/P prior to resetting the ACS8947T.

See PLL Configuration for details on how to configure the PLL dividers.

Either clock input can be manually or automatically selected as the current reference, based on the detection of clock activity. Signals AUTO_SEL and SEL_CLK2 shown in Table 5 are used to control the input clock selection. In automatic mode, the selection between CLK1 and CLK2 is non-revertive: i.e. if the PLL is locked on to CLK1 and CLK1 fails and the PLL switches to CLK2, when CLK1 becomes operational again, the PLL does not revert to CLK1.

Table 5 Clock Input Selection Decoding

AUTO_SEL	SEL_CLK2	Selected Reference	Feedback Clock
0	0	CLK1	Internal path
0	1	CLK2	Internal path
1	0	CLK1	CLK2
1	1	AUTOMATIC SELECTION (determined by activity monitor)	Internal path

External feedback

An external feedback mode is available and can be used for greater control of phase discrepancies: for example when using external buffers. In external feedback mode, the reference clock is presented to CLK1N/P and the external feedback signal is presented to CLK2N/P. In this mode, CLK1N/P is the only permitted input.

Source Switching

Figure 4 Simplified State Diagram of Source Switching

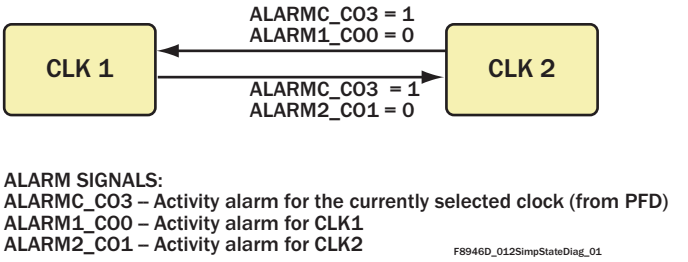


Figure 4 shows a simplified view of the automatic switching behavior in the presence of activity alarms. Signal ALARMC_CO3 from the PFD is used to disqualify a clock, and signals ALARM1_CO0 and ALARM2_CO1 (representing no activity on input clocks CLK1 and CLK2 respectively), determine whether to select the remaining clock. Switching between CLK1 and CLK2 is non-revertive.

With ALARMC_CO3 providing a view of the currently selected clock that is independent of the ALARM1_CO0 and ALARM2_CO1 signals, source selection behavior can be more complex when these alarm signals disagree. Consequently, to accommodate such behavior, the state machine is necessarily more complex than that shown here: e.g. when a clock signal is disconnected for a very short period, or when an input clock is running at the wrong frequency.

For more information, please contact Semtech Sales Support.

Activity Alarms

Input activity monitors ALARM1_CO0 and ALARM2_CO1 flag the occurrence of six or more consecutive missing cycles from inputs CLK1N/P and CLK2N/P. The alarm signals operate on the input reference clock prior to the internal PFD, and use an internal feedback clock from the VCO to determine whether the reference clock has failed.

ALARMC_CO3 is an additional activity alarm that monitors clock inputs to the PFD. This signal is more sensitive than ALARM1_CO0 and ALARM2_CO1, triggering after three missing clock edges to the PFD rather than at complete failure of the input reference clock. Although alarm ALARMC_CO3 has greater sensitivity than the input activity monitor, it may take longer to assert if the input divide ratio is greater than 2.

All activity monitor flags are low during normal operation and active high when missing clock cycles are detected.

SYNC Input

In addition to the main input clock inputs, a single differential SYNC input is provided. It provides a resynchronization path to SYNC_OUT that is clocked and synchronized to the rising edge of the OUT1 clock. The SYNC input frequency should be limited to half the OUT1 clock rate, up to a maximum of 40 MHz. For correct operation, the OUT1 output frequency should be at least double that of the SYNC clock.

Input Divider DIV_{IP}

The selected input clock is connected to the PFD via an 8-bit programable divider capable of division ratios from 1 to a maximum 256.

Feedback Divider DIV_{FB}

The feedback path from the internal 2.35 GHz to 2.9 GHz oscillator to the PFD includes a 9-bit programmable divider that is capable of division ratios from 1 to a maximum of 512. Depending on the chosen output frequency, this divider is in series with a fixed divide-by-8 or the odd divider path described below.

Odd Divider DIV_{ODD}

The odd divider is capable of division ratios 1, 3, 5, 7, 9,11, 13 and 15. The output of the divider is connected to the output multiplexing and divider stage. If odd number division is used, the frequency adjustment factor applies to all outputs - adjusting all selected output frequencies proportionally.

Under some PLL configurations, the odd divider may also be included in the feedback path to the PFD.

Phase and Frequency Detector

The internal phase and frequency detector is designed to operate across the full input frequency range of 580 kHz to 180 MHz and includes the ALARMC_CO3 activity alarm.

Charge Pumps and External Low-Pass Filter

A differential charge pump is used to drive the external loop filter via pins VCN and VCP. For linear operation of the PLL, the differential voltage range is limited to ±1.2 V centered around a typical common mode voltage of 1.25 V.

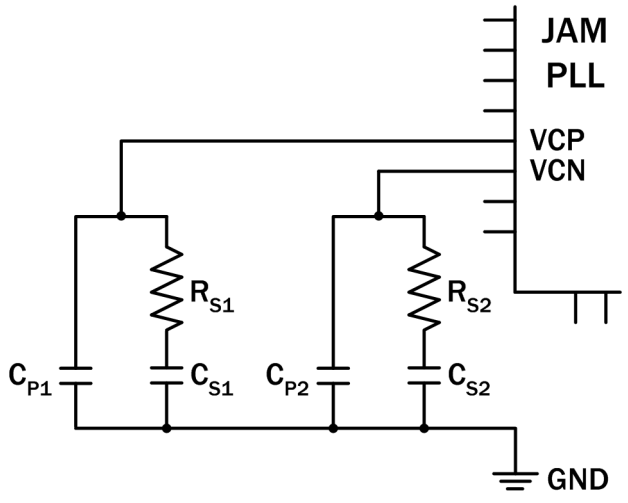
To maintain sensible external component values, the magnitude of the charge pump current (IC) is dependent on the OSC/8 divider ratio as defined in Table 6.

Table 6 Relationship of IC and OSC/8 Divider Ratio

IC (µA)	OSC/8 Divide By
10	1 -> 2
40	3 -> 8
160	9 -> 24
210	25 -> 512

The closed loop PLL bandwidth is set by two identical sets of passive RC components that connect to the differential charge pump outputs pins VCN and VCP. Figure 5 shows the recommended configuration of the second order loop differential filter.

Figure 5 Configuration of Second Order Loop Filter



Refer to PLL Configuration for details on how to calculate the loop filter component values for a given closed loop bandwidth and phase margin. Automatic calculation is available in the the ACS8947T evaluation software GUI.

Voltage Controlled Oscillator

The internal VCO operates across a frequency range of 2.35 GHz to 2.9 GHz. The VCO frequency is divided down to the selected output rate, giving a precise 50/50 balanced mark/space ratio for the output.

Output Multiplexer and Divider

A 5-bit tapped, differential CML divider tree is used in conjunction with the odd divider to generate the required output frequencies. The divider ratios are set according to the frequency list defined by the external configuration wiring and cannot be modified once the device is locked.

The device automatically allocates the frequency list to outputs as part of the PLL configuration sequence.

Outputs

Four programmable LVPECL/CML differential outputs are provided via signal pairs OUT[4:1]N/P (pins 11/12, 8/9, 5/6 and 2/3). Interfacing to LVDS is also possible using suitable passive components (see Input and Output Interface Terminations). The frequency assigned to each output is programable between 1.23 MHz and 625 MHz and, during device reset, is set by the frequency map defined by the configuration sequence. Although the theoretical maximum output frequency of the PLL is 725 MHz, the output ports are only guaranteed to meet VOH/VOL to a maximum of 625 MHz.

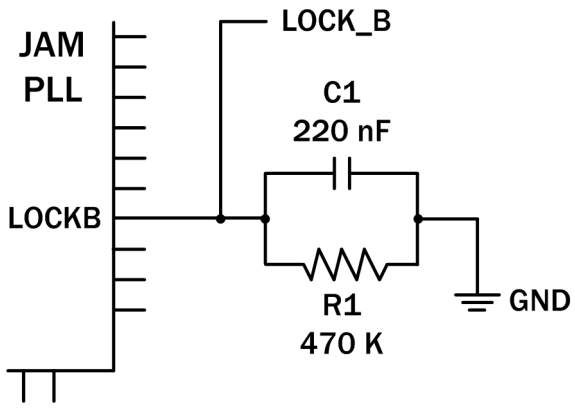
Each differential output has a dedicated power supply pin that should be connected to VDD if the output is required to be active. If an output port is not required, connect the dedicated power pin to ground to disable the differential output.

Lock Detector

A simple lock detector is incorporated. It combines the plus and minus phase errors output from the PFD so that, if any phase error signal is present, the LOCKB output drives a PWM +10 µA current. The mark/space ratio indicates the current input phase error.

By filtering this signal with a basic external RC parallel filter as shown in Figure 6, a signal whose output level indicates PLL phase and frequency lock is obtained.

Figure 6 Lock Detector External RC Filter



The filtering components are external so that the time to indicate lock can be optimized for the application. The output indicates both phase and frequency lock. During off-frequency conditions, the LOCKB output is predominately high.

Jitter Filtering

Input jitter is attenuated by the PLL with the frequency cut-off point (Fc), at which jitter is tracked or attenuated, defined by the -3 dB point: i.e. the position of the first pole of the PLL loop filter. The bandwidth is the frequency at which the first pole occurs and is defined by the component value selected for the filter.

For a 19.44 MHz input, using a loop filter bandwidth of 2 kHz and damping factor of 1.2 gives:

- High input jitter attenuation and roll off:
  - 20 dB/decade from first loop filter pole, (Fc);
  - 40 dB/decade from 2nd pole (typically 10 x Fc).
- Jitter peaking is less than 1 dB (dependent on the loop filter components);
- Typical final output jitter: e.g. 2.8 ps RMS measured over the integration range of 12 kHz to 20 MHz offset from carrier.

Input Jitter Tolerance

Jitter tolerance is defined as the maximum amplitude of sinusoidal jitter that can exist on the input reference clock above which the device fails to acquire/maintain lock.

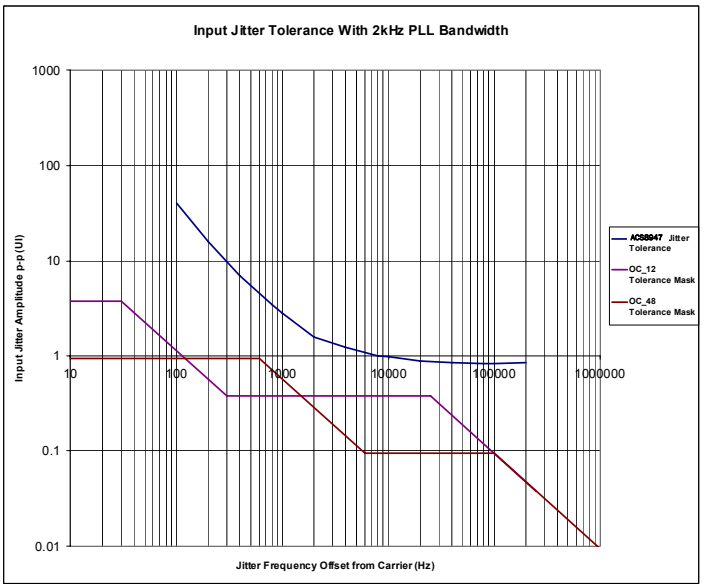
For the stand-alone device, the jitter tolerance for an undivided reference (i.e. full rate PFD) is shown in Figure 7.

For frequencies below the PLL bandwidth, jitter tolerance is seen to decrease at a rate of -20 dB per decade. For jitter frequencies above the PLL bandwidth, jitter tolerance is limited to 0.9 UI p-p.

Note...If the reference clock is divided, then the jitter tolerance will be improved.

When the ACS8947T follows an ACS8525, the input jitter tolerance is wholly defined by the latter. The system jitter tolerance is dramatically increased due to the extended phase capture range of the digital PLL within the ACS8525.

Figure 7 Jitter Tolerance ACS8947T

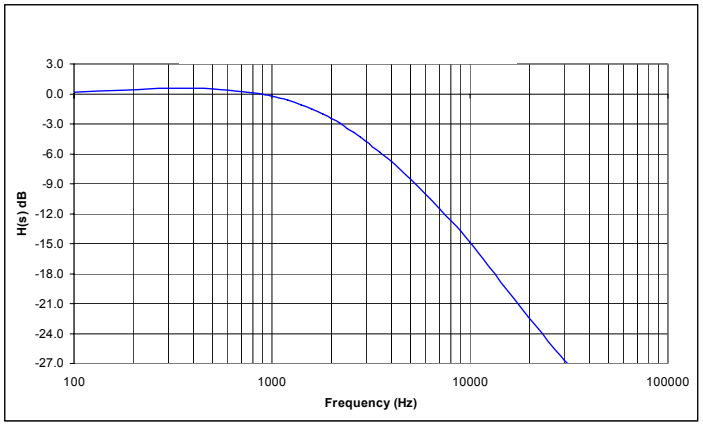


Jitter Transfer

Jitter transfer is a ratio of input jitter present on the reference clock to filtered jitter present on the output clock. The ACS8947T jitter transfer characteristic is defined solely by the loop filter bandwidth.

Figure 8 is an example showing the measured jitter transfer characteristic on a 19.44 MHz reference clock with a closed loop bandwidth of 2 KHz and a damping factor of 1.2.

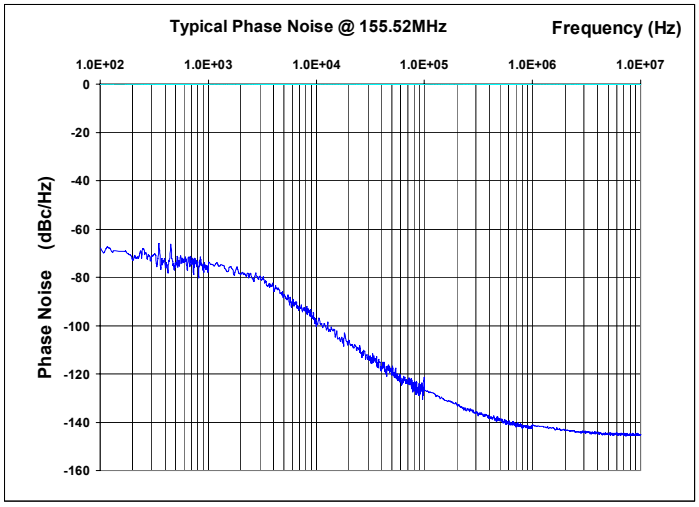
Figure 8 Jitter Transfer Characteristic - ACS8947T Stand-alone



Phase Noise Performance

The inherent jitter generation by the ACS8947T is shown in the phase noise plot in Figure 9, measured on a 155.52 MHz output clock using an input reference of 19.44 MHz.

Figure 9 Phase Noise Offset from Carrier of ACS8947T 622.08 MHz output clock



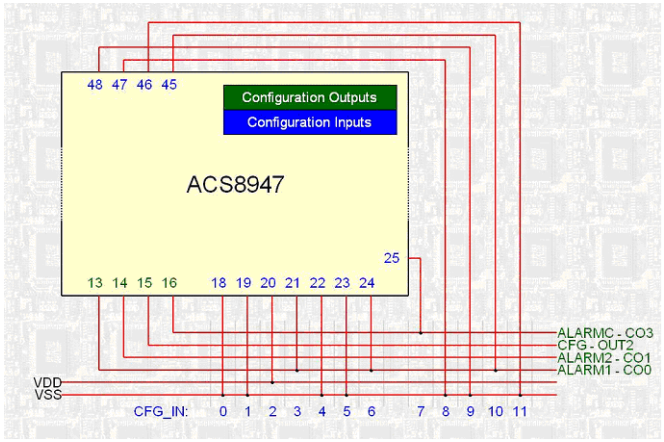
PLL Configuration

On device reset all divider ratios, charge pump settings, lock detector mode and output pad types are set by the Configuration Block, which decodes the wiring connections present on CFG[11:0]. This allows the PLL to be entirely configured without the need for an external microprocessor.

The configuration pins CFG[11:0] (device pins 18:25 and 48:45) are hardwired (via VDD, GND, ALARM1_CO0, ALARM2_CO1, CFG_OUT2, or ALARMC_CO3) to produce a unique programming code. On device reset, this code is decoded and used to configure the PLL.

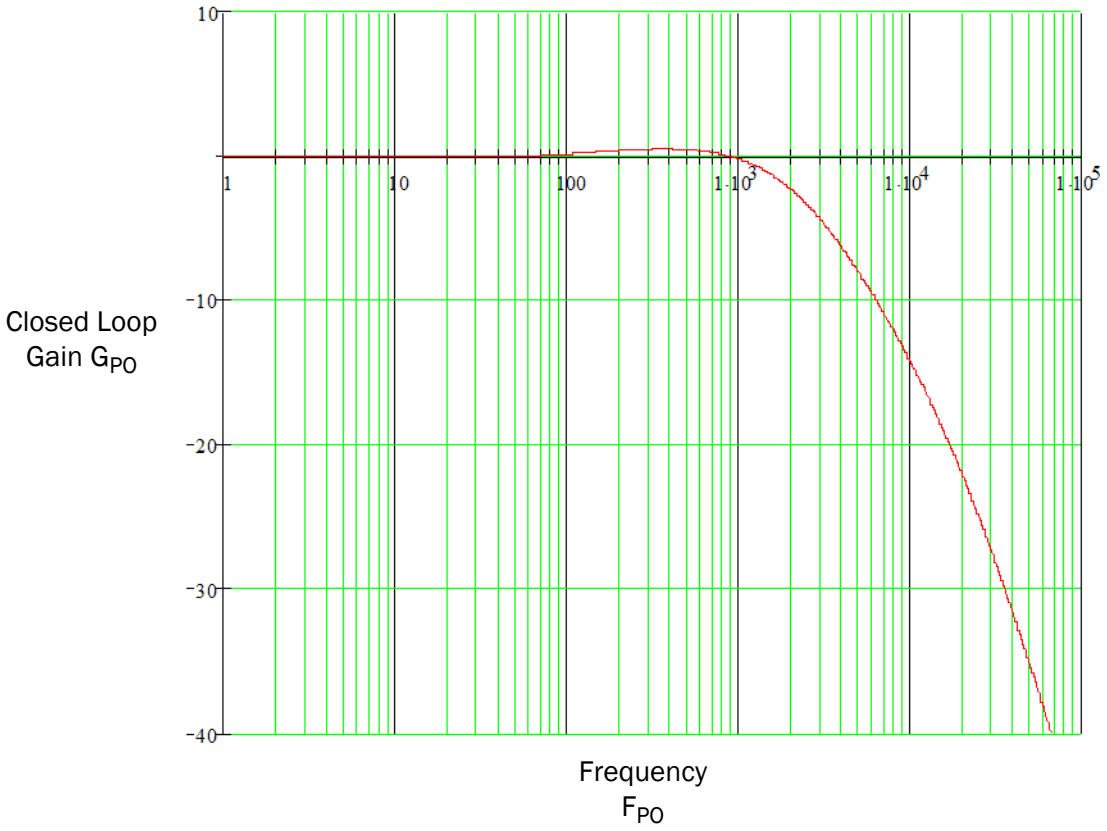
Evaluation software that calculates the configuration hardwire connection matrix for CFG[11:0] based on the required PLL setup is available for download from Semtech. Figure 10 shows a typical connection sheet.

Figure 10 Example of ACS8947T Connection Sheet



Use of the ACS8947T evaluation software is the simplest and preferred method of calculating the required divider ratios as this will also calculate loop filter component values and configuration wiring settings.

Figure 11 ACS8947T - Typical Closed Loop Transfer Function



Output Jitter

The output jitter meets all requirements of ITU, Telcordia and ETSI standards for SONET rates up to 622.08 MHz (OC-12/STM-4). See Electrical Specifications for details on the jitter figures across the different output jitter frequency bands relevant to each specification.

Device Reset

The RESETB pin is active low and requires a minimum reset pulse duration of 100 ms once the power supplies are stable and powered up. When the reset process is triggered, the required PLL settings are decoded from the configuration wiring connections, and the internal control logic waits for the presence of an input signal of approximately the correct frequency.

When a suitable input clock signal is detected, the ACS8947T calibrates the VCO using a fast tuning algorithm, and both frequency-lock and phase-lock to the input reference. This calibration routine is run only after a reset condition, so the RESETB pin should be held low until the input frequency is within 200 ppm of nominal.

Layout Recommendations

It is highly recommended that a stable and filtered 3.3 V power supply is used for the ACS8947T. A separate filtered power and ground plane is recommended, with supply decoupling capacitors of 10 nF and 100 pF utilizing good, high-frequency chip capacitors (0402 or 0603 format surface mount package) on each VDD.

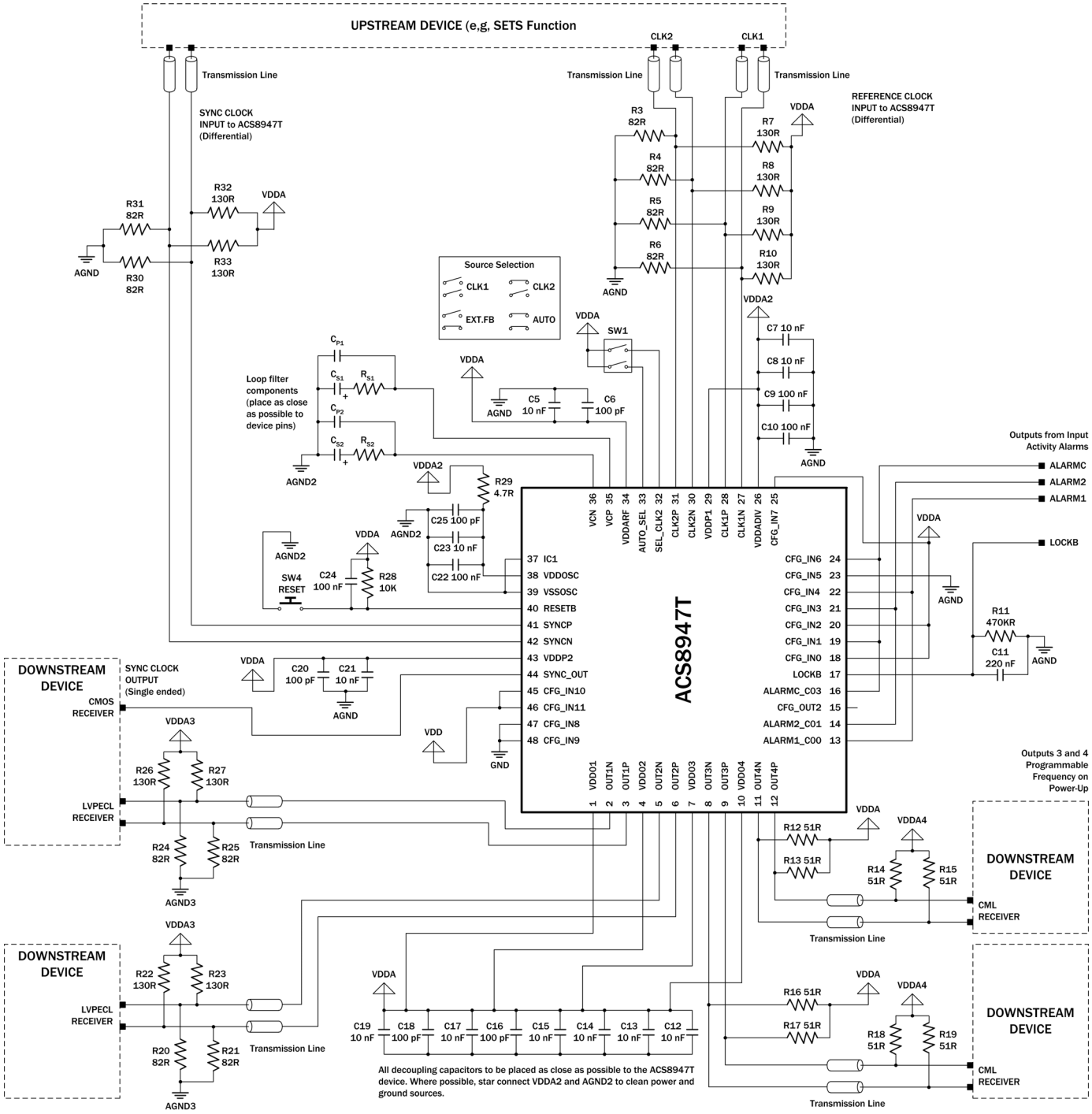
For optimum jitter cleaning performance, additional care should be taken over the supply connection to VDDOSC, which should be supplied directly from a 3.3 V LDO or a 4R7/68UF low-pass filter.

The wiring connections required for device configuration are calcuated by the ACS8947T Evaluation Software GUI. This program provides a schematic definition for the wired connections to CFG[11:0] and includes a loop filter component calculator.

Good differential signal layout on the input and output lines should be used to ensure matched track impedance and phase. Contact Semtech directly for further layout recommendations.

Example Schematic

Figure 12 Generic Line Card Clock Source with Protection - Example Schematic



Notes: (i) For configuration wiring information, refer to the ACS8947T evaluation software GUI.

(ii) For optimal performance, use a low voltage dropout (LDO) regulator to supply VDDA2.

Maximum Ratings

Important Note. The absolute maximum ratings given in Table 7 are stress ratings only, and functional operation of the device at conditions other than those indicated in Table 8 to Table 16 of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 7 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage (D.C.): VDD01, VDD02, VDD03, VDD04, VDDP1, VDDP2, VDDADIV, VDDARF, VDDOSC	V_{DD}	-0.5	3.6	V
Input voltage (non-supply pins): Digital Inputs: CFG_IN0, CFG_IN1, CFG_IN2, CFG_IN3, CFG_IN4, CFG_IN5, CFG_IN6, CFG_IN7, CFG_IN8, CFG_IN9, CFG_IN10, CFG_IN11, SELCLK2, AUTO_SEL, RESETB	V_{IN}	-0.5	5.5	V
Input voltage (non-supply pins) LVPECL Inputs: CLK1N, CLK1P, CLK2N, CLK2P, SYNCN, SYNCP ANALOG I/O: VCN, VCP, LOCKB	V_{IN}	-0.5	V_{DD} + 0.5	V
Output voltage (non-supply pins): Digital Output: ALARM1_C01, ALARM2_CO1, CFG_OUT2, ALARMC_CO3, SYNC_OUT LVPECL Outputs: OUT1N, OUT1P, to OUT 4N/P	V_{OUT}	-0.5	V_{DD} + 0.5	V
Ambient operating temperature range	T_A	-40	+85	°C
Storage temperature	T_{STOR}	-50	+150	°C
Reflow temperature (Pb)	T_{REPB}	-	+245	°C
Reflow temperature (Pb Free)	$T_{REPBFREE}$	-	+260	°C
ESD HBM (Human Body Model)[(i), (ii)]	ESD_{HBM}	2	-	kV
Latchup[(iii)]	I_{LU}	±100	-	mA

Notes: (i) All pins pass 2 kV HBM except VCN/VCP which are rated at 500 V HBM.

(ii) Tested to JEDEC standard JESD22-A114.

(iii) Tested to JEDEC standard JESD78.

Operating Conditions

Table 8 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage (DC): VDDP1, VDDP2, VDDADIV, VDDARF,	V_{DD}	3.135	3.3	3.465	V
Supply voltage (DC): VDDOSC	V_{DDOSC}	3.0	3.3	3.465	V
Supply voltage (DC): VDD01, VDD02, VDD03, VDD04. ** 3.135. V min required to enable output. Supply may be connected to 0 V to disable the associated output.*	V_{DD}	3.135 or 0 V*	3.3	3.465	V
Ambient temperature range	T_A	-40	-	+85	°C
VDD01 supply current	I_{DD01}	-	29	33	mA
VDD02 supply current	I_{DD02}		29	33	mA
VDD03 supply current	I_{DD03}		29	33	mA
VDD04 supply current	I_{DD04}		29	33	mA
VDDP1 supply current	I_{DDP1}		25	31	mA
VDDP2 supply current	I_{DDP2}		22	30	mA
VDDADIV supply current	I_{DDADIV}		100	111	mA
VDDARF supply current	I_{DDARF}		64	72	mA
VDDOSC supply current	I_{DDVOSC}		20	25	mA
Device total power dissipation with all outputs on @625 MHz. Excluding power dissipation in external biasing components.	P_{TOT}	-	1,1	1,2	W

Note...Supply currents for VDDOn assumes CML 50Ω termination.

Thermal Characteristics

Table 9 Thermal Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Thermal resistance junction to ambient	θ_{JA}	-	-	25	°C/W
Operating junction temperature	T_{JCT}	-	-	125	°C

AC Characteristics

Table 10 AC Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output to output skew(i)	t_{OSK}	-	-	100	ps
Input to output delay	t_{PDIO}	0.5	-	3.0	ns
SYNC_OUT to OUT1 delay	t_{PDSO}	-2.9	-	-0.4	ns
OUT1 to SYNC set-up	t_{SS}	3.7	-	-	ns
OUT1 to SYNC hold	t_{SH}	2.8	-	-	ns
Input clock rise/fall time(ii) (CLK1, CLK2, SYNC)	t_{CRF}	-	-	10	ns
LVPECL output rise/fall time(ii), (iii)	t_{PECLRF}	-	0.8	1.2	ns
CML output rise/fall time(ii), (iv)	t_{CMLRF}	-	0.7	1.2	ns
SYNC_OUT rise/fall time(ii), (v)	t_{SRF}	-	3.0	5.0	ns
Input clock duty cycle (CLK1, CLK2, SYNC)	t_{CDF}	40	50	60	%
Output clock duty cycle	t_{ODC}	48	50	52	%
RESETB pulse width after power-up	t_{RPW}	100	-	-	ms
Settling time before start of frequency tuning after RESETB high	t_{FT}	10	-	60	ms
Input reference frequency	F_{IN}	0.580	-	180	MHz
Output frequency	F_{OUT}	1.230		625	MHz

Notes: (i) Outputs running at same frequency.

(ii) Rise/fall time measured 10% to 90%.

(iii) Using output load specified in Figure 16.

(iv) Using output load specified in Figure 13.

(v) Using 50 Ω load.

(vi) Using 5 pF capacitive load.

DC Characteristics

Across all operating conditions, unless otherwise stated.

Table 11 VCN/VCP Differential Charge Pump Input/Output Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
Common mode voltage	V_{CM}	1.0	1.25	1.5	V
VCN/VCP linear tuning range	V_{TUNE}	-	±1.2	-	V
Low level output voltage	V_{OL}	GND + 0.2	-	-	V
High level output voltage	V_{OH}	-	-	VDD - 0.2	V
Output current (10 µA)	I_O	8	10	12	µA
Output current (40 µA)	I_O	32	40	48	µA
Output current (160 µA)	I_O	128	160	192	µA
Output current (210 µA)	I_O	168	210	252	µA

Table 12 DC Characteristics: LVCMOS Input Ports with Internal Pull-down/LVCMOS Schmitt Input Port with Internal Pull-up

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-down resistor	R_{PD}	43	-	108	kΩ
Pull-up resistor (Schmitt Input)	R_{PU}	53	-	113	kΩ
Input current	I_{IN}	-10	-	+10	µA

Table 13 DC Characteristics: LVPECL Input Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVPECL input offset voltage differential inputs (Note (ii))	V_{IO_LVPECL}	V_{DD}-2.0	-	V_{DD}-0.5	V
Input differential voltage	V_{ID_LVPECL}	0.1	-	1.4	V
LVPECL input low voltage single-ended input (Note (i))	$V_{IL\_LVPECL\_S}$	V_{SS}	-	V_{DD}-1.5	V
LVPECL input high voltage single-ended input (Note (i))	$V_{IL\_LVPECL\_S}$	V_{DD}-1.3	-	V_{DD}	V
Input high current input differential voltage V_{ID} = 1.4 V	I_{IH_LVPECL}	-10	-	+10	µA
Input low current input differential voltage V_{ID} = 1.4 V	I_{IL_LVPECL}	-10	-	+10	µA

Notes: (i) Unused differential input terminated to VDD-1.4 V.

(ii) Both pins must remain within the supply voltage, i.e. >V_{SS} and <V_{DD}.

Table 14 DC Characteristics: CML Output Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
I_{OUT} current source	I_{OUT}	13.3	16	19.2	mA
Single-ended output voltage amplitude with 50 Ω load to V_{DD} and 50 Ω input impedance into next stage.	V_{OS}	-	400	-	mV
Differential output voltage amplitude with 50 Ω load to VDD and 50 Ω input impedance into next stage on both pins.	V_{OD}	-	800	-	mV

Table 15 DC Characteristics: LVPECL Output Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVPECL output low voltage (Note (i))	V_{OL_LVPECL}	V_{DD}-2.1	-	V_{DD}-1.62	V
LVPECL output high voltage (Note (i))	V_{OH_LVPECL}	V_{DD}-1.45	-	V_{DD}-0.88	V
LVPECL output differential voltage (Note (i))	V_{OD_LVPECL}	0.37	-	1.22	V

Note: (i) With a 50 ohms load on each pin to V_{DD} -2V

Table 16 DC Characteristics: LVTTL/CMOS Output Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output low voltage @ I_{OL} (MAX)	V_{OL}	-	-	0.4	V
Output high voltage @ I_{OH} (MIN)	V_{OH}	2.4	-	-	V
Low level output current @ V_{OL} = 0.4 V	I_{OL}	2	-	-	mA
High level output current @ V_{OH} = 2.4 V	I_{OH}	2	-	-	mA

Input and Output Interface Terminations

Interfacing to either the same type or electrically different interface types is illustrated by the following circuit diagrams in Figure 13 to Figure 18.

In applications where the output clocks are always running, they may be AC coupled, allowing the receive end to be at any common mode voltage, however, the lines must always be terminated at their characteristic impedance.

The preferred termination for the CML type output is 50 Ω to VDD, as shown in Figure 13. AC coupling may be used subsequently to translate the levels to other interface types, e.g. to LVPECL/LVDS as shown in Figure 14.

The example of Figure 16 shows LVPECL to LVPECL terminations with DC coupling, so that the ACS8947T sees an equivalent load of around 50 Ω from the resistor arrangement at the receiver end. Note that signal levels given in the accompanying graph are nominal levels at 622.08 MHz, and will change with load.

The preferred termination circuitry for the LVDS signals between the ACS8525/26/27 and the ACS8947T LVPECL is shown in Figure 18. The bias for the LVPECL input is set for AC inputs at a mid point of approximately 2 V (with VDD of 3.3 V), as opposed to a normal DC coupled bias of VDD - 2 V. This is due to the push-pull nature of an AC coupled signal.

Where inputs to the ACS8947T are AC coupled, problems may be experienced with activity detection. This is due to noise/cross-talk on the inputs being interpreted as activity. To avoid this, DC couple wherever possible and, if AC coupling must be used, consider offsetting the DC bias of the N and P signals. See Figure 15.

Figure 13 CML Output - DC Coupled to CML Receiver

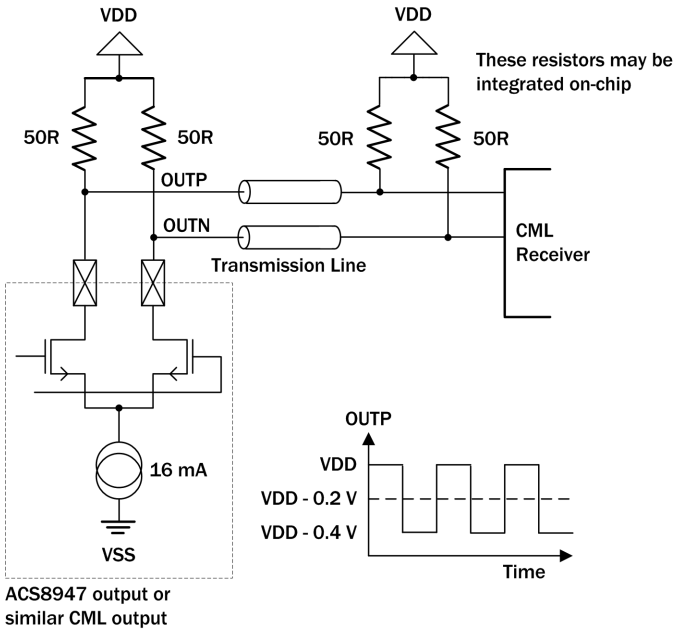
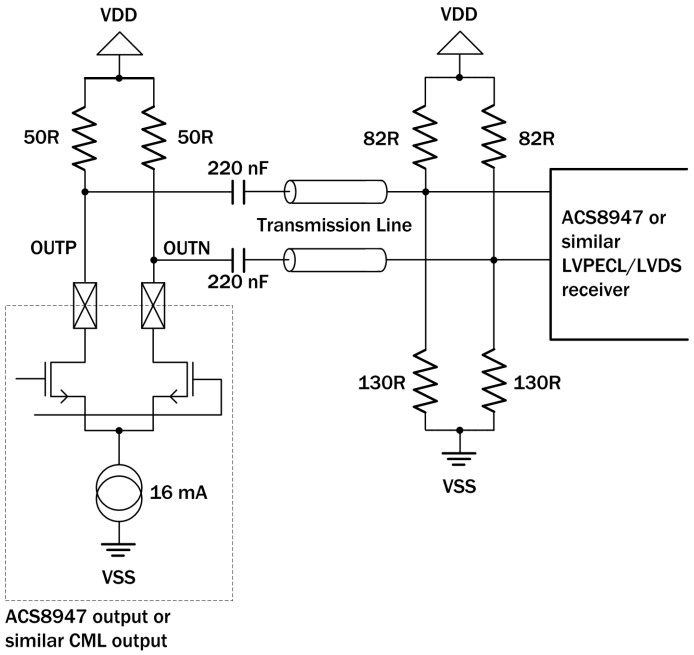


Figure 15 Generic CML Output AC Coupled to LVPECL Receiver



130/120R mismatch is used in the input bias network in Figure 15 to emulate a simplified differential Schmitt trigger, reducing the susceptibility to input noise when no input is connected.

Figure 14 JAM PLL CML Output DC coupled to LVPECL or LVDS Receiver

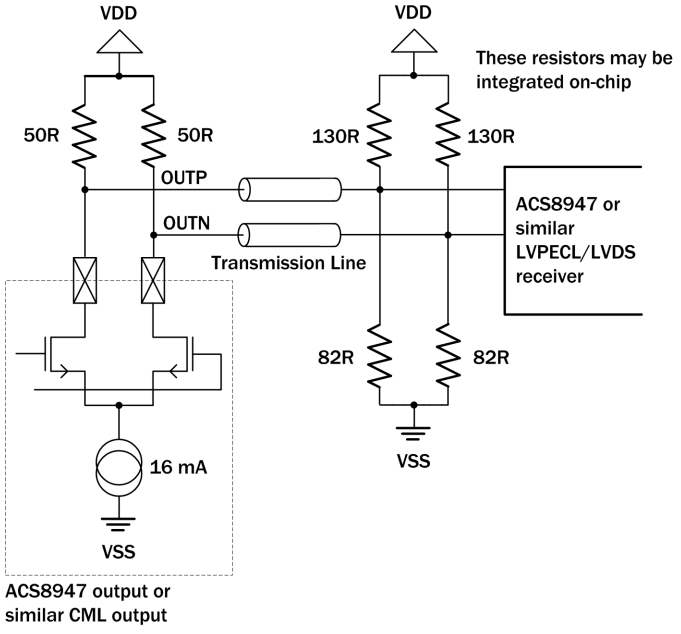


Figure 16 LVPECL Output - DC Coupled to LVPECL or LVDS Receiver

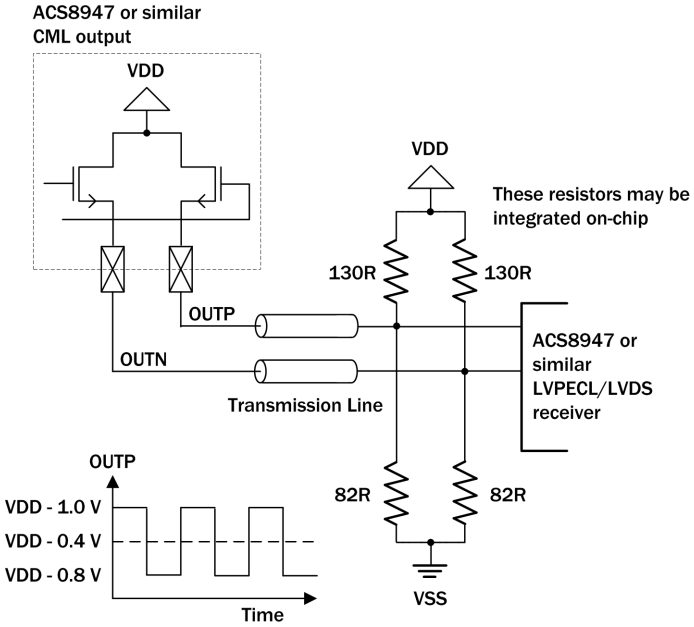


Figure 17 SETS LVDS Output - DC Coupled to LVPECL Receiver

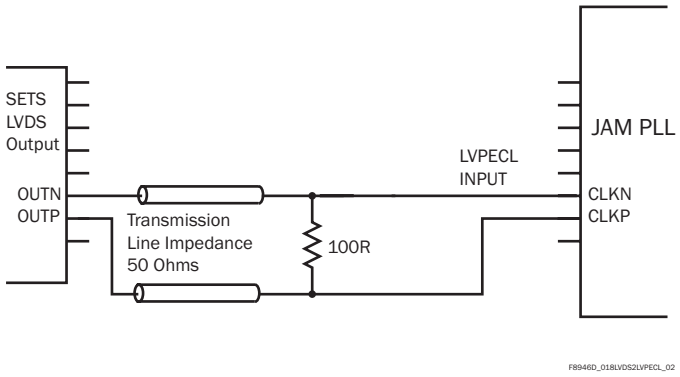
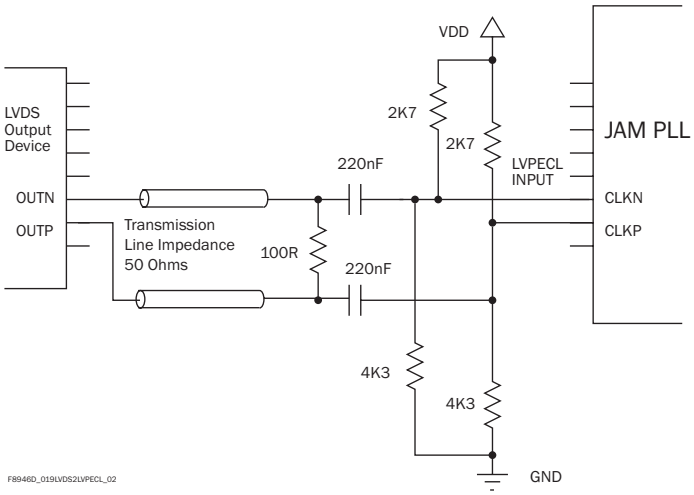


Figure 18 Generic LVDS - AC Coupled to LVPECL Receiver



Note...Activity monitors will not function with this scheme as noise may cause activity detection by mistake. Consider replacing one 4K3 resistor with a 4k7 resistor.

Jitter Performance

Table 17 Phase Noise Parameters with LVPECL Input of 167 MHz and LVPECL Output of 167 MHz

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Phase noise at 100 Hz	phn_{100}	-	-64	-	dBc/Hz
Phase noise at 1 kHz	phn_{1k}	-	-75	-	dBc/Hz
Phase noise at 10 kHz	phn_{10k}	-	-91	-	dBc/Hz
Phase noise at 100 kHz	phn_{100k}	-	-120	-	dBc/Hz
Phase noise at 1 MHz	phn_{1M}	-	-142	-	dBc/Hz
Phase noise at 10 MHz	phn_{10M}	-	-142	-	dBc/Hz
Phase noise at 20 MHz	phn_{20M}	-	-142	-	dBc/Hz
RMS jitter integrated from 12 kHz to 20 MHz	J_{RMS}	-	5.1	-	ps
Total jitter	Tj	-	138	-	ps

Notes: (i) Phase noise specifications when f_{in} = 10 MHz and f_{out} = 100 MHz.
(ii) PLL closed loop bandwidth set to 2 kHz with a damping factor of 3.8.
(iii) Total jitter is broadband jitter accumulated over 100 s.

Table 18 Phase Noise Parameters with LVPECL Input of 25 MHz and LVPECL Output of 625 MHz

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Phase noise at 100 Hz	phn_{100}	-	-60	-	dBc/Hz
Phase noise at 1 kHz	phn_{1k}	-	-68	-	dBc/Hz
Phase noise at 10 kHz	phn_{10k}	-	-79	-	dBc/Hz
Phase noise at 100 kHz	phn_{100k}	-	-110	-	dBc/Hz
Phase noise at 1 MHz	phn_{1M}	-	-135	-	dBc/Hz
Phase noise at 10 MHz	phn_{10M}	-	-142	-	dBc/Hz
Phase noise at 20 MHz	phn_{20M}	-	-142	-	dBc/Hz
RMS jitter integrated from 12 kHz to 20 MHz	J_{RMS}	-	4.3	-	ps
Total jitter	Tj	-	198	-	ps

Notes: (i) Phase noise specifications when f_{in} = 25 MHz and f_{out} = 625 MHz.
(ii) PLL closed loop bandwidth set to 2 kHz with a damping factor of 1.2.
(iii) Total jitter is broadband jitter accumulated over 100 s.

Table 19 Phase Noise Parameters with LVPECL Input of 62.5 MHz and LVPECL Output of 125 MHz

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Phase noise at 100 Hz	phn_{100}	-	-71	-	dBc/Hz
Phase noise at 1 kHz	phn_{1k}	-	-75	-	dBc/Hz
Phase noise at 10 kHz	phn_{10k}	-	-93	-	dBc/Hz
Phase noise at 100 kHz	phn_{100k}	-	-124	-	dBc/Hz
Phase noise at 1 MHz	phn_{1M}	-	-140	-	dBc/Hz
Phase noise at 10 MHz	phn_{10M}	-	-142	-	dBc/Hz
Phase noise at 20 MHz	phn_{20M}	-	-142	-	dBc/Hz
RMS jitter integrated from 12 kHz to 20 MHz	J_{RMS}	-	4.6	-	ps
Total jitter	Tj	-	149	-	ps

Notes: (i) Phase noise specifications when f_{in} = 62.5 MHz and f_{out} = 125 MHz.
(ii) PLL closed loop bandwidth set to 2 kHz with a damping factor of 1.2.
(iii) Total jitter is broadband jitter accumulated over 100 s.

Table 20 Phase Noise Parameters with LVPECL Input of 19.44 MHz and LVPECL Output of 622.08 MHz

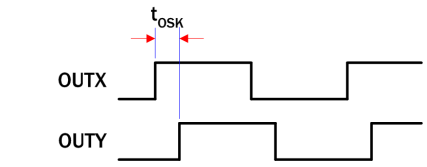
Parameter	Symbol	Minimum	Typical	Maximum	Unit
Phase noise at 100 Hz	phn_{100}	-	-57	-	dBc/Hz
Phase noise at 1 kHz	phn_{1k}	-	-66	-	dBc/Hz
Phase noise at 10 kHz	phn_{10k}	-	-79	-	dBc/Hz
Phase noise at 100 kHz	phn_{100k}	-	-110	-	dBc/Hz
Phase noise at 1 MHz	phn_{1M}	-	-135	-	dBc/Hz
Phase noise at 10 MHz	phn_{10M}	-	-142	-	dBc/Hz
Phase noise at 20 MHz	phn_{20M}	-	-142	-	dBc/Hz
RMS jitter integrated from 12 kHz to 20 MHz	J_{RMS}	-	4.3	-	ps
Total jitter	Tj	-	194	-	ps

Notes: (i) Phase noise specifications when f_{in} = 19.44 MHz and f_{out} = 622.08 MHz.
(ii) PLL closed loop bandwidth set to 2 kHz with a damping factor of 1.2.
(iii) Total jitter is broadband jitter accumulated over 100 s.

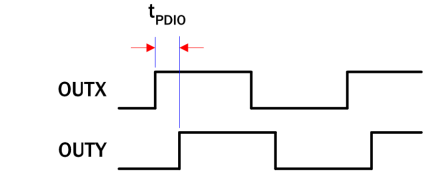
Input/Output Timing

Figure 19 Timing Diagrams

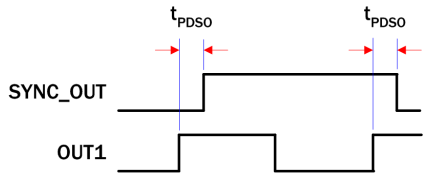
1 Output to output clock skew



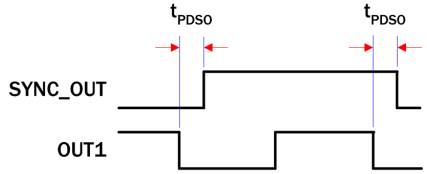
2 Input to output delay



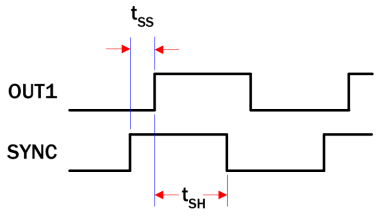
3a SYNC_OUT to OUT_1 delay
(OUT_1 rising edge aligned)



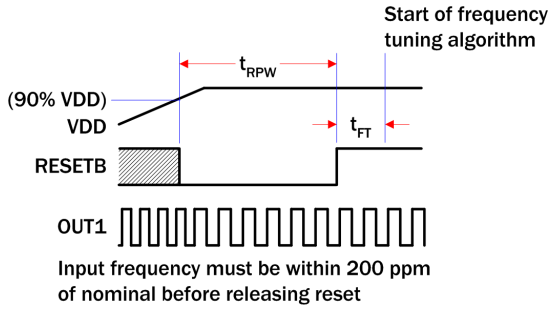
3b SYNC_OUT to OUT_1 delay
(OUT_1 falling edge aligned)



4 CLK to SYNC SETUP and HOLD

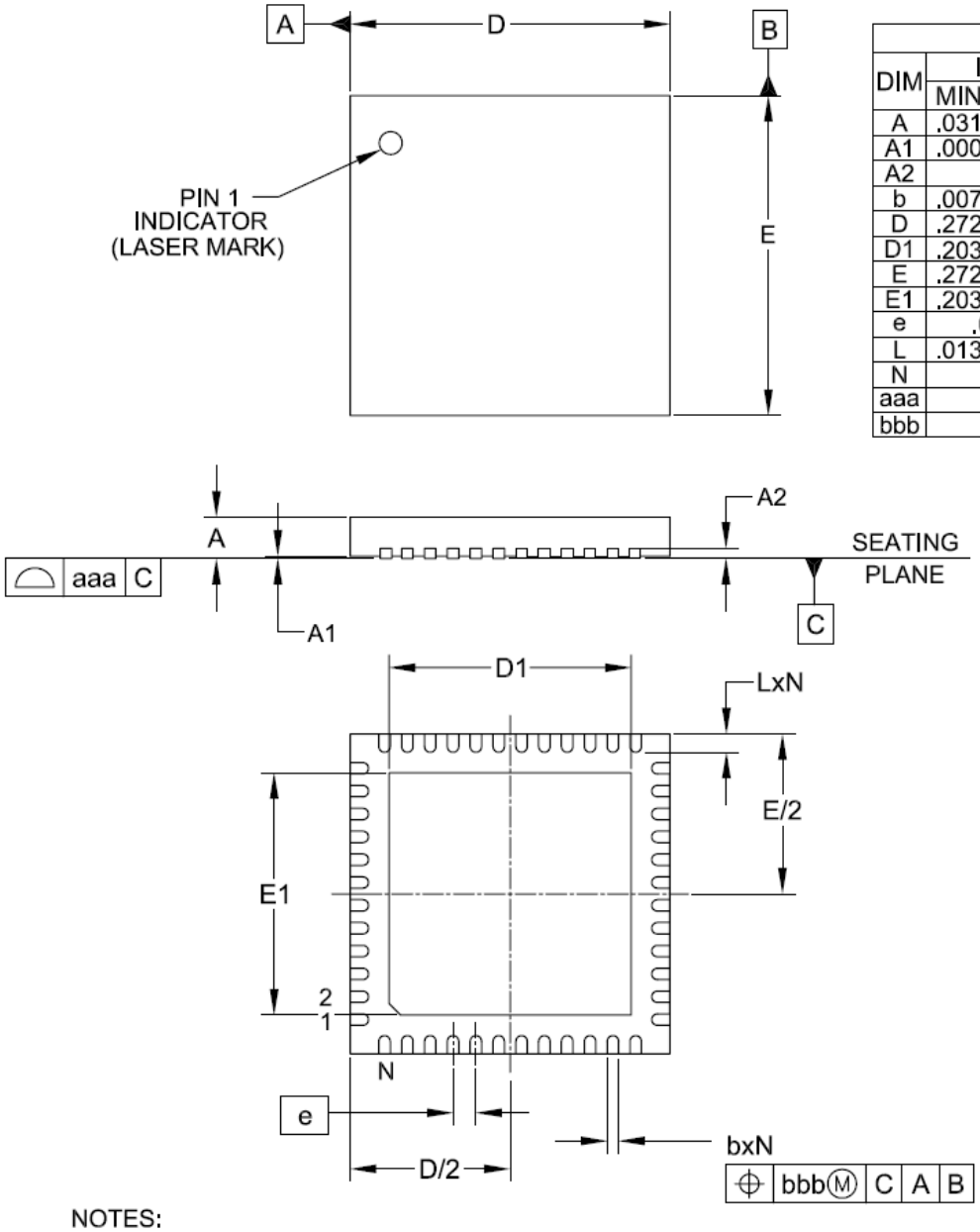


5 Power-up sequence



Package Information

Figure 20 QFN48 Package.



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2		(.008)			(0.20)	
b	.007	.009	.012	0.18	0.23	0.30
D	.272	.276	.280	6.90	7.00	7.10
D1	.203	.209	.213	5.15	5.30	5.40
E	.272	.276	.280	6.90	7.00	7.10
E1	.203	.209	.213	5.15	5.30	5.40
e		.020 BSC			0.50 BSC	
L	.013	.016	.018	0.35	0.40	0.45
N		48			48	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

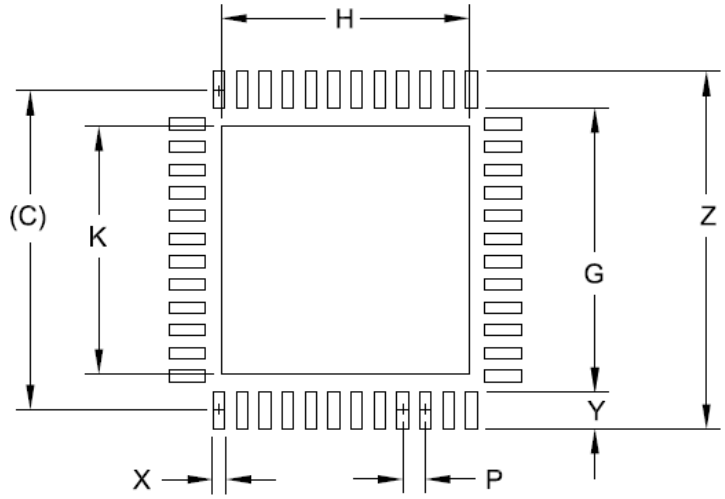
Thermal Conditions

The device is rated for full temperature range when this package is used with a 4-layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

As the device includes a large thermal die paddle ground connection which must be soldered to the PCB in addition to the pins, giving improved pull-off strength and thermal dissipation characteristics as well as the necessary grounding.

Although not essential for the ACS8947T, one technique that may be used to improve heat dissipation from through the large centre pad is to include a thermal landing the same size as the centre pad on the component side of the board (and one on the opposite side of the PCB) connected to analog ground using a number of thermal vias, approximately 0.33 mm diameter. These vias should be completely connected (flooded over) to the thermal landing(s) as well as to internal ground planes if using a multi-layer PCB. 3 x 3 vias pitched at 1.27 mm between via centres would be more than sufficient for the ACS8947T if this method were adopted.

Figure 21 Typical 48 Pin QFN PCB Footprint



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.274)	(6.95)
G	.240	6.10
H	.213	5.40
K	.213	5.40
P	.021	0.50
X	.010	0.25
Y	.033	0.85
Z	.307	7.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
3. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

Abbreviations

CML	Current Mode Logic
CMU	Clock Multiplier Unit
ESD	Electrostatic Discharge
ESR	Effective Series Resistance
HBM	Human Body Model
I/O	Input - Output
JAM PLL	Jitter Attenuating, Multiplying Phase Locked Loop
GbE	Gigabit Ethernet
JAM PLL	Jitter Attenuating, Multiplying PLL
LC/P	Line Card Protection
LDO	Low Voltage Drop-out
LVDS	Low Voltage Differential Signal
LVPECL	Low Voltage (3.3 V) PECL
OC-3/12/48	Optical Carrier Signal Level 3/12/48 155.52 Mbps/ 622.08 Mbps/ 2.488 Gbps
PECL	Positive Emitter Coupled Logic
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
POR	Power-On Reset
p-p	peak-to-peak
rms	root-mean-square
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing source
SONET	Synchronous Optical Network
STM-1/4/16	Synchronous Transport Module Levels 1/4/16: 155.52 Mbps/ 622.08 Mbps 2.488 Gbps (SDH)
STS-12/48	Synchronous Transport Signal Level: 12/48, 622.08 Mbps/2.488 Gbps (SONET)
UI	Unit Interval
uP (µP)	Microprocessor
VCO	Voltage Controlled Oscillator
WEEE	Waste Electrical and Electronic Equipment (directive)

References and Related Standards

[1] EN 300 462-7-1 v1.1.2 (06/2001)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 7-1: Timing characteristics of slave clocks suitable for synchronization supply to equipment in local node applications

[2] ETSI EN 302 084 V1.1.1 (2000-02)
Transmission and Multiplexing (TM); The control of jitter and wander in transport networks

[3] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

[4] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC)

[5] ITU-T G.823 (03/2000)
The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

[6] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

[7] ITU-T G.825 (03/2000)
The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH)

[8] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

[9] Telcordia GR-499-CORE, Issue 2 (12/1998)
Transport Systems Generic Requirements (TSGR) Common requirements

[10] Telcordia GR-1244-CORE, Issue 2 (12/2000)
Clocks for the Synchronized Network: Common Generic Criteria

[11] RoHS Directive 2002/95/EC: Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

[12] Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC): Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

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Revision Status/History

The Revision Status, as shown in top center of the datasheet header bar, may be DRAFT, PRELIMINARY, or FINAL, and refers to the status of the device (not the datasheet), within the design cycle. DRAFT status is used when the design is being realized but is not yet physically available, and the datasheet content reflects the intention of the design. The datasheet is raised to PRELIMINARY status when initial prototype devices are physically available, and the datasheet content more accurately represents the realization of the design. The datasheet is only raised to FINAL status after the device has been fully characterized, and the datasheet content updated with measured, rather than simulated parameter values.

This is the FINAL release of the ACS8947T datasheet. The changes made for this revision are given in Table 21.

Table 21 Revision History

Revision	Reference	Description of Changes
Rev. 1.00/September 2007	All Pages	First revision of FINAL release of ACS8947T datasheet.

Ordering Information

Table 22 Parts List

Part Number	Description
ACS8947T	Lead (Pb)-free packaged version of ACS8947T.

Disclaimers

Life support - this product is not designed or intended for use in life support equipment, devices or systems, or other critical applications, and is not authorized or warranted for such use.

Right to change - changes may be made to this product without notice. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards - operation of this device is subject to the user's implementation and design practices. It is the responsibility of users to ensure that equipment using this device is compliant to all relevant standards.

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