General Description

The MAX4987AE/MAX4987BE are overvoltage protection

devices with built-in ESD protection for USB data lines.

These devices feature a low $100m\Omega$ (typ) RON internal

nFET switch and protect low-voltage systems against voltage faults up to +28V. When the input voltage exceeds

the overvoltage threshold or decreases below the under-

voltage threshold, the internal nFET switch is turned off to

All switches feature a minimum 1.5A current-limit pro-

tection. During a short-circuit occurrence, the switch

operates in an autoretry mode where the internal nFET

switch is turned on to check if the fault has been

removed. The autoretry interval is 30ms, and if the fault

The MAX4987AE/MAX4987BE feature low-capacitance

(3pF) ESD protection for USB data lines that allow

The overvoltage threshold (OVLO) is preset to 6.15V. The undervoltage thresholds (UVLO) are preset to 2.55V

(MAX4987AE) or 4.2V (MAX4987BE). When the input

voltage drops below the undervoltage (UVLO) thresh-

old, the devices enter a low-current standby mode. All devices are offered in a small 2mm x 3mm, 8-pin TDFN package and operate over the -40°C to +85°C

prevent damage to the protected components.

is removed, the nFET switch remains on.

extended temperature range.

Cell Phones Media Players

transmission of high-speed USB 2.0 signals.

Features

- Input Voltage Protection Up to +28V
- Integrated Low RON (100mΩ) nFET Switch
- Internal Overcurrent Protection 1.5A (min)
- Overcurrent Protection (Autoretry)
- Enable Input
- Internal 30ms Startup Delay
- Low-Capacitance USB High-Speed Data Line ESD Protection (3pF) ±15kV Human Body Model
 - ±15kV IEC 61000-4-2 Air Gap ±6kV IEC 61000-4-2 Contact
- Thermal-Shutdown Protection
- 2mm x 3mm, 8-Pin TDFN Package

Pin Configuration



Ordering Information/Selector Guide

PART	PIN- PACKAGE	TOP MARK	PACKAGE CODE	UVLO (V)	OVLO (V)	OVERCURRENT MODE
MAX4987AEETA+	8 TDFN-EP**	AAI	T823-1	2.55	6.15	Autoretry
MAX4987BEETA+*	8 TDFN-EP**	AAJ	T823-1	4.2	6.15	Autoretry

Note: All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes a lead-free package.

*Future product—contact factory for availability.

**EP = Exposed paddle.

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

____Applications

Typical Operating Circuit appears at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

IN0.3V to +30	VC
OUT0.3V to +(IN + 0.3	V)
V _{CC} , EN, ACOK, CD+, CD0.3V to +6	δÝ
Continuous Power Dissipation ($T_A = +70^{\circ}C$) for multilayer boar	rd:
8-Pin TDFN (derate 16.7mW/°C above +70°C)	W
Package Junction-to-Ambient Thermal Resistance	
(θ _{JA}) (Note 1)60.0°C/	W
Continuous Power Dissipation (T _A = +70°C) for multilayer boar 8-Pin TDFN (derate 16.7mW/°C above +70°C)1333m Package Junction-to-Ambient Thermal Resistance	rd: iW

Package Junction-to-Case Thermal Resistance	
(θ _{JC}) (Note 1)	10.8°C/W
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	
Lead Temperature (soldering)	+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, go to <u>www.maxim-ic.com/thermal-tutorial</u>.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{IN} = +2.2V \text{ to } +28V, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } V_{IN} = +5V \text{ and } T_A = +25^{\circ}\text{C}.)$

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNIT
ANALOG SWITCH							
Input-Voltage Range	VIN			2.2		28	V
V _{CC} Input Voltage	Vcc					5.5	V
lenget Supply Coursest		$\overline{EN} = 0V, V_{IN} > V_{L}$	IVLO		60	150	
Input Supply Current	IIN	$\overline{\text{EN}} = 5\text{V}, \text{V}_{\text{IN}} > \text{V}_{\text{L}}$	JVLO		50	100	μA
UVLO Supply Current	IUVLO	VIN < VUVLO				40	μΑ
			MAX4987AE	2.3			
		(V _{IN} falling)	MAX4987BE	3.8			
IN Undervoltage Lockout	Vuvlo		MAX4987AE	2.35	2.55	2.75	V
		(V _{IN} rising)	MAX4987BE	3.85	4.2	4.45	
IN Undervoltage Lockout Hysteresis					1		%
	Vovlo	(V _{IN} rising)		5.55	6.15	6.45	V
Overvoltage Trip Level		(V _{IN} falling)		5.5			
IN Overvoltage Lockout Hysteresis					1		%
Switch On-Resistance	Ron	$V_{IN} = 5V, I_{OUT} = 5$	500mA		100	200	mΩ
Overcurrent Protection Threshold	ILIM			1.5		4.2	А
Maximum Output Capacitance		VIN = 5V, no over	current shutdown		1000		μF
CD+ and CD- Leakage Current	ILKG_CD	V _{CC} = 5.5V, V _{CD}	= 0V, 3.3V	-300		+300	nA
CD+ and CD- Capacitance	CCD	$f = 1MHz, V_{CD} =$	0.5p-p		3		рF
DIGITAL SIGNALS							
ACOK Output Low Voltage	Vol	I _{SINK} = 1mA				0.4	V
ACOK High-Leakage Current		$V_{\overline{ACOK}} = 5.5V$, flag deasserted				1	μA
EN Input-Voltage High	VIH			1.4			V
EN Input-Voltage Low	VIL					0.4	V
EN Input-Leakage Current	I _{LEAK}	V _{EN} = 5.5V		-1		+1	μA

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{IN} = +2.2V \text{ to } +28V, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } V_{IN} = +5V \text{ and } T_A = +25^{\circ}\text{C}.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNIT
TIMING CHARACTERISTICS (Note	e 2)					
Debounce Time	^t INDBC	Time from V _{UVLO} < V _{IN} < V _{OVLO} to charge-pump enable		30		ms
ACOK Assertion Time	TACOK	$V_{UVLO} < V_{IN} < V_{OVLO}$, to \overline{ACOK} low		30		ms
Switch Turn-On Time	ton	$V_{UVLO} < V_{IN} < V_{OVLO}, R_{LOAD} = 100\Omega,$ from 10% to 90% of V_{OUT}		3		ms
Switch Turn-Off Time	tOFF	$V_{IN} < V_{UVLO}$ or $V_{IN} > V_{OVLO}$ to internal switch off, $R_{LOAD} = 100\Omega$	10		10	μs
Current-Limit Turn-Off Time	^t BLANK	Overcurrent fault to internal switch off	10			μs
Autoretry Time	utoretry Time tRETRY From		30			ms
THERMAL PROTECTION			•			
Thermal Shutdown	T _{SHDN}			150		°C
Thermal-Shutdown Hysteresis				40		°C
ESD PROTECTION						
		Human Body Model		±15		
CD+ and CD-		IEC 61000-4-2 Air Gap		±15		kV
		IEC 61000-4-2 Contact		±6		
All Other Pins		Human Body Model		±2		kV

Note 2: All timing is specified using 20% and 80% levels, unless otherwise noted.

Typical Operating Characteristics

 $(T_A = +25^{\circ}C, unless otherwise noted.)$





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Pin Description

PIN	NAME	FUNCTION
1	IN	Voltage Input. Bypass IN with a 1μ F ceramic capacitor as close to the device as possible to obtain ± 15 kV HBM ESD protection. No capacitor required to obtain ± 2 kV HBM ESD protection.
2	CD+	USB Data Line
3	GND	Ground
4	CD-	USB Data Line
5	V _{CC}	Positive Supply-Voltage Input. V _{CC} is required only when USB signals are present.
6	ĒN	Enable Active-Low Input. Drive \overline{EN} low to enable the switch. Drive \overline{EN} high to disable the switch.
7	ACOK	Open-Drain Adapter-Voltage Indicator Output. ACOK is driven low after the V _{IN} voltage is stable between UVLO and OVLO for 30ms (typ). Connect a pullup resistor from ACOK to the logic I/O voltage of the host system.
8	OUT	Output Voltage. Output of internal switch.
EP	EP	Exposed Pad. Connect exposed pad to ground. Do not use EP as a sole ground connection.

Functional Diagram





Figure 1. MAX4987AE/MAX4987BE Timing Diagram

Detailed Description

The MAX4987AE/MAX4987BE are overvoltage protection devices with integrated ESD protection for USB data lines. These devices feature a low R_{ON} internal FET and protect low-voltage systems against voltage faults up to +28V. If the input voltage exceeds the overvoltage threshold, the internal nFET switch is turned off to prevent damage to the protected components. The 30ms debounce time prevents false turn-on of the internal nFET switch during startup. An open-drain activelow logic output is available to signal that a successful power-up has occurred.

Device Operation

The MAX4987AE/MAX4987BE have an internal oscillator and charge pump that control the turn-on of the internal nFET switch. The internal oscillator controls the timers that enable the turn-on of the charge pump and controls the state of the open-drain ACOK output. If V_{IN} < V_{UVLO} or if V_{IN} > V_{OVLO}, the internal oscillator remains off, thus disabling the charge pump. If V_{UVLO} < V_{IN} < V_{OVLO}, the internal charge pump is enabled. The charge-pump startup, after a 30ms internal delay, turns on the internal nFET switch and asserts ACOK (see Figure 1). At any time, if V_{IN} drops below V_{UVLO} or rises above V_{OVLO}, ACOK is pulled high and the charge pump is disabled.

Internal nFET Switch

The MAX4987AE/MAX4987BE incorporate an internal nFET switch with a 100m Ω (typ) on-resistance. The nFET switch is internally driven by a charge pump that generates a voltage above the input voltage. The MAX4987AE/MAX4987BE is equipped with a 1.5A (min) current-limit protection that turns off the nFET switch within 5µs (typ) during an overcurrent fault condition.

Autoretry

The MAX4987AE/MAX4987BE have an overcurrent autoretry function that turns on the nFET switch again after a 30ms (typ) retry time (see Figure 2). If the faulty load condition is still present after the blanking time, the switch turns off again and the cycle is repeated. The fast turn-off time and 30ms retry time result in a very low duty cycle in order to keep power consumption low. If the faulty load condition is not present, the switch remains on.

Undervoltage Lockout (UVLO)

The MAX4987AE has a 2.55V undervoltage-lockout threshold (UVLO), while the MAX4987BE has a 4.15V UVLO threshold. When V_{IN} is less than V_{UVLO}, $\overrightarrow{\text{ACOK}}$ is high impedance.



Overvoltage Lockout (OVLO)

The MAX4987AE/MAX4987BE have a 6.15V (typ) overvoltage threshold (OVLO). When V_{IN} is greater than V_{OVLO} , ACOK is high impedance.

ACOK

 $\overline{\text{ACOK}}$ is an active-low open-drain output that asserts low when VUVLO < VIN < VOVLO following the 30ms (typ) debounce period. Connect a pullup resistor from $\overline{\text{ACOK}}$ to the logic I/O voltage of the host system. During a short-circuit fault, $\overline{\text{ACOK}}$ may deassert due to VIN not being in the valid operating voltage range.

Thermal-Shutdown Protection

The MAX4987AE/MAX4987BE feature thermal-shutdown circuitry. The internal nFET switch turns off when the junction temperature exceeds T_{SHDN} and immediately goes into a fault mode. The device exits thermal shutdown after the junction temperature cools by +40°C (typ).

Applications Information

IN Bypass Capacitor

For most applications, bypass IN to GND with a 1 μ F ceramic capacitor as close to the device as possible to enable ±15kV HBM ESD protection on IN. If ±15kV HBM ESD protection is not required, there is no capacitor required at IN. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the absolute maximum rating on IN.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4987AE/MAX4987BE are specified for ± 15 kV HBM ESD protection on the CD+, CD-, and IN pins when IN is bypassed to ground with a 1µF ceramic capacitor. The CD+ and CD- inputs are also protected against ± 15 kV Air Gap and ± 6 kV contact IEC 61000-4-2 ESD events.

Human Body Model

Figure 3 shows the Human Body Model, and Figure 4 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, that is then discharged into the device through a $1.5 k\Omega$ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX4987AE/ MAX4987BE



Figure 2. Autoretry Timing Diagram



Figure 3. Human Body ESD Test Model



Figure 4. Human Body Current Waveform

are specified for ±15kV Air-Gap Discharge and ±6kV Contact Discharge IEC 61000-4-2 on the CD+ and CDpins.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2, due to lower series resistance. Hence, the ESD withstand voltage measured to IEC 61000-4-2 generally is lower than that measured using the Human Body Model. Figure 5 shows the IEC 61000-4-2 model. The Contact Discharge method connects the probe to the device before the probe is charged. The Air-Gap Discharge test involves approaching the device with a charged probe.



Figure 5. IEC 61000-4-2 ESD Test Model





Chip Information

PROCESS: BICMOS

MAX4987AE/MAX4987BE

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

	C	IMENSION	IS				
SYMBOL	MIN.	NOM.	MAX.				
А	0.70	0.70 0.75 0.80					
E	2.95	2.95 3.00 3.05					
D	1.95	1.95 2.00 2.05					
A1	0.00	0.00 0.02 0.05					
L	0.30						
k	0.20 MIN.						
A2		0.20 REF.					
Ν	8						
е	0.50 BSC						
b	0.18	0.18 0.25 0.30					

	EXPOSED PAD PACKAGE							
PKG.	E2			D2				
CODE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T823-1	1.60	1.75	1.90	1.50	1.63	1.75		

NOTES:

-DRAWING NOT

MAX4987AE/MAX4987BE

- NOTES:
 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
 3. WARPAGE SHALL NOT EXCEED 0.10mm.
 4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
 5. COMPLY TO JEDEC M0229, TYPE 1, VERSION WCED-2.
 6. "N" IS THE TOTAL NUMBER OF LEADS.
 7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
 8. MARFRIAI MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC #10-013

- 9. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC #10-0131.

		\$ <i>/N/</i> JX		M
	^{TITLE} PACKAGE 8L TDFN, E	OUTLINE XPOSED PAD, 2x3x0.8mn	n	
TD SCALE-	APPROVAL	DICUMENT CONTROL NO. 21-0174	rev. B	2/2

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