NX2A4WP

A4WP compliant high frequency wireless charging receiver front end

Rev. 3 — 4 August 2015 Product short data sheet

1. General description

The NX2A4WP is an A4WP (Alliance for Wireless Power) compliant wireless power receiver front end. It contains a high-voltage, highly efficient rectifier, integrated LDOs, a D3C-to-DC converter, a multi-channel 12-bit ADC, four GPIOs and a Fast-Mode I^2C-bus interface. The integrated rectifier supports voltages of up to 20 V and is protected by an integrated automatic clamping function and an automatic over-power protection function. The DC-to-DC regulator delivers a nominal voltage of 5 V. The host microcontroller configures the on-chip controller for automatic interrupt-driven system control.
The controller reads the rectifier output voltage, current level information, junction temperature and external temperature sensor information from the ADC. It controls the DC-to-DC converter as well as the GPIOs.

2. Features and benefits

- 25 V tolerant antenna input pins
- Automatic over-voltage protection of the antenna inputs
- 6.78 MHz compatible integrated rectifier
- High efficiency with an active rectifier and a DC-to-DC converter
- Integrated LDOs (1.8 V and 3.3 V up to 100 mA) with auto enable and discharge path
- Integrated DC-to-DC buck regulator with 5 V, 1.2 A output
- Multi-channel 12-bit ADC subsystem
- Temperature sensor (NTC) analog interface
- USB bus power supply detection
- 400 kHz I^2C-bus slave interface
- Software and power-on reset of the on-chip digital controller
- Programmable rectifier modes: active, half-active and passive
- 2 digital General Purpose Input and Output ports (GPIOs) with open-drain outputs and up to 60 V tolerance for control and communication applications
- 2 digital General Purpose Input and Output ports (GPIOs) with open-drain outputs and 25 V tolerance for control and communication applications
- Protection circuitry
  - Automatic over-power protection
  - Automatic AC short to ground for OVP option
  - Automatic DC-to-DC over-voltage protection lock out option
  - Over-temperature protection
  - Over-voltage protection
  - Under-voltage protection

- Under-voltage lockout (for LDOs and DC-to-DC controller)
- Specified from −40 °C to +85 °C ambient temperature
- 3.56 × 3.41 mm WLCSP with 0.5 mm pitch

3. Applications

- Portable electronic devices with integrated wireless charging / wireless power RX capabilities according to the A4WP standard

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NX2A4WP	NX2A4WP	WLCSP42	Wafer level chip-scale package; 42 bumps; 3.56 × 3.41 × 0.57 mm (back side coating included)	NX2A4WP

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
NX2A4WP	NX2A4WPZ	WLCSP42	Reel 7” Q1/T1 *Standard mark chips DP	2000	−40 °C to +85 °C

5. Block diagram

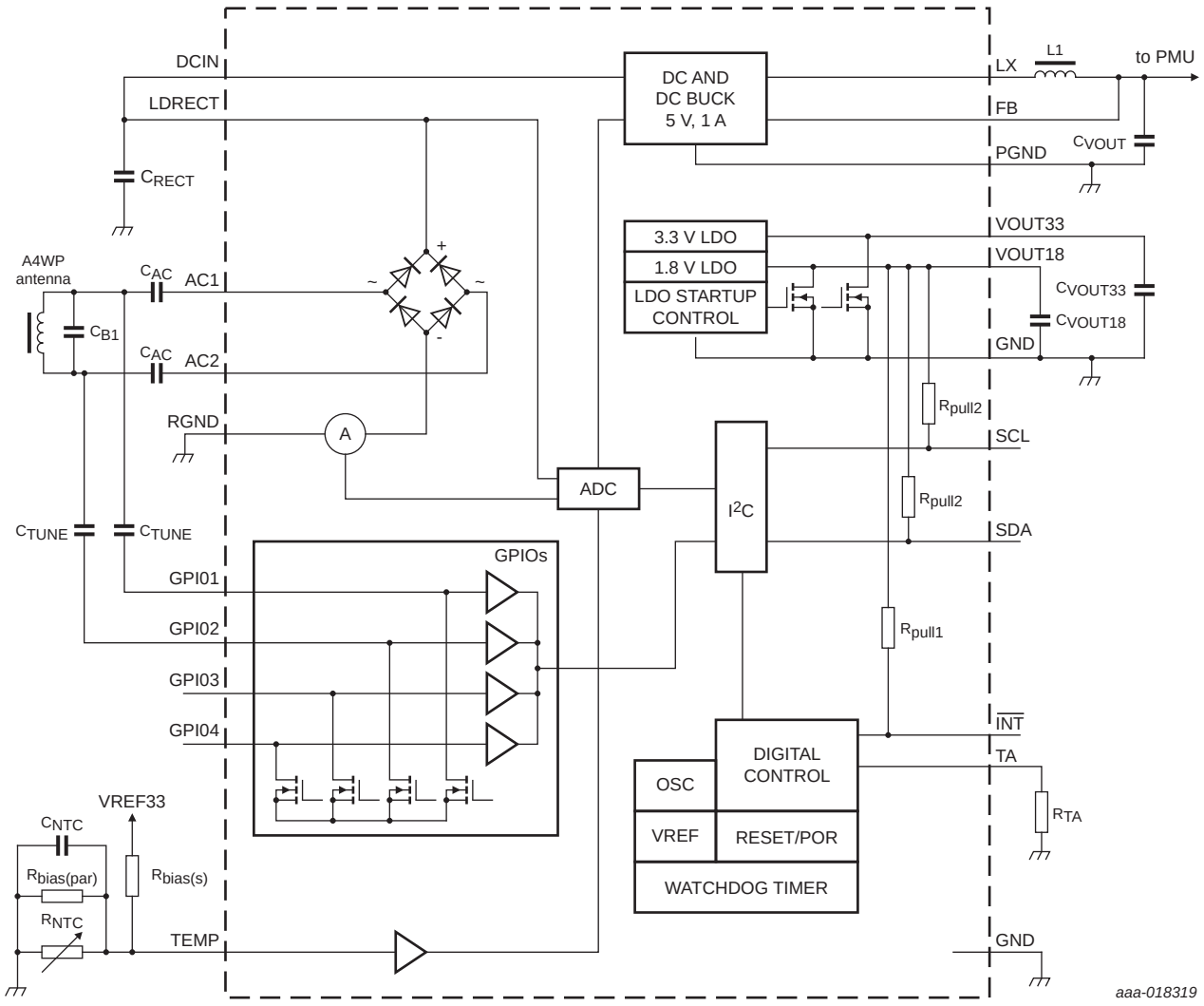


Fig 1. Simplified block diagram

6. Functional diagram

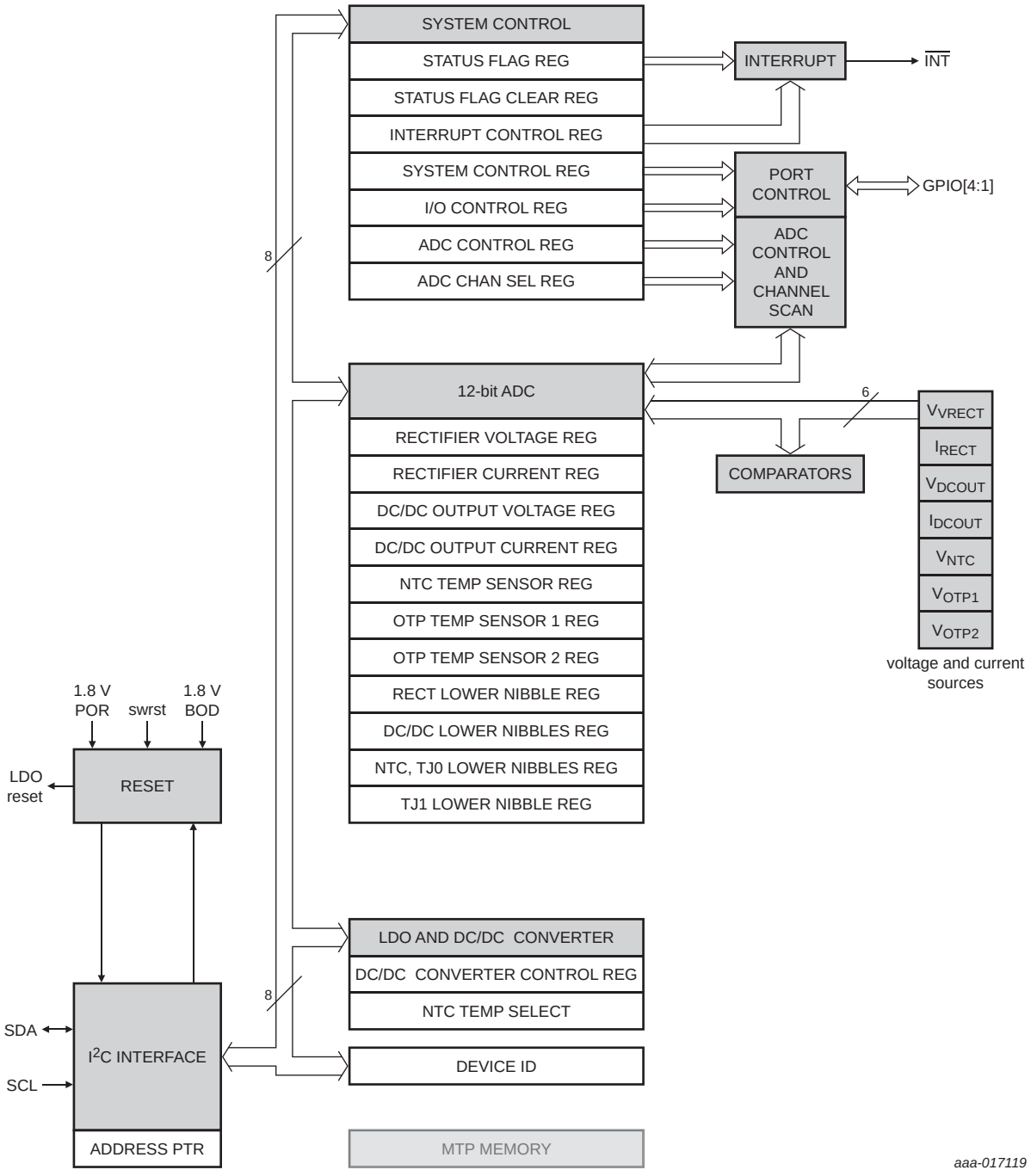
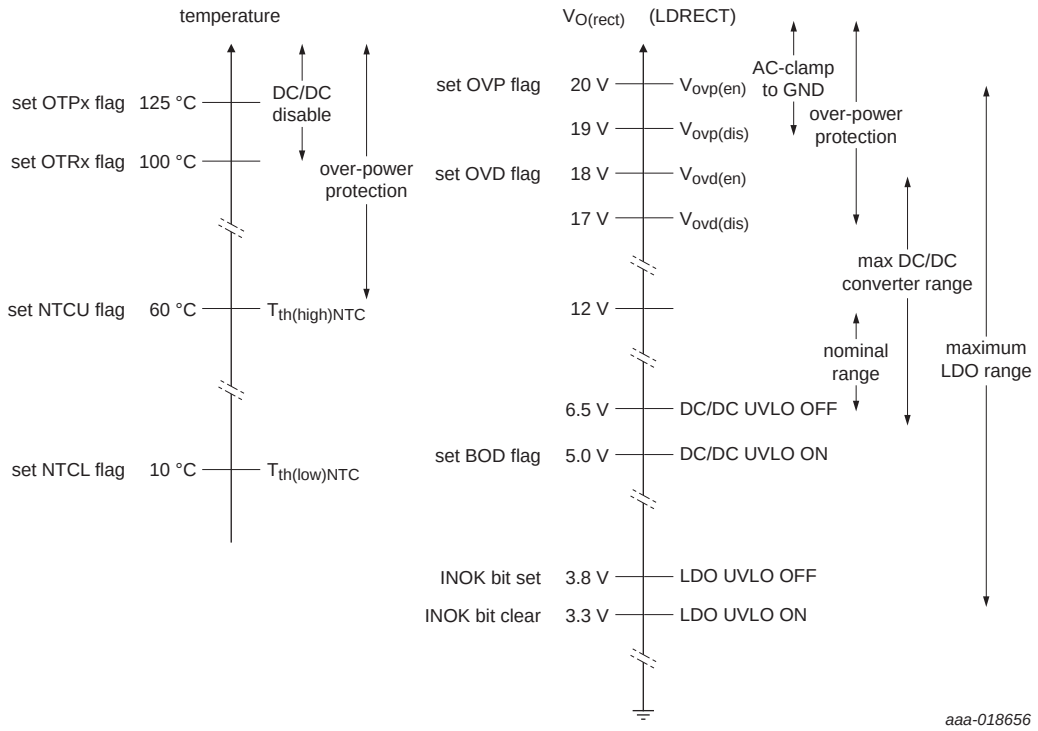


Fig 2. Functional diagram of the digital controller



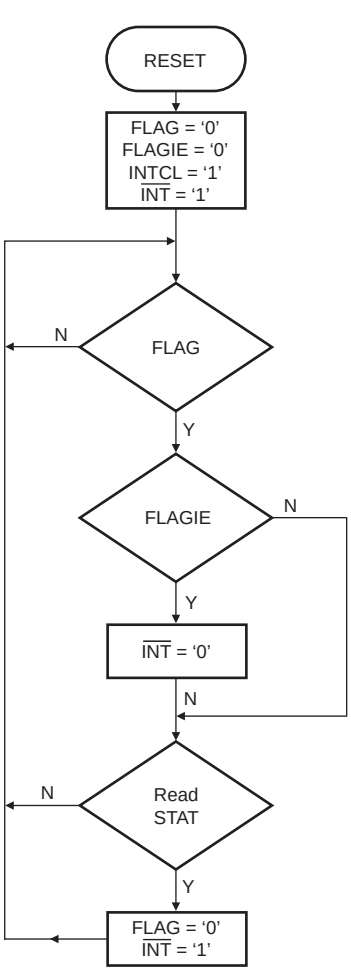
Note: temperature protection is not set by default

Fig 3. Diagram of key voltage and temperature limits

7. Functional description

7.1 Interrupt handling

Figure 4 and Figure 5 provide flow diagrams of the interrupt service request for the host MCU.



FLAG = STATUS FLAG BIT (SET TO '1')
FLAGIE = INTERRUPT ENABLE BIT
INT = INT OPEN-DRAIN PIN
INTCL = INT and Flag automatic clear
STAT = STATUS REGISTERS

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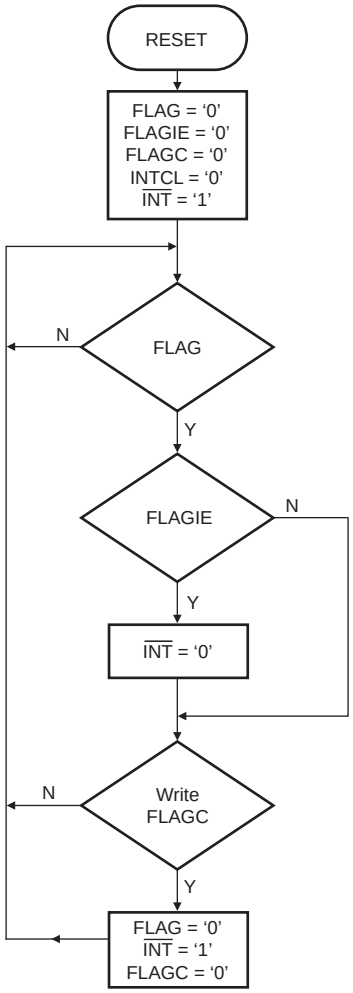
Fig 4. ISR flow diagram using automatic status flag and INT clear (reset) (INTCL = '1')



FLAG = STATUS FLAG BIT (SET TO '1')
FLAGIE = INTERRUPT ENABLE BIT
FLAGC = CLEAR FLAG BIT
INT = INT OPEN-DRAIN PIN
INTCL = INT and Flag automatic clear

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Fig 5. ISR flow diagram using the status flag clear registers (INTCL = '0')

7.1.1 Automatic over-power protection (OVP)

The over-power function automatically enables when the rectifier output voltage ($V_{O(rect)}$) exceeds 18 V. It turns on GPIO1 and GPIO2 in an effort to reduce energy transfer.

The OVD function is permanently enabled. A voltage comparator is used to detect when $V_{O(rect)}$ rises above the upper voltage limit, $V_{ovd(en)}$. The rising edge of the comparator output sets the OVD flag bit to logic 1. The OVD flag is a bit corresponding to the status register STATU. The OVD flag records the occurrence of the event. The GPIO1 and GPIO2 open-drain pins connect the C_{TUNE} capacitors to ground as long as V_{RECT} is above $V_{ovd(dis)}$. Also, if the OVDIE bit is set to logic 1, the open-drain $\overline{INT}$ pin is set to logic 0. It initiates an interrupt service request from the host microcontroller. To clear the interrupt triggered condition, the V_{RECT} voltage must drop below the over-voltage limit ($V_{ovd(dis)}$). The OVD flag bit is cleared by using the automatic clear of status bits (INTCL = logic 1 in the SYSCONL register) and reading the STATU register. Alternatively, it can be cleared by writing a logic 1 to the OVDC bit in the status flag clear register. Resetting the $\overline{INT}$ pin back to logic 1 clears the interrupt request. Once the OVD flag is cleared, it is not set again until the $V_{O(rect)}$ voltage crosses below $V_{ovd(dis)}$ and then exceeds $V_{ovd(en)}$ again. See Figure 4 and Figure 5 for diagrams of interrupt request handling by the host microcontroller and the NX2A4WP device.

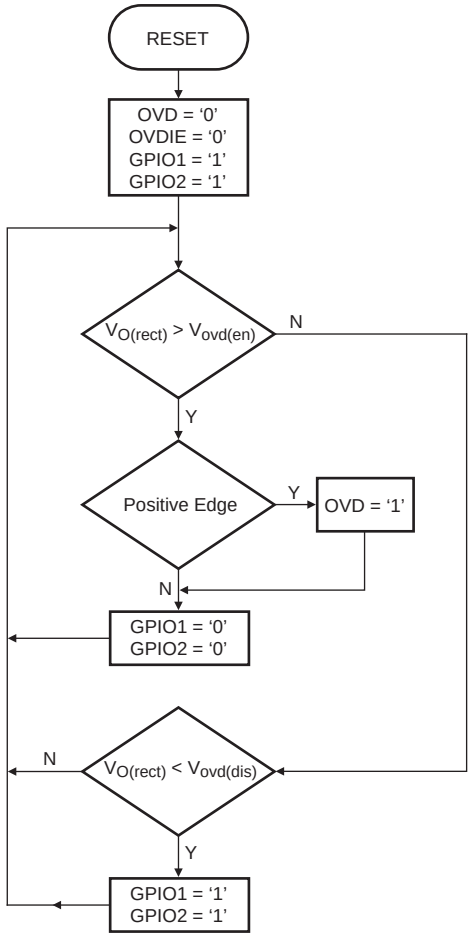


Fig 6. Flow diagram of automatic over-power protection

7.1.2 Automatic over-voltage protection

Sudden jumps in the voltage or energy transmitted to a receiver can occur when other receivers are switched in and out of the common radiation field of a single transmitter. There are two alternative mechanisms available for over-voltage protection of the AC-input pins (AC1 and AC2). The automatic frequency over-power protection method is described above in Section 7.1.1, and the other option, the AC-clamp, is described in this section. For details see Figure 3, Figure 6 and Figure 7.

The automatic over-voltage protection shorts both AC-input pins directly to ground when the rectifier output voltage ($V_{O(rect)}$) exceeds the over-voltage protection limit ($V_{ovp(en)}$). When the over-voltage takes place, the energy stays in the resonator circuit. In this way, the rectifier voltage stops from rising any further. When the rectifier voltage drops below the over-voltage protection limit ($V_{ovp(dis)}$) the shorts are removed and the rectifier returns to normal operation.

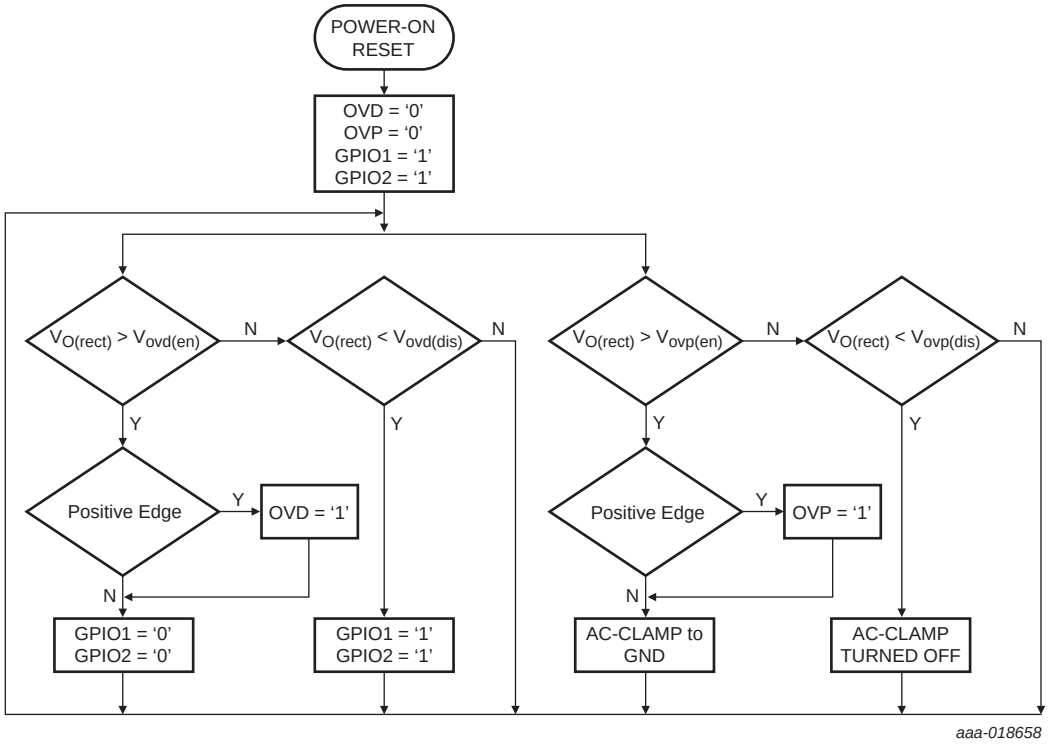
The AC-clamp function is permanently enabled. When $V_{O(rect)}$ is higher than $V_{ovp(en)}$, the OVP flag bit in the status register is set to logic 1. Both AC-input pins are shorted to ground as long as $V_{O(rect)}$ is above $V_{ovp(dis)}$. Also, if the OVPIE bit is set to logic 1, the open-drain INT pin is set to logic 0. It initiates an interrupt service request (ISR) from the host microcontroller. To clear the interrupt condition, the $V_{O(rect)}$ voltage must drop below the over-voltage Protection Off limit ($V_{ovp(dis)}$). The microcontroller clears the OVP status flag by setting the OVPC bit to logic 1 in the status flag clear register. It is also cleared if the INTCL bit in the SYSCONL register is enabled, and the STATU register is read. The INT pin is reset back to logic 1. For details, see Figure 7.

During an over-voltage event, all LDO regulators remain enabled.

In contrast, the response of the DC-to-DC converter to an over-voltage event is software selectable by the host microcontroller. The default setting of the DCOVE bit is logic 0 in the system control register. The DC-to-DC converter is permanently enabled and an OVP event does not control it.

WARNING: When both the DCOVE bit and the OVPIE bit are set to logic 1, the DC-to-DC converter is disabled automatically. It is done by setting the DCEN bit to logic 0 in the system control register when the OVP flag bit is set to logic 1 in the status register. These settings disrupt the power supply in case the DC-to-DC converter output is the only source of energy for the BLE host microcontroller. Once the power is lost, the host microcontroller might be inoperable and cannot re-enable the DC-to-DC converter.

The OVP flag triggers an interrupt request and is cleared by clearing the flag bit.
After the over-voltage event is removed and the rectifier returns to normal operation, the DC-to-DC converter must be re-enabled. It is re-enabled by setting the DCEN bit to logic 1 and clearing the OVP flag using the host microcontroller.



GPIO1 = GPIO1 open-drain pin
GPIO2 = GPIO2 open-drain pin
OVD = over-power protection flag
OVP = over-voltage protection flag
$V_{O(rect)}$ = voltage on pin LDRECT
$V_{ovd(en)}$ = over-power protection enable trip point
$V_{ovd(dis)}$ = over-power protection disable trip point
$V_{ovp(en)}$ = over-voltage protection (AC-clamping) enable trip point
$V_{ovp(dis)}$ = over-voltage protection (AC-clamping) disable trip point

Fig 7. Flow diagram of automatic over-power protection and AC-clamping for over-voltage protection

7.2 ADC

The ADC enables direct measurements of internal voltages, currents, on-chip temperatures, and off-chip temperatures ($V_{O(rect)}$, $I_{O(rect)}$, V_O, I_O, chip temperature and NTC voltage). It is a 12-bit successive approximation (SAR) Analog-to-Digital converter (ADC) with a 7-channel input multiplexer. The host microcontroller configures and controls the ADC. The ADC does a single scan cycle of the selected input channels and stores their code values in corresponding data registers for readout by the microcontroller.

The analog input channels are selected or de-selected by setting the ADx bits to logic 1 or logic 0 in the ADC channel enable register. The ADC controller subsystem sequentially converts the input voltage of each of the selected input channels. It stores the corresponding 12-bit results in the respective data registers in the form of the MSB byte register and the LSB nibble register. After completion of the last selected channel, the ADC is disabled.

The ADC samples the selected input channels before the 400 kHz I^2C bus allows the host MCU to read the first data byte from the first enabled channel. So, the host microcontroller does not require further control of the ADC or completion confirmation.

7.3 On-chip over-temperature protection

On-chip temperature sensors are used to monitor the DC-to-DC converter and the active rectifier for excessive heating. They are intrinsic p-n-junction diode references each connected to a voltage comparator with their own voltage reference. The OTP1 or OTP2 flags in the status register are set to logic 1 whenever the diode voltage transitions above the comparator reference voltage (125 °C, typically). If this condition occurs, the DC-to-DC converter can be disabled. The automatic disable mode is enabled when both the DCTOE bit in the system control register and the corresponding OTPxIE bit in the ICON register are set to logic 1.

WARNING: These settings disrupt the power supply in case the DC-to-DC converter output is the only source of energy for the BLE host microcontroller. Once the power is lost, the host microcontroller might be inoperable and cannot re-enable the DC-to-DC converter.

When the temperature drops below 100 °C (typically), another interrupt is triggered and the OTRx flag is set to logic 1. It indicates that the device has recovered from the over-temperature condition and is ready to operate in a safe range again. The OTPx and/or OTRx flags remain set to logic 1. The microcontroller can clear the flags. Alternatively, the flags can be cleared by using the automatic clear function (INTCL = logic 1) and reading the STATL register via the I^2C bus.

The OTPx or OTRx flags trigger an interrupt service request (ISR) from the microcontroller by setting the $\overline{INT}$ pin to logic 0. The microcontroller can measure the voltages directly with the ADC. It makes the necessary adjustments either by disabling the DC-to-DC converter or reducing the power of the transmitter. It can monitor the temperature until it returns to a lower value before it re-enables the DC-to-DC converter.

7.4 Off-chip NTC over- and under-temperature protection

The NX2A4WP supports one external NTC temperature sensor. A constant and accurate 3.3 V voltage source is supplied from the VREF33 pin. The NTC voltage is input through the TEMP pin and connected to two voltage comparators. The voltage comparators have their voltage references $T_{th(high)NTC}$ typically 60 °C, and $T_{th(low)NTC}$ typically 10 °C. Whenever the temperature is outside this range, either the NTCU flag or the NTCL flag is set to logic 1 in the status register. If the corresponding interrupt enable bits are set to logic 1 in the interrupt control register, the NTCU or NTCL flags trigger an interrupt service request (ISR) from the microcontroller by setting the $\overline{INT}$ pin to logic 0. The microcontroller can trigger an ADC scan cycle and directly measure the output voltage of the NTC temperature sensor. For details refer to Figure 3, Figure 5 and Figure 8. (See also Table 4 and Section 7.10.4). By setting the DCNTE bit in the SYSCONL register to logic 1, the DC-to-DC converter is disabled when the upper NTC temperature limit ($T_{th(high)NTC}$) is exceeded.

WARNING: These settings disrupt the power supply in case the DC-to-DC converter output is the only source of energy for the BLE host microcontroller. Once the power is lost, the host microcontroller might be inoperable and cannot re-enable the DC-to-DC converter.

Refer to Section 7.10.4.4 for further details.

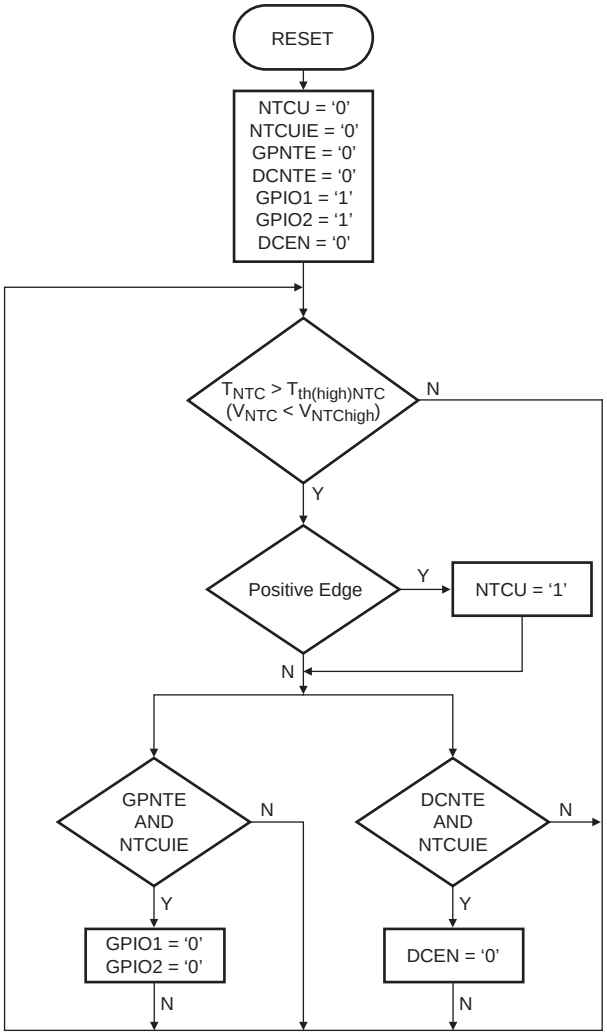


Fig 8. Flow diagram of the off-chip NTC over-temperature protection

7.5 DCIN and LDRECT inputs

To minimize supply voltage noise and ripple, bypass capacitor of value between 35 μF to 100 μF is connected between these pins and ground.

7.6 LDODCPL

The pin LDODCPL allows for noise filtering of the internal LDO18 and LDO33 supply rail. It reduces supply noise and allows the switching of the LDO supply input between $V_{O(rect)}$ and the DC-to-DC converter output voltage in order to optimize efficiency. As soon as the DC-to-DC converter output voltage is sufficiently high, the LDO supply input is switched from the LDRECT pin to the LDDC pin. The LDDC pin is connected to the output of the DC-to-DC converter. A decoupling capacitor of 10 μF is connected between this node and ground.

7.7 LDO start-up control

The LDO start-up control monitors the DC input voltage. Once this voltage exceeds V_{UVLO} the two LDOs are enabled simultaneously after a delay of ~1.5 ms.
The LDOs are disabled in case their DC supply voltage drops below $V_{BODtrip}$ ($V_{UVLO(LDO)} = V_{BOD(LDO)} + V_{BODhys}$), see Figure 9.

If there is a shutdown, the LDOs contain discharge paths to ramp down the supply voltage.

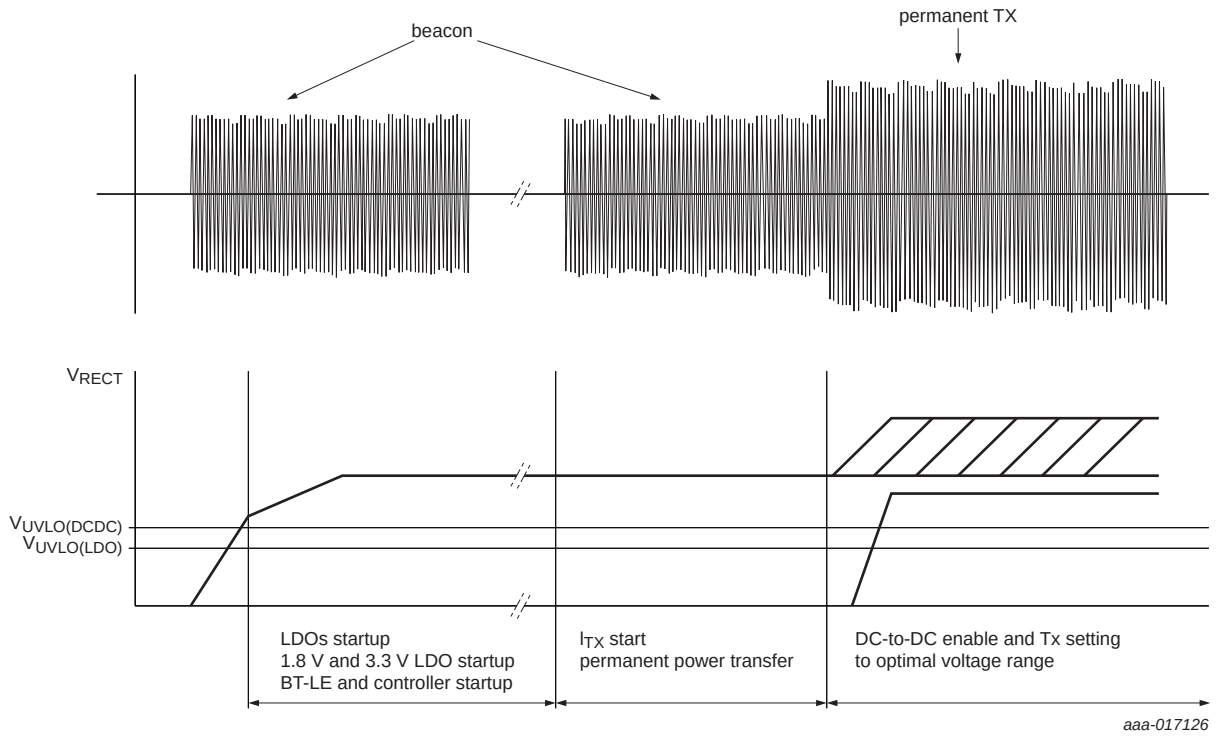


Fig 9. NX2A4WP start-up sequence

7.8 General Purpose digital Input Output ports (GPIOs)

The GPIOs can be used for control and communication applications. They are software configured and controlled through the I^2C and can be configured as digital inputs and/or open-drain outputs.

Each GPIO's operation mode can be controlled individually using the GPIEx bits in the IOCONL register. When configured as inputs, the logic level of each GPIO pin can be read through the associated GPI bit in the IOCONU register. If a GPIO is used as an open-drain output, the open-drain pull-down transistor is enabled. The pin is pulled low by writing a logic 0 to the related GPO bit in the IOCONL register. Otherwise, the pin is tri-stated (high impedance). When the pin is not pulled to a logic level, the input buffer should be disabled to prevent feed-through currents in the buffer.

7.9 External supply detect pin (TA)

The TA pin can be used to sense an external supply connection or state change. If the logic value changes from high to low or low to high for more than 11 ms, the interrupt pin is asserted. The pin cannot be disabled through I^2C, and it should not be left floating. When the TA pin is not used, it is recommended to pull it down to ground through resistor R_{TA} (see Table 4).

7.10 Software interface[1]

7.10.1 I²C device address

The slave address of the NX2A4WP is shown in Figure 10.

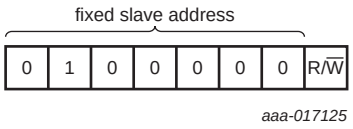


Fig 10. NX2A4WP address

The LSB of the slave address defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

7.10.2 I²C-bus interface definition

Table 3. Interface definition

Byte	Bit							
	7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
I²C-bus slave address	0	1	0	0	0	0	0	R/$\overline{W}$
I/O data bus	B7	B6	B5	B4	B3	B2	B1	B0

7.10.3 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a register address byte, which is stored in the Pointer register of the NX2A4WP. This register is write only.

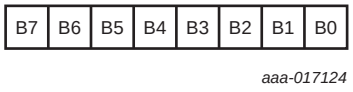


Fig 11. Pointer register bits

If auto increment is enabled (default: the AUTO bit in the SYSCONU register set to logic 1), the register address will be incremented after every data read or data write transaction.
As an example, the communication flow to read the ADC channels from the ADC0DU to the ADC6DL register is shown here:

1. AUTO in SYSCONU = logic 1
2. MCU writes FDh to register address ADCEL to trigger ADC conversions on 6 of the 7 ADC input channels:
   - send slave/device address 0100 0000 (with LSB = logic 0 for write operation)
   - send ADCEL address 0000 1001 (09h) to the pointer register
   - send data 1111 1101 to ADCEL so that the 6 ADC channels are selected and the conversions are started

1. Reference: 'I²C-bus specification and user manual', UM10204, Rev. 06, 4 April 2014

3. MCU reads channels ADC0DU to ADC6DL:
   - send the slave/device address 0100 0000 (with LSB = logic 0 for write operation)
   - send the ADC0DU address 0000 1011 (0Bh) to the pointer register
   - send the slave/device address 0100 0001 (with LSB = logic 1 for READ operation)
   - read the register address 0Bh; the pointer register is incremented after it is read automatically from ADC0DU (0Bh) 0000 1011 to ADC1DU (0Ch) 00001100
   - read the register address 0Ch; the pointer register is incremented after it is read automatically from ADC1DU (0Ch) 0000 1100 to ADC2DU (0Dh) 00001101;
   - continue until e.g. ADC6DL is read and MCU terminates read sequence by not acknowledging and sending a stop condition

Table 4. NX2A4WP Register address map and bit definitions

				Address / data content [1][2]								
Hexadecimal Address	**Name**	**Description**	**Access**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**Reset value**
System Control and Status Registers												
00	STATL	Status Register Lower Byte	RO	IDC	NTCL	NTCU	OTR2	OTR1	OTP2	OTP1	INOK	xxxx xxxx
01	STATU	Status Register Upper Byte	RO	–	–	–	OVP	OVD	–	BOD	TAH	0000 0000
02	SFCLRL	Status Flag Clear Register Lower Byte	WO	IDCC	NTCLC	NTCUC	OTR2C	OTR1C	OTP2C	OTP1C	–	0000 0000
03	SFCLRU	Status Flag Clear Register Upper Byte	WO	–	–	–	OVPC	OVDC	–	BODC	TAHC	0000 0000
04	ICON	Interrupt Control Register	R/W	TAIE	OVPIE	OVDIE	IDCIE	NTCLIE	NTCUIE	OTP2IE	OTP1IE	0000 0000
05	SYSCONL	System Control Register Lower Byte	R/W	INTCL	DCOVE	HRECT	PRECT	DCNTE	GPNTE	–	DCTOE	1000 0010
06	SYSCONU	System Control Register Upper Byte	R/W	–	–	–	–	–	AUTO	SWRT	DCEN	1111 0101
07	IOCONL	I/O Control Register Lower Byte	R/W	GPIE4	GPIE3	GPIE2	GPIE1	GPO4	GPO3	GPO2	GPO1	0000 1111
08	IOCONU	I/O Control Register Upper Byte	RO	–	–	–	–	GPI4	GPI3	GPI2	GPI1	0000 0000
ADC Registers												
09	ADCEL	ADC Channel Enable Register Lower Byte	R/W	ADEN	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0111 1111
0A	ADCEU	ADC Channel Enable Register Upper Byte	R/W	–	–	–	–	–	–	–	–	0000 0000
0B	ADC0DU	ADC Channel 0 V_{RECT} Data Reg. Upper Byte	RO	ADC0DU								[2]
0C	ADC1DU	ADC Channel 1 I_{RECT} Data Reg. Upper Byte	RO	ADC1DU								[2]
0D	ADC2DU	ADC Channel 2 V_{DCOUT} Data Reg. Upper Byte	RO	ADC2DU								[2]
0E	ADC3DU	ADC Channel 3 I_{DCOUT} Data Reg. Upper Byte	RO	ADC3DU								[2]
0F	ADC4DU	ADC Channel 4 V_{NTC} Data Register Upper Byte	RO	ADC4DU								[2]
10	ADC5DU	ADC Channel 5 V_{OTP1} Data Reg. Upper Byte	RO	ADC5DU								[2]

Table 4. NX2A4WP Register address map and bit definitions

				Address / data content [1][2]								
Hexadecimal Address	**Name**	**Description**	**Access**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**Reset value**
11	ADC6DU	ADC Channel 6 V_{OTP2} Data Reg. Upper Byte	RO	ADC6DU								[2]
12	ADC10DL	ADC Channel 1 and 0 Data Register Lower Nibble	RO	ADC10DL								[2]
13	ADC32DL	ADC Channel 3 and 2 Data Register Lower Nibble	RO	ADC32DL								[2]
14	ADC54DL	ADC Channel 5 and 4 Data Register Lower Nibble	RO	ADC54DL								[2]
15	ADC6DL	ADC Channel 6 Data Register Lower Nibble	RO	ADC6DL								[2]
DC-to-DC Control Registers												
19	DCSEL	DC-to-DC V_{OUT} and I_{OUT} Level Select	R/W	V3	V2	V1	V0	C3	C2	C1	C0	0100 1011
NTC interrupt temperature limit control register												
1A	NTCSEL	NTC High and Low $\overline{INT}$ Level Select	R/W	–	–	NTCUL 1	NTCUL 0	–	–	NTCLL1	NTCLL0	0001 0001
Device Identification code												
1F	DEVID	Device Identification Code Register	RO	DEVID7	DEVID6	DEVID5	DEVID4	DEVID3	DEVID2	DEVID1	DEVID0	0100 0000

[1] Bits described with '-' in this table are reserved for future use.
Always write logic 0 to undefined bits.

[2] Bits with no value given have no default (e.g. the ADC data bits). Generation of valid content for those bits has to be triggered by conducting an ADC conversion cycle.

7.10.4 Register descriptions

7.10.4.1 Status registers (STATL, address 00h; STATU, address 01h)

The status register contains basic device status flags. It contains temperature limit status, over-current, over-voltage, recorded reset events (BOD), and detection of the presence of a USB power supply. The status registers are read-only and writes to these registers have no effect. With autoincrement and autoclear active (AUTO = logic 1 and INTCL = logic 1), both registers must be read simultaneously in one I^2C read segment. It is to prevent the STATU register being cleared with the next ACK, due to data caching in this mode and information might get lost. These registers should be read after power-up of the controller to clear them initially as it is not done by the POR. A read operation is performed as described in Section 7.10.5.2.

Table 5. Status register lower byte (STATL, address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	IDC	NTCL	NTCU	OTR2	OTR1	OTP2 [3]	OTP1 [3]	INOK
Default	X	X	X	X	X	X	X	X

Table 6. Status register lower byte bit mapping (STATL, address 00h)

Bit	Symbol	Function [1][2]
0	INOK [2]	INOK reflects the current voltage level of the power supply for the LDO regulators (LDODCPL pin) INOK = logic 0; $V_{LDODCPL}$ < 3.3 V INOK = logic 1; $V_{LDODCPL}$ > 3.8 V
1	OTP1 [3]	If the OTP1 (rectifier) temperature sensor rises above the T_j = 125 °C limit, OTP1 toggles from logic 0 to logic 1 OTP1 = logic 0 if $T_{j(OTP1)}$ < 125 °C or after resetting OTP1
2	OTP2 [3]	If the OTP2 (DC-to-DC) temperature sensor rises above the T_j = 125 °C limit, OTP2 toggles from logic 0 to logic 1 OTP2 = logic 0 if $T_{j(OTP2)}$ < 125 °C or after resetting OPT2
3	OTR1	If the OTP1 (rectifier) temperature sensor falls below the T_j = 100 °C limit, OTR1 toggles from logic 0 to logic 1 OTR1 = logic 0 at any other temperature and after resetting OTR1
4	OTR2	If the OTP2 (DC-to-DC) temperature sensor falls below the T_j = 100 °C limit, OTR2 toggles logic 0 to logic 1 OTR2 = logic 0 at any other temperature and after resetting OTR2
5	NTCU[4]	If the NTC sensor temperature rises above the $T_{th(high)NTC}$ limit, NTCU toggles from logic 0 to logic 1 NTCU = logic 0 if NTC < $T_{th(high)NTC}$ or after resetting NTCU
6	NTCL[4]	If the NTC sensor temperature falls below the $T_{th(low)NTC}$ limit, NTCL toggles from logic 0 to logic 1 NTCL = logic 0 if NTC > $T_{th(low)NTC}$ or after resetting NTCL
7	IDC	IDC = logic 1; DC-to-DC converter output current rises above the current limit (DCSEL, bits C3-C0) IDC = logic 0; DC-to-DC converter output current is below limit (DCSEL, bits C3-C0)

[1] The status bits, except INOK, are edge triggered on the related event occurring (edge triggered: flag stores an event at its beginning with no relation to the duration or its end. For example, the event can be a rising or a falling edge of a signal). The bits are not automatically reset once triggered. They store the event related to their function until cleared via the respective status flag clear bit or by reading the STATL register while INTCL is logic 1.

[2] INOK is a non-latched bit representing the level of the LDO supply voltage $V_{LDODCPL}$ sensed by a BOD circuit.

[3] The OTP1 sensor is located near the rectifier area while the OPT2 sensor is near the DC-to-DC converter.

[4] The NTC comparator has hysteresis of 10 °C.

Table 7. Status register upper byte (STATU, address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	–	–	–	OVP	OVD	–	BOD	TAH
Default	0	0	0	0	0	0	0	0

Table 8. Status register upper byte bit mapping (STATU, address 01h)

Bit	Symbol	Function [1] [2]
0	TAH[2]	TAH is a non-latched bit always reflecting the TA input pin voltage level. It cannot be cleared via TAHC. TAH = logic 1; a high voltage is detected on the TA pin TAH = logic 0; a low voltage is detected on the TA pin
1	BOD	BOD = logic 1; DCIN ($V_{O(rect)}$) voltage falls below $V_{BOD(DCDC)}$, brownout detector monitoring the voltage on the DCIN pin was triggered BOD = logic 0; DCIN voltage did not experience a brownout event The BOD flag is cleared on the initial power-up.
2	–	Reserved
3	OVD	OVD = logic 0; $V_{O(rect)} < V_{ovd(en)}$ OVD = logic 1; over-voltage protection limit reached (DCIN voltage > $V_{ovd(en)}$)
4	OVP	OVP = logic 0; $V_{O(rect)} < V_{ovd(en)}$ OVP = logic 1; AC-clamping over-voltage protection limit reached (DCIN voltage > $V_{ovd(en)}$)
5	–	Reserved
6	–	Reserved
7	–	Reserved

[1] The status bits, except TAH, are edge triggered on the related event occurring (edge triggered: flag bit stores an event at its beginning with no relation to the duration or its end. For example, an event can be a rising and/or a falling edge of a signal). The bits are not automatically reset once triggered and only store the event related to their function until cleared via the respective status flag clear bit or by reading the STATU register while INTCL is logic 1.

[2] TAH is a non-latched bit representing the voltage level of the TA input pin. The $\overline{INT}$ signal records the event in a hidden register and is edge triggered on both edges of TAH. ($\overline{INT}$ is triggered in case TAH toggles from logic 0 to logic 1 or reverse). The $\overline{INT}$ hidden register is cleared by writing a logic 1 to the TAHC bit in the SFCLRU register or by reading the STATU register with the INTCL bit set to logic 1 in the SYSCONL register.

The basic behavior of TAH in combination with $\overline{INT}$ while reading the status registers (INTCL = logic 1) is depicted in Figure 12 below. The TA input pin filters out glitches less than 11 ms wide using a digital debounce circuit.

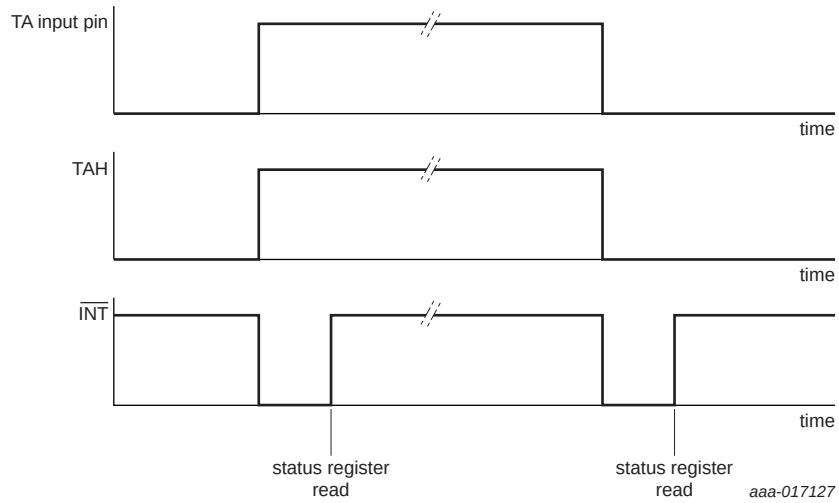


Fig 12. TA, TAH and $\overline{INT}$ behavior during a TA interrupt trigger and read cycle

7.10.4.2 Status flag clear registers (SFCLRL, address 02h; SFCLRU, address 03h)

Status flag bits record certain events and reside in the status registers, STATL or STATU. They can be cleared individually by writing a logic 1 to the matching bit in the status flag clear registers. The bit positions in SFCLRL matching positions in STATL are cleared by writing a logic 1. Similarly, the bit positions in SFCLRU matching those positions in STATU, are cleared by writing a logic 1. Refer to Table 5 and Table 7 for details.
For TAH, the corresponding status flag clear bit TAHC is to reset the hidden $\overline{INT}$ pin control latch. However, it does not clear the non-latched TAH flag bit to logic 0. The INOK bit is a non-latched bit and does not trigger an interrupt. Therefore, there is no corresponding clear bit. These 2 bits represent true logic level of the related signals and do not record events. Alternatively, all the status flags can be cleared automatically by reading each status register when the INTCL bit in the SYSCONL register is set to logic 1 (reset default value).

Table 9. Status flag clear register lower byte (SFCLRL, address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	IDCC	NTCLC	NTCUC	OTR2C	OTR1C	OTP2C	OTP1C	[1]
Default	0	0	0	0	0	0	0	0

Table 10. Status flag clear register upper byte (SFCLRU, address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	[1]	[1]	[1]	OVPC	OVDC	[1]	BODC	TAHC [2]
Default	0	0	0	0	0	0	0	0

[1] Reserved, always write logic 0 to undefined bits.

[2] INOK and TAH cannot be reset. By writing a logic 1 to the TAHC bit, only the $\overline{INT}$ pin control latch for the TAH bit is cleared.

7.10.4.3 Interrupt control register (ICON, address 04h)

The interrupt control register enables the masking of the different available interrupt signals. When enabled, interrupt events trigger the $\overline{INT}$ pin to be pulled low when the matching flag bit in the status registers (STATL and STATU) is set. The status registers are cleared by reading the register with INTCL = logic 1 (automatic clear) or via the status flag clear register. The status bits in each status register remain set until cleared. The $\overline{INT}$ pin is connected to the VOUT18 supply via an integrated 20 kΩ resistor.

Table 11. Interrupt control register (ICON, address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	TAIE	OVPIE	OVDIE	IDCIE	NTCLIE	NTCUIE	OTP2IE	OTP1IE
Default	0	0	0	0	0	0	0	0

Table 12. Interrupt control register bit mapping (ICON, address 04h)

Bit	Symbol	Function
0	OTP1IE	Over-temperature protection 1 interrupt enable OTP1IE = logic 1; OTP1 or OTR1 can trigger $\overline{INT}$ OTP1IE = logic 0;OTP1 or OTR1 trigger of $\overline{INT}$ disabled
1	OTP2IE	Over-temperature protection 2 interrupt enable OTP2IE = logic 1; OTP2 or OTR2 can trigger $\overline{INT}$ OTP2IE = logic 0; OTP2 or OTR2 trigger of $\overline{INT}$ disabled
2	NTCUIE	NTC high temperature limit exceeded ($T_{th(high)NTC}$) $\overline{INT}$ enable NTCUIE = logic 1; NTCU can trigger $\overline{INT}$ NTCUIE = logic 0; NTCU trigger of $\overline{INT}$ disabled
3	NTCLIE	NTC lower temperature limit exceeded ($T_{th(low)NTC}$) $\overline{INT}$ enable NTCLIE = logic 1; NTCL can trigger $\overline{INT}$ NTCLIE = logic 0; NTCL trigger of $\overline{INT}$ disabled
4	IDCIE	DC-to-DC converter output current limit exceeded $\overline{INT}$ enable IDCIE = logic 1; IDC can trigger $\overline{INT}$ IDCIE = logic 0; IDC trigger of $\overline{INT}$ disabled
5	OVDIE	over-power protection reached $\overline{INT}$ enable OVDIE = logic 1; OVD can trigger $\overline{INT}$ OVDIE = logic 0; OVD trigger of $\overline{INT}$ disabled
6	OVPIE	V_{OVPon} over-voltage protection limit reached $\overline{INT}$ enable OVPIE = logic 1; OVP can trigger $\overline{INT}$ OVPIE = logic 0; OVP trigger of $\overline{INT}$ disabled
7	TAIE	TA input interrupt trigger $\overline{INT}$ enable TAIE = logic 1; TA rising or falling input change can trigger $\overline{INT}$ TAIE = logic 0; TA input trigger of $\overline{INT}$ disabled

7.10.4.4 System control registers (SYSCONL, address 05h; SYSCONU, address 06h)

The lower byte of the system control register enables or disables possible automatic actions triggered by the status flags. Enabled interrupts trigger the $\overline{INT}$ pin LOW. If the INTCL bit is set, the set status bits in a status register are cleared after the register is read, except for the INOK and the TAH flags. The INOK and TAH flags cannot be cleared as they are level triggered. If the INTCL bit is logic 0, the set status bits in the status registers remain set until cleared via the status flag clear register.

Table 13. System control register lower byte (SYSCONL, address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	INTCL	DCOVE	HRECT	PRECT	DCNTE	GPNTE	[1]	DCTOE
Default	1	0	0	0	0	0	0	0

[1] Reserved, always write logic 0 to undefined bits

Table 14. System control register lower byte bit mapping (SYSCONL, address 05h)

Bit	Symbol	Function
0	DCTOE	Enable OTP1 or OTP2 control of DC-to-DC converter DCTOE = logic 1; if (OTP1 and OTP1IE) are set to logic 1 or (OTP2 and OTP2IE) are set to logic 1, DCEN is reset to logic 0 (junction over-temperature trip point reached, DC-to-DC turned off) DCTOE = logic 0; no automatic DC-to-DC disable at over-temperature trip point
1	–	Reserved
2	GPNTE	Enable NTCU control of GPO1 and GPO2 for over-power protection GPNTE = logic 1; over-power protection enabled (GPO1, GPO2 low ohmic) as long as $T_{th(high)NTC}$ limit is exceeded GPNTE = logic 0: automatic over-power protection disabled
3	DCNTE	Enable NTCU control of DC-to-DC converter DCNTE = logic 1; if NTCU and NTCUIE are set to logic 1, and the NTC over-voltage limit is reached, DCEN is reset to logic 0; no automatic DC-to-DC disable when the NTC upper temperature limit is reached
4	PRECT	PRECT = logic 1 and HRECT logic 0; enable passive rectification mode PRECT = logic 0 and HRECT = logic 0; active rectification mode enabled Bits PRECT and HRECT are mutually exclusive. If both bits are set at once, then they both default to 00b (active rectification mode)
5	HRECT	HRECT = logic 1 and PRECT = logic 0: enable half-active rectification mode HRECT = logic 0 and PRECT = logic 0: active rectification mode enabled Bits PRECT and HRECT are mutually exclusive. If both bits are set at once, then they both default to 00b (active rectification mode)
6	DCOVE	Enable OVP control of DC-to-DC DCOVE = logic 1 If OVP and OVPIE are set to logic 1 and the AC-clamp enable trip point is reached, DCEN is reset to logic 0 DCOVE = logic 0; no automatic DC-to-DC disable at AC-clamp trip point
7	INTCL[1]	Enable automatic clear (reset) of set status bits in the status registers and $\overline{INT}$ pin after a register read INTCL = logic 1; automatic clear of flag bits after read enabled INTCL = logic 0; no automatic clear. Status flags are cleared by writing a logic 1 to the related status flag clear register bits

[1] When enabled, both status registers (STATL, STATU) must be read in a single I^2C transaction sequence to avoid losing information.

The upper byte of the system control register controls the DC-to-DC controller. It allows for the software reset of the on-chip digital control logic back to its initialized logic state.

Table 15. System control register upper byte (SYSCONU, address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	[1]	[1]	[1]	[1]	[1]	AUTO	SWRT	DCEN
Default	1	1	1	1	0	1	0	1

[1] Though the four MSBs [7:4] are set to logic 1 after reset and bit 3 is set to logic 0, always write logic 0 to these 5 bits.

Table 16. System control register upper byte bit mapping (SYSCONU, address 06h)

Bit	Symbol	Function
0	DCEN	Enable DC-to-DC converter DCEN = logic 1; DC-to-DC converter enabled DCEN = logic 0; DC-to-DC converter disabled
1	SWRT	Software reset resets all registers to their power-up default values only after the I^2C-bus stop condition is detected SWRT = logic 1 reset all registers; bit SWRT is reset to logic 0
2	AUTO	Enable pointer register auto increment. Pointer register address is incremented after every data byte transfer (read or write) AUTO = logic 1; pointer register auto increment enabled (default) AUTO = logic 0; pointer register auto increment disabled
3	-	Reserved
4	-	Reserved
5	-	Reserved
6	-	Reserved
7	-	Reserved

7.10.4.5 I/O control register (IOCONL, address 07h; IOCONH, address 08h)

The I/O control register controls the General Purpose Input Output (GPIO) pins. The over-power protection circuit also controls the 60 V tolerant GPIO1 and GPIO2 pins. The GPIO3 and GPIO4 pins are 25 V tolerant and can be used for control and communication applications. A logic 1 written to the GPOx bits, tri-states the open-drain output. A logic 0 enables the open-drain output and the pin is shorted to ground. The logic level of GPIO pins is read by enabling the read buffers. The read buffers are enabled by writing a logic 1 to the corresponding GPIEx bit. The logic level of the GPIO pin is found in the matching GPIx bit.

Table 17. I/O control register byte (IOCONL, address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	GPIE4	GPIE3	GPIE2	GPIE1	GPO4	GPO3	GPO2	GPO1
Default	0	0	0	0	1	1	1	1

Table 18. I/O control register byte bit mapping (IOCONL, address 07h)

Bit	Symbol	Function
0	GPO1	GPIO1 control, logic 1 = Z; logic 0 = low ohmic; OR linked to over-power protection
1	GPO2	GPIO2 control, logic 1 = Z; logic 0 = low ohmic; OR linked to over-power protection
2	GPO3	GPIO3 control, logic 1 = Z; logic 0 = low ohmic
3	GPO4	GPIO4 control, logic 1 = Z; logic 0 = low ohmic

Table 18. I/O control register byte bit mapping (IOCONL, address 07h) *…continued*

Bit	Symbol	Function
4	GPIE1	GPIO1 input buffer control, logic 0 = off; logic 1 = on
5	GPIE2	GPIO2 input buffer control, logic 0 = off; logic 1 = on
6	GPIE3	GPIO1 input buffer control, logic 0 = off; logic 1 = on
7	GPIE4	GPIO2 input buffer control, logic 0 = off; logic 1 = on

Table 19. I/O control register byte (IOCONU, address 08h)

Bit	7	6	5	4	3	2	1	0
Symbol	[1]	[1]	[1]	[1]	GPI4	GPI3	GPI2	GPI1
Default	0	0	0	0	0	0	0	0

[1] Always write logic 0 to undefined bits

Table 20. I/O control register byte bit mapping (IOCONU, address 08h)

Bit	Symbol	Function
0	GPI1	Input data latch for GPIO1. The input buffer must be enabled by setting the GPIE1 bit to logic 1
1	GPI2	Input data latch for GPIO2. The input buffer must be enabled by setting the GPIE2 bit to logic 1
2	GPI3	Input data latch for GPIO3. The input buffer must be enabled by setting the GPIE3 bit to logic 1
3	GPI4	Input data latch for GPIO4. The input buffer must be enabled by setting the GPIE4 bit to logic 1
4	–	Reserved [1]
5	–	Reserved [1]
6	–	Reserved [1]
7	–	Reserved [1]

[1] Always write logic 0 to undefined bits

7.10.4.6 ADC controller subsystem channel enable registers (ADCEL, address 09h; ADCEU, address 0Ah)

The ADC channel enable registers control the individual channels to be converted during a one-time scan cycle. Channels 0 to 6 can be individually selected. The conversion cycle is triggered by writing a logic 1 to the ADEN bit in the ADCEL register. The ADC controller subsystem samples and converts all selected channels in one sweep starting at the lowest selected number and stores the results. The data is transferred to the host controller via I^2C reads. After the ADC cycle is triggered, the host microcontroller can start immediately to read the conversion results.

Table 21. ADC enable register lower byte (ADCEL, address 09h)

Bit	7	6	5	4	3	2	1	0
Symbol	ADEN [1]	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default	0	1	1	1	1	1	1	1

Table 22. ADC enable register lower byte bit mapping (ADCEL, address 09h)

Bit	Symbol	Function
0	AD0	V_{RECT} measurements
1	AD1	I_{RECT} measurements
2	AD2	V_{DCOUT} measurements
3	AD3	I_{DCOUT} measurements
4	AD4	V_{NTC} measurements
5	AD5	V_{OTP1} measurements
6	AD6	V_{OTP2} measurements
7	ADEN [1]	ADC sweep enable for channels 0 to 6 (reset after channels are read)

[1] Writing to the ADEN bit triggers the ADC controller subsystem to convert all the selected channels in one conversion cycle. The ADC controller is fast enough so that the first data can be read immediately through the 400 kHz I^2C bus. Although not recommended for actual implementation, the following is just for completeness of information.
The ADEN bit in the ADCEL register serves 2 purposes. It initiates ADC conversion of the selected channels and acts as a conversion busy flag. It remains logic 1 until the ADC conversion of the last selected channel is completed, and then, it is cleared. The ADEN bit cannot be written to until it is cleared to logic 0 by the ADC controller. There is no interrupt associated with the ADC.

Table 23. ADC enable register upper byte (ADCEU, address 0Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Default	0	0	0	0	0	0	0	0

[1] Reserved, always write logic 0 to undefined bits.

7.10.4.7 ADC channel data registers (ADCxDU, ADCxDL, addresses 0Bh - 14h)

The ADC data registers are separated into upper byte and lower nibble of the respective 12-bit data word generated by the ADC for each channel conversion. In cases where an 8-bit value is sufficient, only the upper byte of each value can be read to reduce the read cycle time. Each 12-bit data word consists of ADCxDU(8 MSBs) and ADCxDL(4 LSBs).

Table 24. ADC channels, range and nominal resolution (ADCxDU, ADCxDL, addresses 0Ah - 17h)

ADC address	Data								ADC channel
	B7	B6	B5	B4	B3	B2	B1	B0	
0Bh	ADC0DU								V_{RECT} upper byte
0Ch	ADC1DU								I_{RECT} upper byte
0Dh	ADC2DU								V_{DCOUT} upper byte
0Eh	ADC3DU								I_{DCOUT} upper byte
0Fh	ADC4DU								V_{NTC} upper byte
10h	ADC5DU								V_{OTP1} upper byte
11h	ADC6DU								V_{OTP2} upper byte
12h	ADC1DL				ADC0DL				I_{RECT} lower nibble, V_{RECT} lower nibble
13h	ADC3DL				ADC2DL				Reserved nibble, V_{DCOUT} lower nibble
14h	ADC5DL				ADC4DL				V_{OTP1} lower nibble, V_{NTC} lower nibble
15h					ADC6DL				V_{OTP2} lower nibble

The ADC channel binary codes related to electrical signals are listed in Table 26 to Table 27. The individual scaling per channel may differ, as the channels are scaled to the respective range.

Table 25. Rectifier output voltage coding, channel ADC0Dx, V_{RECT}

Channel electrical value	ADC readout,	ADC0DU 0Bh[7:0]b	ADC0DL 12h[3:0]b
V_{RECT} [V]	decimal code	upper byte, binary code	lower nibble, binary code
4	500	00011111	0100
5	624	00100111	0000
6	750	00101110	1110
7	875	00110110	1011
8	999	00111110	0111
9	1124	01000110	0100
10	1249	01001110	0001
11	1374	01010101	1110
12	1499	01011101	1011
13	1624	01100101	1000
14	1749	01101101	0101
15	1875	01110101	0011
16	1999	01111100	1111
17	2125	10000100	1101
18	2250	10001100	1010
19	2374	10010100	0110
20	2498	10011100	0010

Table 26. Rectifier output current coding, channel ADC1Dx,

Channel electrical value	ADC readout,	ADC1DU 0Ch[7:0]b	ADC1DL 12h[7:4]b
I_{RECT}[1] [A]	decimal code	upper byte, binary code	lower nibble, binary code
0.1	160	00001010	0000
0.2	336	00010101	0000
0.3	504	00011111	1000
0.4	688	00101011	0000
0.5	856	00110101	1000
0.6	1024	01000000	0000
0.7	1199	01001010	1111
0.8	1370	01010101	1010
0.9	1535	01011111	1111
1.0	1697	01101010	0001
1.1	1853	01110011	1101

[1] I_{RECT} can be estimated using approximation formulas:
$I_{RECT} \approx ADC(12bit) / 1715$
$I_{RECT} \approx ADC(8bit) / 107$

Table 27. DC-to-DC converter output voltage coding, channel ADC2Dx, V_{DCOUT}

Channel electrical value	ADC readout,	ADC2DU 0Dh[7:0]b	ADC2DL 13h[3:0]b
V_{DCOUT} [V]	decimal code	upper byte, binary code	lower nibble, binary code
4.2	1566	01100001	1110
4.4	1642	01100110	1010
4.6	1716	01101011	0100
4.8	1792	01110000	0000
5.0	1866	01110100	1010
5.2	1941	01111001	0101
5.4	2016	01111110	0000
5.6	2091	10000010	1011
5.8	2166	10000111	0110
6.0	2240	10001100	0000
6.2	2315	10010000	1011

The DC-to-DC converter current readout offers only 7 effective bits.

Table 28. DC-to-DC converter output current coding, channel ADC3Dx, I_{DCOUT}

Channel electrical value	ADC3DU 0Eh[7:0]d	ADC3DU 0Eh[7:0]b
I_{DCOUT} [A] (average)[1]	upper byte, decimal code	upper byte, binary code
0.06	35	00100011
0.14	39	00100111
0.23	43	00101011
0.32	47	00101111
0.42	51	00110011
0.51	55	00110111
0.61	59	00111011
0.70	63	00111111
0.79	67	01000011
0.89	71	01000111
1.0	75	01001011
1.1	79	01001111
1.2	83	01010011
1.3	87	01010111
1.4	91	01011011

[1] I_{DCOUT} is the nominal value for the maximum average output current when the DC-to-DC converter is used with a 2.2 mH inductor for L1 in Figure 1. Accuracy of the limit is largely dependent upon the inductor value tolerance

Table 29. V_{NTC} voltage coding and temperature coding, channel ADC4Dx, V_{NTC}

Channel electrical value		ADC readout,	ADC4DU 0Fh[7:0]b	ADC4DL 14h[3:0]b
V_{NTC} [1] [V]	T_{amb} [°C] (10 kΩ B[1] = 3380)	decimal code	upper byte, binary code	lower nibble, binary code
3.05	−40	3783	11101100	0111
3.02	−35	3756	11101010	1100
3.00	−30	3723	11101000	1011
2.96	-25	3682	11100110	0010
2.92	-20	3630	11100010	1110
2.87	-15	3568	11011111	0000
2.81	-10	3494	11011010	0110
2.74	-5	3407	11010100	1111
2.66	0	3306	11001110	1010
2.57	5	3192	11000111	1000
2.47	10	3065	10111111	1001
2.36	15	2927	10110110	1111
2.24	20	2779	10101101	1011
2.11	25	2620	10100011	1100
1.98	30	2461	10011001	1101
1.85	35	2297	10001111	1001
1.72	40	2131	10000101	0011
1.59	45	1967	01111010	1111
1.46	50	1809	01110001	0001
1.34	55	1657	01100111	1001
1.22	60	1513	01011110	1001
1.11	65	1377	01010110	0001
1.01	70	1251	01001110	0011
0.91	75	1136	01000111	0000
0.83	80	1029	01000000	0101
0.75	85	931	00111010	0011
0.68	90	842	00110100	1010
0.61	95	762	00101111	1010
0.55	100	690	00101011	0010
0.50	105	624	00100111	0000
0.46	110	566	00100011	0110
0.41	115	513	00100000	0001
0.37	120	466	00011101	0010
0.34	125	423	00011010	0111

[1] Refer to the NTC parameters in Table 40, Block Diagram in Figure 1 and trimester circuit component values in Table 4.

The NTC temperature values can be approximated for the full 12-bit value by the formula:

$$ADC(12bit) = trunc(0.00191 \times T_{amb}{}^{3} - 0.225 \times T_{amb}{}^{2} - 22.76 \times T_{amb} + 3295)$$

The maximum error within the temperature range of −40 °C to +85 °C is < 3 %.

For the 8-bit MSB value, the approximation formula is:

$$ADC(8bit) = trunc(0.0001 \times T_{amb}{}^{3} - 0.0121 \times T_{amb}{}^{2} - 1.43 \times T_{amb} + 204)$$

The maximum error within the temperature range of −40 °C to +80 °C is < 3 %.

Table 30. V_{OTPx}, on-chip temperature sensor coding, channel ADC5Dx and ADC6Dx, V_{OTPx}

Channel Electrical Value	ADC readout,	ADCxDU 10h[7:0]b 11h[7:0]b	ADCxDL 14h[7:4]b 15h[3:0]b
T_j [°C]	decimal code	upper byte, binary code	lower nibble, binary code
−40	837	00110100	0101
−30	808	00110010	1000
−20	779	00110000	1011
−10	749	00101110	1101
0	720	00101101	0000
5	703	00101011	1111
10	689	00101011	0001
15	674	00101010	0010
20	659	00101001	0011
25	644	00101000	0100
30	630	00100111	0110
35	614	00100110	0110
40	600	00100101	1000
45	584	00100100	1000
50	569	00100011	1001
55	554	00100010	1010
60	540	00100001	1100
65	524	00100000	1100
70	509	00011111	1101
80	479	00011101	1111
90	449	00011100	0001
100	420	00011010	0100
110	389	00011000	0101
125	344	00010101	1000

7.10.4.8 DC-to-DC regulator control register (DCSEL, address 19h)

The DC-to-DC regulator control register configures the external supply DC-to-DC converter operation mode and output voltage.

Table 31. DC-to-DC voltage and current select register (DCSEL, address 19h)

Bit	7	6	5	4	3	2	1	0
Symbol	V3	V2	V1	V0	C3	C2	C1	C0
Default	0	1	0	0	1	0	1	1

Table 32. DC-to-DC voltage and current select register bit mapping (DCSEL, address 19h)

Symbol						Description
DC-to-DC peak current limit [1]						
	C3	C2	C1	C0	I_{nom} [2]	
	0	0	0	0	0.06 A	
	0	0	0	1	0.14 A	
	0	0	1	0	0.23 A	
	0	0	1	1	0.32 A	
	0	1	0	0	0.42 A	
	0	1	0	1	0.51 A	
	0	1	1	0	0.61 A	
	0	1	1	1	0.70 A	
	1	0	0	0	0.79 A	
	1	0	0	1	0.89 A	
	1	0	1	0	1.0 A	
	1	0	1	1	1.1 A	default value
	1	1	0	0	1.2 A	
	1	1	0	1	1.3 A	
	1	1	1	0	1.4 A	
	1	1	1	1	1.5 A	
DC-to-DC output voltage select [1]						
	V3	V2	V1	V0	nominal output voltage	
	0	0	0	0	4.20 V	
	0	0	0	1	4.40 V	
	0	0	1	0	4.60 V	
	0	0	1	1	4.80 V	
	0	1	0	0	5.00 V	default value
	0	1	0	1	5.20 V	
	0	1	1	0	5.40 V	
	0	1	1	1	5.60 V	
	1	0	0	0	5.80 V	
	1	0	0	1	6.00 V	
	1	0	1	0	6.20 V	
other codes					5.00 V	

[1] Contact NXP if there is a requirement for the use of another inductor value than 2.2 mH.

[2] I_{nom} is the nominal value for the maximum average output current when the DC-to-DC converter is used with a 2.2 mH inductor for L1 in Figure 1. Accuracy of the limit is largely dependent upon the inductor value tolerance.

7.10.4.9 NTC temperature limit control register (NTCSEL, address 1Ah)

The NTC interrupt temperature control register allows for selecting the trigger points for NTCU (NTC high limit temperature ($T_{th(high)NTC}$)) and NTCL (NTC low limit temperature ($T_{th(low)NTC}$)).

Table 33. NTC interrupt level temperature control register (NTCSEL, address 1Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	[1]	[1]	NTCUL1	NTCUL0	[1]	[1]	NTCLL1	NTCLL0
Default	0	0	0	1	0	0	0	1

Table 34. NTC interrupt level temperature control register bit mapping (NTCSEL, address 1Ah)

Bits		Description
NTCUL1	NTCUL0	NTCU (upper temperature) trigger $\overline{INT}$ level
0	0	55 °C
0	1	60 °C (default)
1	0	65 °C
1	1	70 °C
NTCLL1	NTCLL0	NTCL (lower temperature) trigger $\overline{INT}$ level
0	0	0 °C
0	1	5 °C (default)
1	0	10 °C
1	1	15 °C

[1] Always write logic 0 to undefined bits.

7.10.4.10 Device identification code (DEVID, address 1Fh)

The device identification code stores a unique identifier for each version and/or revision of a NX2A4WP, so that the connected MCU recognizes it automatically.

Table 35. Device identification code register (DEVID, address 1Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	DEVID7	DEVID6	DEVID5	DEVID4	DEVID3	DEVID2	DEVID1	DEVID0
Default	0	1	0	0	0	0	0	0

7.10.5 Bus transactions[2]

The NX2A4WP is an I²C-bus slave device. Data is exchanged between the master and the NX2A4WP slave through read and write transactions on the I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines are connected to the VOUT18 supply via integrated 2.1 kΩ resistors. Data transfer may be initiated only when the bus is not busy.

7.10.5.1 Write commands

Data is transmitted to the NX2A4WP by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see Figure 10 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. If the auto increment bit AUTO is set to logic 1, the register address receiving the data is increased with every acknowledge of the slave. The example below shows a single write to a hypothetical port register at address 01h.

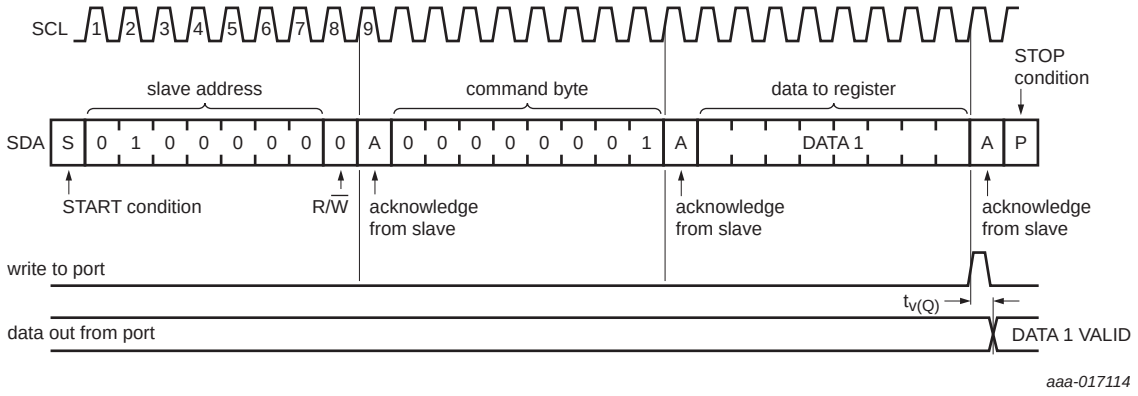


Fig 13. Write to registers

2. Reference: 'I²C-bus specification and user manual', UM10204, Rev. 06, 4 April 2014

7.10.5.2 Read commands

To read data from the NX2A4WP, the bus master must first send the NX2A4WP slave address with the least significant bit set to a logic 0 (see Figure 10 for device address). The command byte (sent after the address) determines which register is to be accessed.

After a restart the device address is sent again, but this time the LSB is set to a logic 1. The NX2A4WP slave sends the data from the register defined by the command byte (see Figure 14). If AUTO is set to logic 1, the address counter is incremented with every acknowledge from the master. If AUTO is logic 0, every data read accesses the same register address.

Data is clocked into the output shift register on the rising edge of the ACK clock pulse. There is no limit on the number of data bytes in one read transmission. However, on the final byte, the bus master must not acknowledge the data.

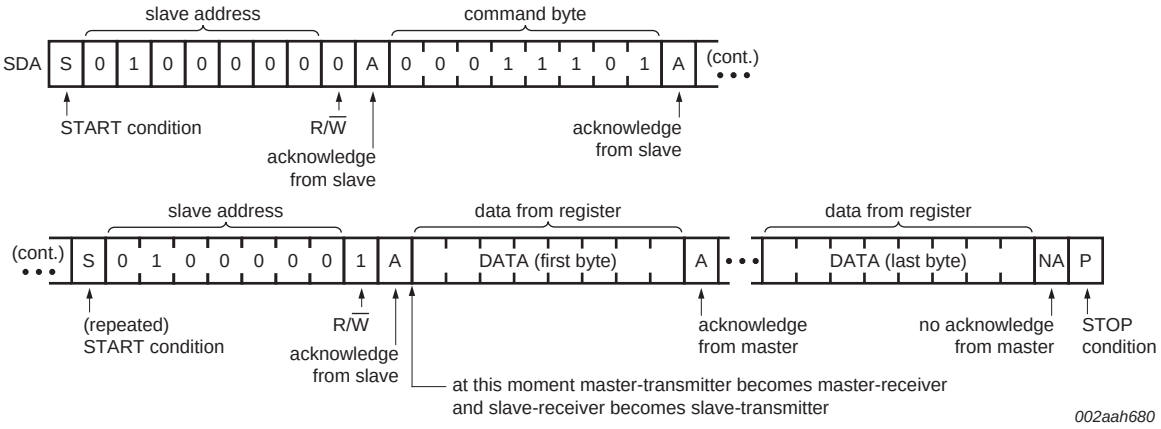


Fig 14. Read from register

7.10.6 Reserved registers (20h to FFh)

The reserved registers are not for customer use. Do not write to these registers.

8. Recommended operating conditions

Table 36. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	AC1, AC2 [1]	6.1	18	V
$V_{O(rect)}$	rectifier output voltage	DC output voltage [2]	4.3	13.7	V
T_{amb}	ambient temperature		−40	+85	°C

[1] A voltage level below 6.1 V is not recommended. The device might not be able to provide the maximum power in combination with nominal output voltage at the highest possible efficiency. A voltage level above 18 V triggers the protection circuit

[2] Refer to the A4WP BSS1.2 $V_{RX\_OC\_HIGH}$ specification.

9. Characteristics

Table 37. Static characteristics

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	SDA, SCL	1.26	-	-	V
		input1; GPIOx	2.3	-	-	V
		input2; TA	1.7	-	-	V
V_{IL}	LOW-level input voltage	SDA, SCL	−0.5	-	+0.54	V
		input1; GPIOx	−0.5	-	+1	V
		input2; TA	−0.5	-	+0.4	V
$V_{I(hys)}$	hysteresis of input voltage		-	0.2	-	V
V_{OL}	LOW-level output voltage	$\overline{INT}$, SDA; I_I = 4 mA	-	-	0.4	V
		GPIOx; I_I = 200 mA	-	-	0.5	V
$V_{startup}$	start-up voltage	$V_{O(rect)}$ for LDOs	-	3.8	-	V
$V_{startup(hys)}$	start-up voltage hysteresis	$V_{O(rect)}$ for LDOs	-	500	-	mV
$V_{trip(bo)}$	brownout trip voltage		-	3.3	-	V
$V_{bo(hys)}$	brownout voltage hysteresis	DC-to-DC supply	-	1.5	-	V
V_{DD}	supply voltage	$V_{O(rect)}$ supply voltage level (LDRECT pin) for DC-to-DC start-up	-	6.5	-	V
V_{en}	enable voltage	I^2C transceiver; at LDRECT	-	4.3	-	V
		ADC; at LDRECT	-	4.3	-	V
$V_{ovd(en)}$	enable over-voltage detection voltage	pin RECT; over-power protection; GPIO1 & GPIO2 low impedance	17	18	19	V
$V_{ovd(dis)}$	disable over-voltage detection voltage	pin RECT; over-power protection; GPIO1 & GPIO2 low impedance	-	17	-	V
$V_{ovp(en)}$	enable over-voltage protection voltage	rectifier is disabled and both AC input ports are shorted to ground and/or over-power protection is enabled	19	20	21.5	V
$V_{ovp(dis)}$	disable over-voltage protection voltage	pin RECT	-	19	-	V
$V_{ovp(hys)}$	overvoltage protection voltage hysteresis	pin RECT; $V_{ovp(en)}$ and $V_{ovd(en)}$	-	1	-	V
T_j	junction temperature	over-temperature trigger	-	125	-	°C
$T_{j(hys)}$	junction temperature hysteresis	over-temperature	-	25	-	°C
$T_{th(high)NTC}$	NTC high threshold temperature		55	60	70	°C
$T_{th(low)NTC}$	NTC low threshold temperature		0	5	15	°C

Table 37. Static characteristics *...continued*

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_q	quiescent current	V_{DCIN} = 8 V = $V_{O(rect)}$; I_{LDO18}, I_{LDO33} = 0 mA; ADC and I^2C enabled	-	-	-	-
		DC-to-DC disabled	-	3.5	-	mA
		DC-to-DC enabled V = 0 mA	-	12	-	mA
$R_{pu(int)}$	internal pull-up resistance	internal $\overline{INT}$ pull-up resistor value	-	20	-	kΩ
		internal SCL, SDA pull-up resistor value	-	2.1	-	kΩ

Table 38. Electrical characteristics LDOs

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	OUT33; I_O = 1 mA	3	3.3	3.6	V
		OUT18; I_O = 1 mA	1.755	1.800	1.860	V
$t_{startup}$	start-up time	OUT33; $V_{O(rect)}$ = 4.5 V	-	2.1	-	ms
		OUT18; $V_{O(rect)}$ = 4.5 V	-	2.0	-	ms
t_r	rise time	start-up ramp: OUT33; $V_{O(rect)}$ = 4.5 V C_{VOUT33} = suggested applications component I_{VOUT33} = 0 A	-	155	-	ms
		start-up ramp: OUT18; $V_{O(rect)}$ = 4.5 V C_{VOUT18} = suggested applications component I_{VOUT33} = 0 A	-	60	-	ms
$I_{O(max)}$	maximum output current	OUT33; V_O = 0.975 × V	100	-	-	mA
		OUT18; V_O = 0.975 × V	100	-	-	mA

[1] The maximum output current I_{ODC} depends on the total power consumption of the device. It is limited by the voltage drop from the incoming DC voltage $V_{O(rect)}$. The power dissipation of the two external supply LDO can be calculated to: $P_{LDO} = (V_{O(rect)} - V_{OUT33})*I_{OUT33} + (V_{O(rect)} - V_{OUT18})*I_{OUT18}$.

[2] Under overload conditions, the LDO maximum current folds back to provide the short circuit protection.

Table 39. Electrical characteristics: DC-to-DC buck converter

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC-to-DC buck regulator						
V_O	output voltage	DC-to-DC converter output voltage; Register 19h[7:3]=00100 (default) [1] [2]	-	5.0	-	V
$V_{O(step)}$	output voltage step size	programmable V_O	-	0.2	-	V

Table 39. Electrical characteristics: DC-to-DC buck converter *…continued*

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{step}	number of steps	programmable V_O	-	11	-	
V_O	output voltage	programmable output voltage range	4.2	–	6.2	V
$I_{O(max)}$	maximum output current	L1 = suggested applications component [2] register 19h[3:0]=1011 (default)	-	1.1	-	A
N_{step}	number of steps	number of programmable I_{OUT} steps	-	16	-	
I_O	output current	programmable output current range	0.06	-	1.5	A
t_{en}	enable time	V_O start-up time after enable command I^2C command until LX switching; $V_{O(rect)}$ = 6.5 V	-	0.6	-	ms
t_r	rise time	10 % to 90 % of the output swing; $V_{O(rect)}$= 6.5 V C_{VOUT} = suggested applications component I_{VOUT} = 0 A	-	0.3	-	ms

[1] $V_{O(nom)}$ = nominal output voltage (I^2C programmable).

[2] If the load current exceeds $I_{Olim(nom)}$, the DC-to-DC output voltage drops below V_{Onom}.

Table 40. Electrical characteristics: ADC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{res(ADC)}$	ADC resolution		-	12	-	bit
DNL	differential non-linearity	Using 5 % to 95 % of full scale linear fit	-	±1	-	LSB
INL	integral non-linearity	Using 5 % to 95 % of full scale linear fit	-	±5	-	LSB
E_O	offset error	Using 5 % to 95 % of full scale linear fit	-	±2	-	LSB
E_G	gain error	Using 5 % to 95 % of full scale linear fit	-	±0.65	-	%FS
f_s	sampling frequency		-	187	-	kHz
f_{clk}	clock frequency		-	6	-	MHz
$E_{res(ADC)}$	ADC resolution error	12-bit; −40 °C ≤ T_j ≤ +125 °C				
		ADC0Dx; $V_{O(rect)}$	-	-	±3	%
		ADC1Dx; $I_{O(rect)}$ [2]	-	-	±8	%
		ADC2Dx; V_{DCOUT}	-	-	±3	%
Internal temperature measurement						
T_j	junction temperature	device temperature range	−40	-	+125	°C
T_{acc}	temperature accuracy	0 °C to +85 °C	-	±3	-	°C
		−40 °C to +125 °C	-	±3	±5	°C
T_{res}	temperature resolution		-	0.4	-	°C

Table 40. Electrical characteristics: ADC *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NTC temperature measurement						
$V_{ref(VREF33)}$	reference voltage on pin VREF33	NTC supply; I_{load} = 150 μA	3.22	3.3	3.38	V
V_I	input voltage	temperature channel input voltage range; I_{load} = 0 A	0.28	-	3.1	V
T_{acc}	temperature accuracy	0 °C to +85 °C	-	±3	-	°C
		–40 °C to +125 °C	-	±3	±5	°C
T_{res}	temperature resolution		-	0.04	-	°C
R_{25}	thermistor resistance (25°C)	NTCs resistance at 25 °C	-	10	-	kΩ
$B_{25/50}$	thermal sensitivity index B25/50	NTCs B-constant (25/50 °C)[4]	-	3380	-	K
$R_{bias(s)}$	series bias resistance		-	5	-	kΩ
$R_{bias(par)}$	parallel bias resistance		-	80	-	kΩ

[1] I_{DCOUT} is the nominal value for the maximum average output current when the DC-to-DC converter is used with a 2.2 μH inductor for L1 in Figure 1. Accuracy of the limit is largely dependent upon the inductor value tolerance

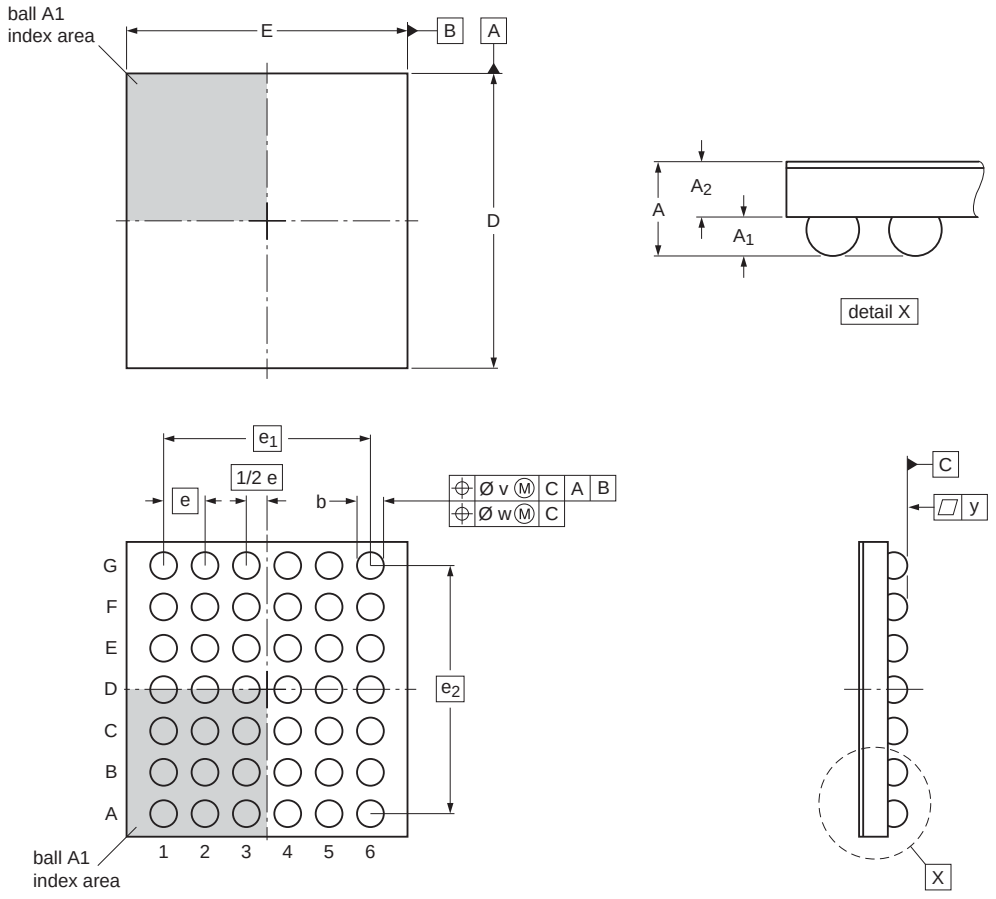
[2] At lower currents the maximum of $I_{O(rect)}$ accuracy is 50 mA.

[3] At lower currents the I_{DCOUT} accuracy is typically 3 LSB.

[4] $$B = \frac{ln(R/R_0)}{1/T - 1/T_0}$$

10. Package outline

WLCSP42: wafer level chip-scale package; 42 bumps; 3.56 x 3.41 x 0.57 mm (backside coating included) **NX2A4WP**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.61	0.26	0.37	0.34	3.58	3.43						
mm	nom	0.57	0.23	0.34	0.32	3.56	3.41	0.5	2.5	3.0	0.15	0.05	0.03
	min	0.53	0.20	0.31	0.30	3.54	3.39						

wlcsp42_nx2a4wp_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NX2A4WP						~~15-03-03~~ 15-03-10

Fig 15. Package outline WLCSP42

11. Soldering of WLCSP packages

A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 “Wafer Level Chip Scale Package” and in application note AN10365 “Surface mount reflow soldering”.

12. Abbreviations

Table 41. Abbreviations

Acronym	Description
A4WP	Alliance For Wireless Power (Rezence)
ADC	Analog-to-Digital Converter
BOD	Brown Out Detection
BT-LE	Bluetooth Low Energy
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
ISR	Interrupt Service Request
LDO	Low-Dropout Regulator
LSB	Least Significant Bit
MCU	Micro-Controller Unit
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NTC	Negative Temperature Coefficient
OCP	Over current protection
OTP	Over-temperature protection
OVP	Over-voltage protection
PMU	Power management Unit
POR	Power-On Reset
SCL Line	Serial Clock Line
SDA Line	Serial Data Line
UVLO	Under-voltage lockout
VBUS	USB Power Supply

13. Revision history

Table 42. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX2A4WP_SDS v.3	20150804	Product short data sheet	-	NX2A4WP_SDS v.2
NX2A4WP_SDS v.2	20150709	Objective short data sheet	-	NX2A4WP_SDS v.1
NX2A4WP_SDS v.1	20150420	Objective short data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

16. Contents

For more information, please visit: http://www.nxp.com
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