



# PSMN1R2-55SLH

N-channel 55 V, 1.03 mOhm, 330 A logic level Application Specific MOSFET in LFPAK88

28 February 2022

Product data sheet

## 1. General description

330 Amp continuous current, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK88 package. Part of the ASFETs for Battery Isolation and DC Motor control family and using Nexperia's unique "SchottkyPlus" technology delivers high efficiency and low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. The ASFET is particularly suited to 36 V battery powered applications requiring strong avalanche capability, linear mode performance, use at high switching frequencies, and also safe and reliable switching at high load-current.

## 2. Features and benefits

- 330 Amp continuous current capability
- LFPAK88 (8 x 8 mm) LFPAK-style low-stress exposed lead-frame for ultimate reliability, optimum soldering and easy solder-joint inspection
- Copper-clip and solder die attach for low package inductance and resistance, and high  $I_{D(max)}$  rating
- Ideal replacement for D2PAK and 10 x 12 mm leadless package types
- Qualified to 175 °C
- Avalanche rated, 100 % tested
- Low  $Q_G$ ,  $Q_{GD}$  and  $Q_{OSS}$  for high efficiency, especially at higher switching frequencies
- Superfast switching with soft body-diode recovery for low-spiking and ringing, recommended for low EMI designs
- Unique "SchottkyPlus" technology for Schottky-like switching performance and low  $I_{DSS}$  leakage
- Narrow  $V_{GS(th)}$  rating for easy paralleling and improved current sharing
- Very strong linear-mode / safe operating area characteristics for safe and reliable switching at high-current conditions

## 3. Applications

- Brushless DC motor control
- Synchronous rectifier in high-power AC-to-DC applications, e.g. server power supplies
- Battery protection
- eFuse and load switch
- Hotswap / in-rush current management
- 10 cell lithium-ion battery applications (36 V – 42 V)

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	55	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	330	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	375	W
$T_j$	junction temperature		-55	-	175	°C

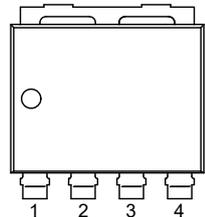
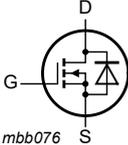
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	0.81	1.03	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	0.9	1.22	mΩ
<b>Dynamic characteristics</b>						
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 27 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	28	62	nC
Q <sub>G(tot)</sub>	total gate charge		-	116	180	nC

[1] 330A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFPAK88 (SOT1235)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R2-55SLH	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R2-55SLH	X1H2L55S

## 8. Limiting values

Table 5. Limiting values

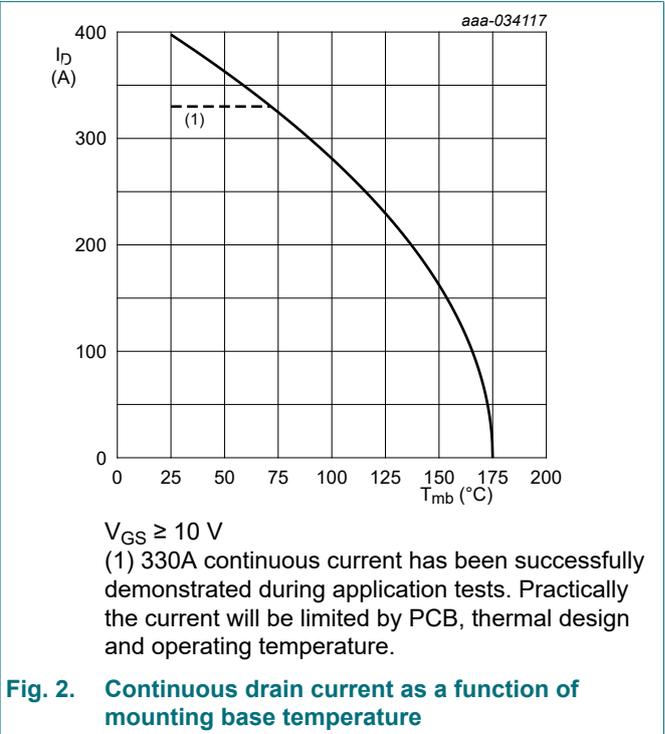
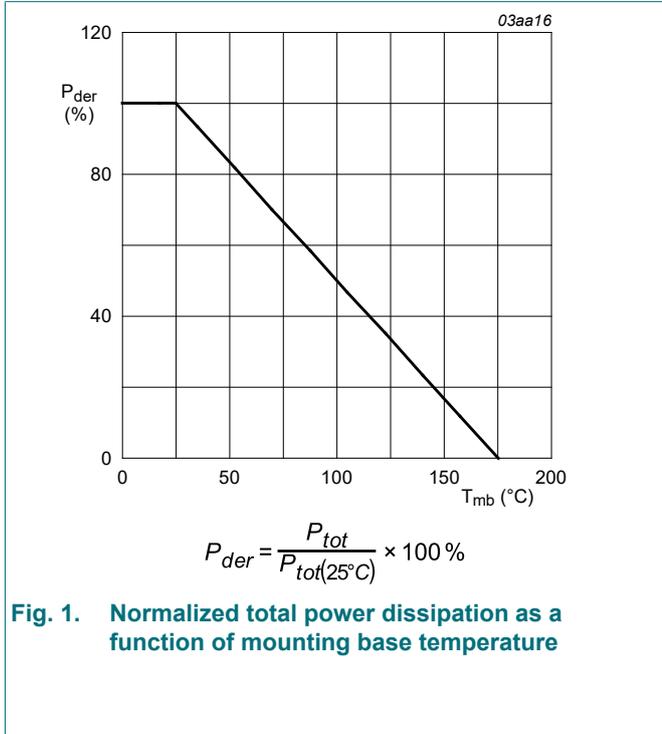
In accordance with the Absolute Maximum Rating System (IEC 60134).

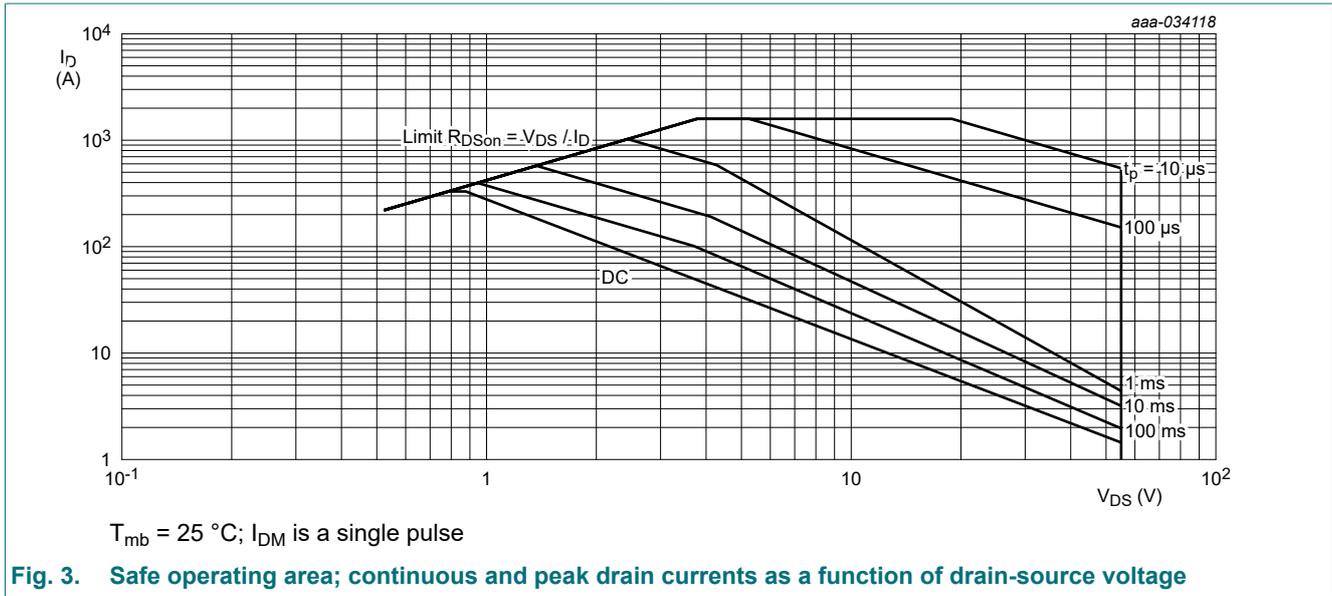
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	55	V
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	55	V
V <sub>GS</sub>	gate-source voltage		-20	20	V

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Symbol	Parameter	Conditions		Min	Max	Unit
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; Fig. 1		-	375	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ }^{\circ}\text{C}$ ; Fig. 2	[1]	-	330	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ }^{\circ}\text{C}$ ; Fig. 2		-	284	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ }^{\circ}\text{C}$ ; Fig. 3		-	1588	A
$T_{stg}$	storage temperature			-55	175	$^{\circ}\text{C}$
$T_j$	junction temperature			-55	175	$^{\circ}\text{C}$
$T_{slid(M)}$	peak soldering temperature			-	260	$^{\circ}\text{C}$
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$		-	330	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ }^{\circ}\text{C}$		-	1588	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 50\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; unclamped; $t_p = 1.5\text{ ms}$	[2]	-	2.6	J
		$I_D = 25\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; unclamped; $t_p = 7.2\text{ ms}$	[2]	-	6.4	J
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 55\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $R_{GS} = 50\text{ }\Omega$	[2]	-	140	A

- [1] 330A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

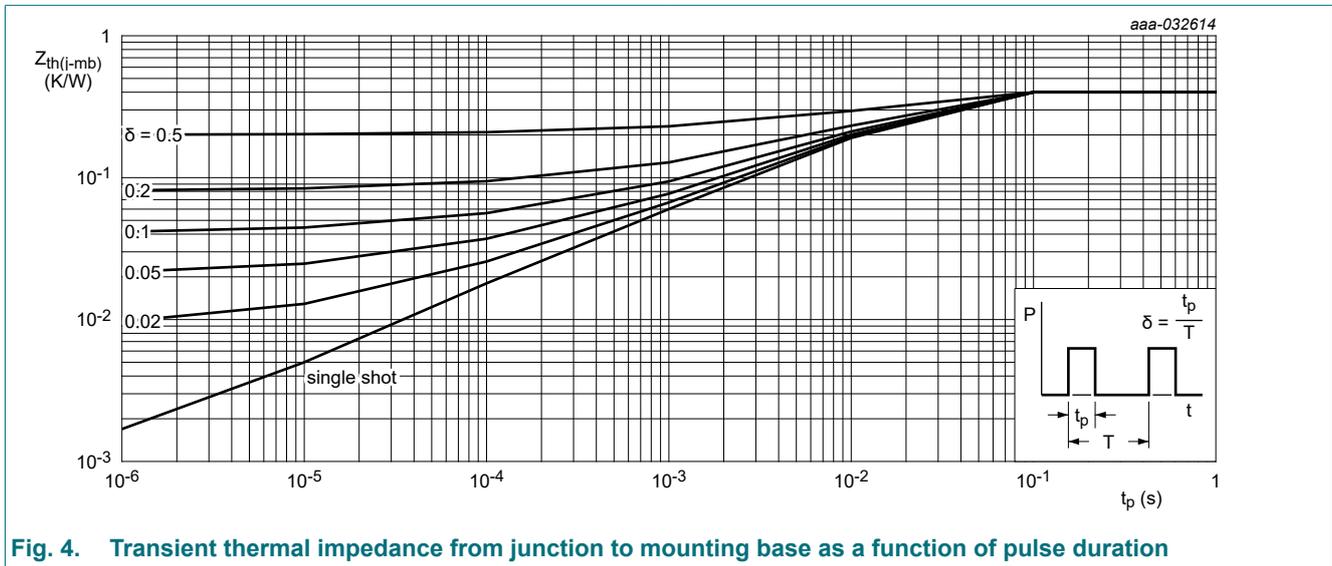


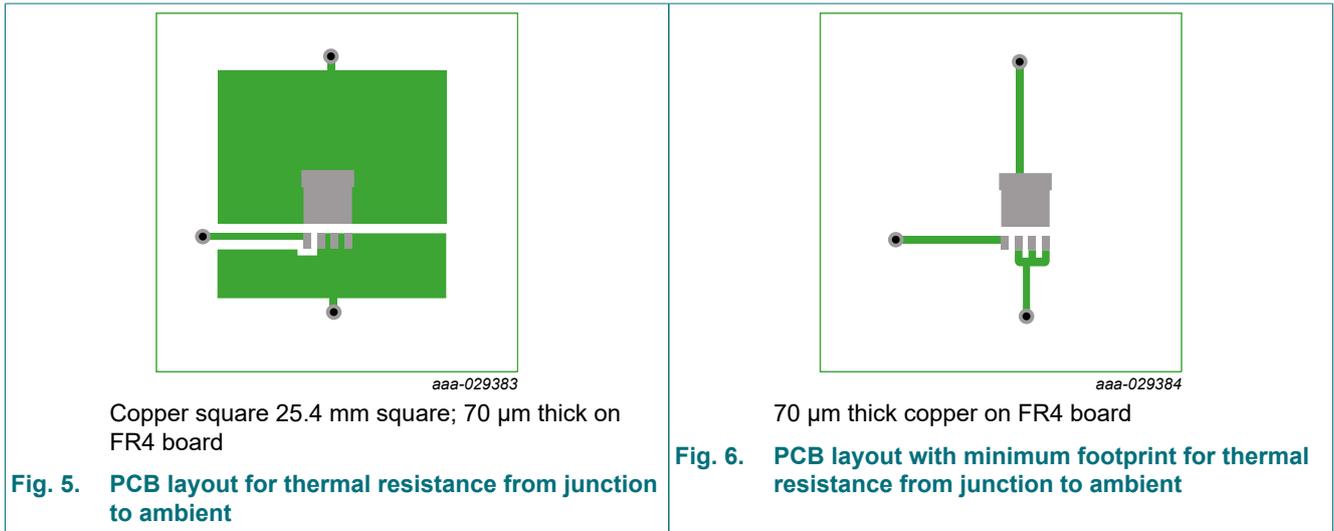


### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.35	0.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	35	-	K/W
		Fig. 6	-	70	-	K/W





## 10. Characteristics

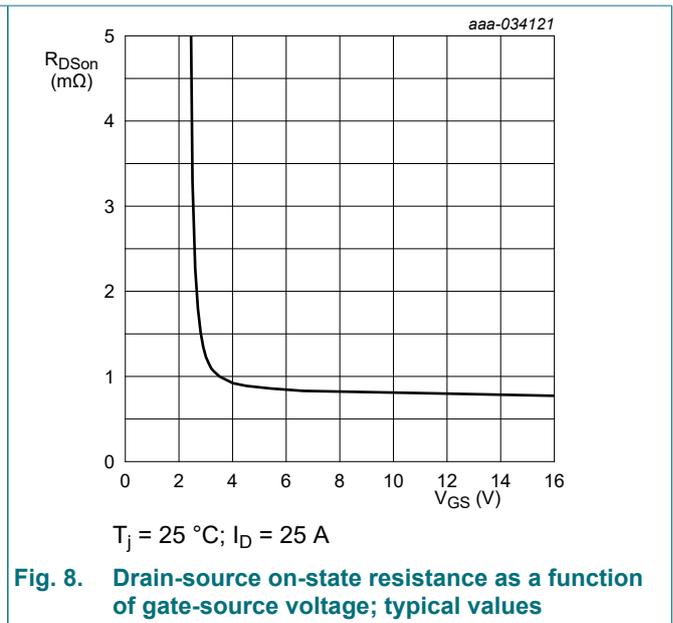
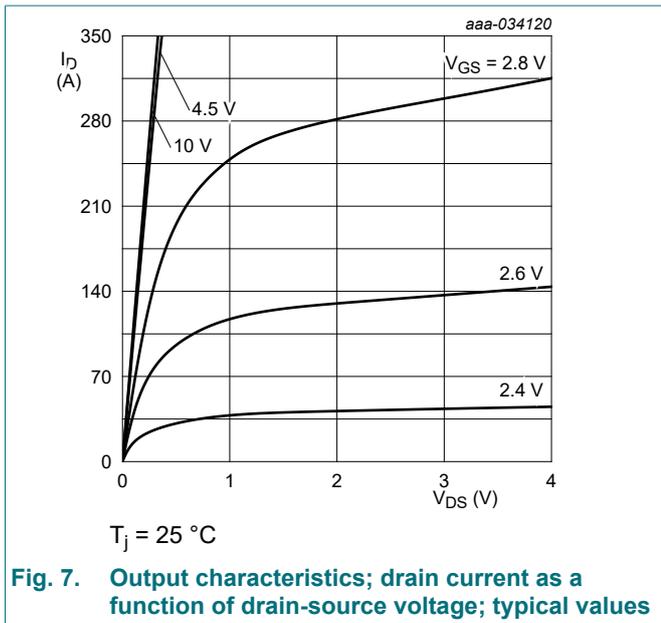
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	55	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	49.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.6	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.8	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 44 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	$\mu A$
		$V_{DS} = 44 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	6.7	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	0.81	1.03	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	2.1	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	0.9	1.22	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	2.5	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.4	1	2.5	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 27 \text{ V}; V_{GS} = 4.5 \text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	116	180	nC
		$I_D = 25 \text{ A}; V_{DS} = 27 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	255	395	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	141	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 27\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	35	53	nC	
$Q_{GS(th)}$	pre-threshold gate-source charge		-	24	36	nC	
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	11	17	nC	
$Q_{GD}$	gate-drain charge		-	28	62	nC	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 27\text{ V};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	2.4	-	V	
$C_{iss}$	input capacitance	$V_{DS} = 27\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 14</a>	-	18409	25773	pF	
$C_{oss}$	output capacitance		-	1411	1975	pF	
$C_{riss}$	reverse transfer capacitance		-	469	1126	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 27\text{ V}; R_L = 1.1\text{ }\Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$	-	75	-	ns	
$t_r$	rise time		-	70	-	ns	
$t_{d(off)}$	turn-off delay time		-	140	-	ns	
$t_f$	fall time		-	58	-	ns	
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 27\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	82	-	nC	
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	0.73	1	V	
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 27\text{ V};$ <a href="#">Fig. 16</a>	-	48	-	ns	
$Q_r$	recovered charge		[1]	-	66	-	nC
$t_a$	reverse recovery rise time		-	-	29	-	ns
$t_b$	reverse recovery fall time		-	-	19	-	ns

[1] includes capacitive recovery



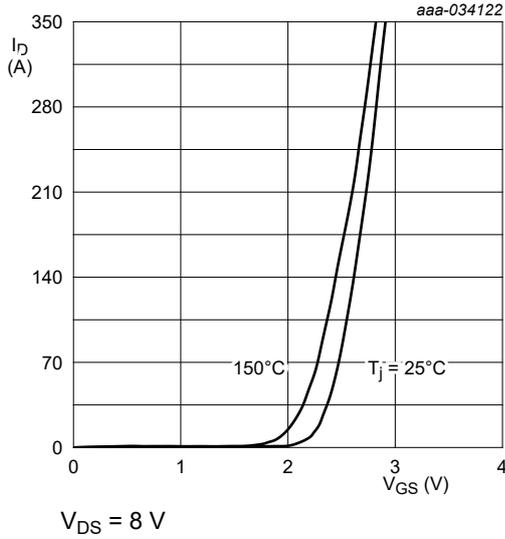


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

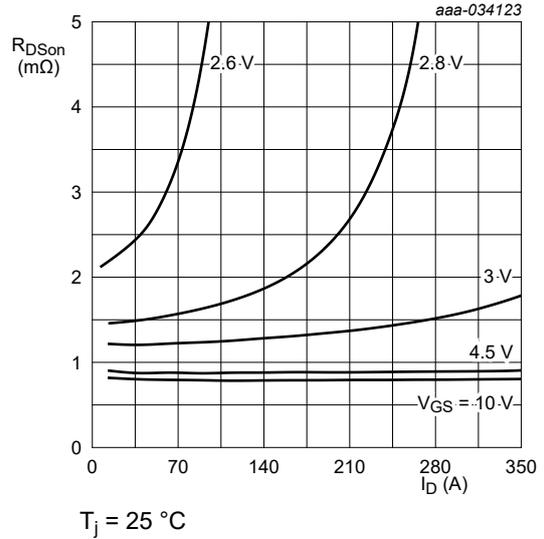


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

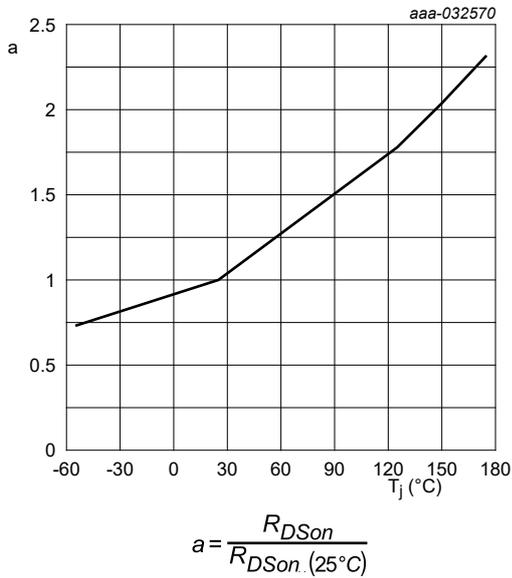


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

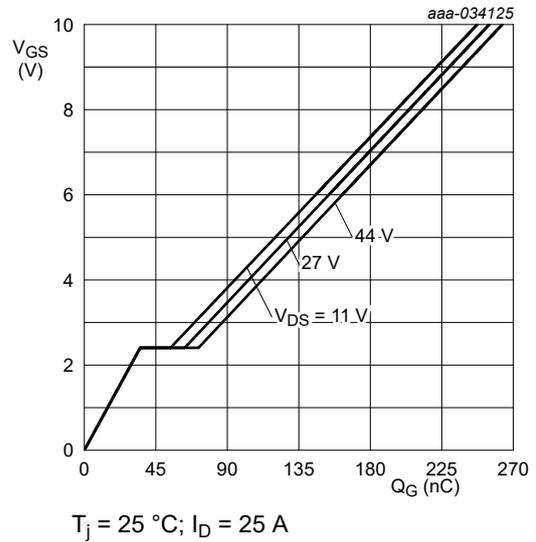


Fig. 12. Gate-source voltage as a function of gate charge; typical values

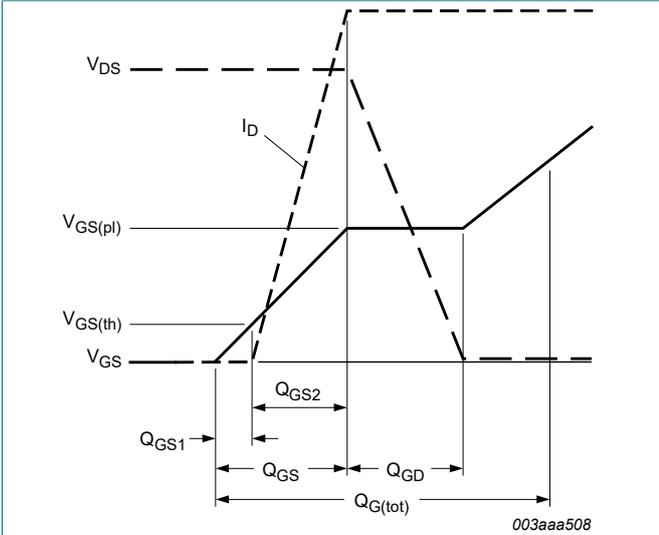


Fig. 13. Gate charge waveform definitions

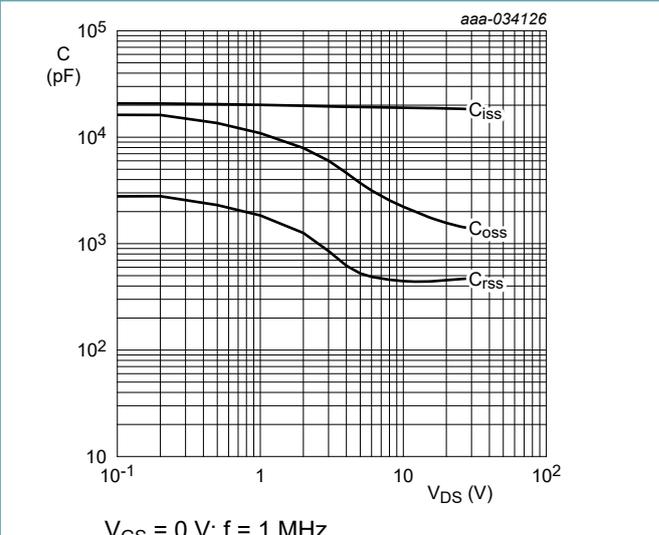


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

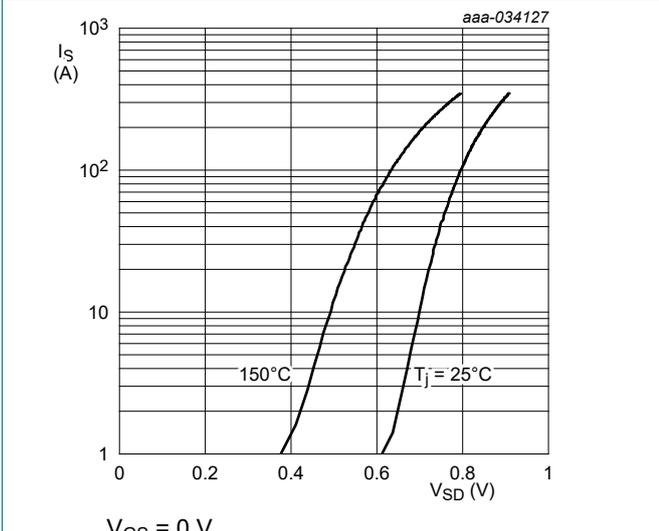


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

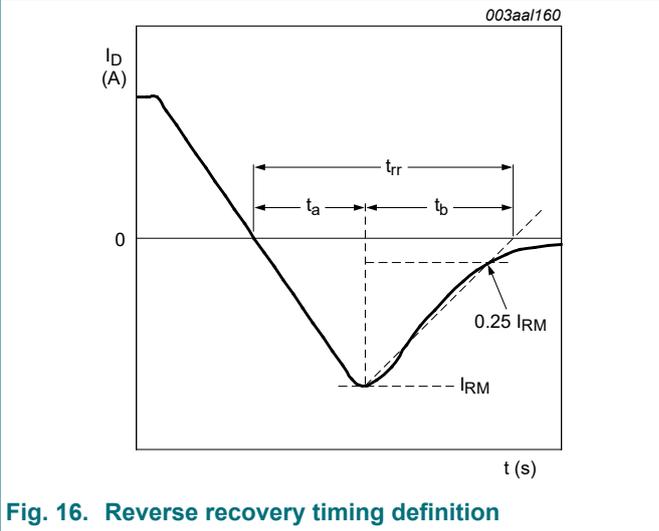


Fig. 16. Reverse recovery timing definition

### 11. Package outline

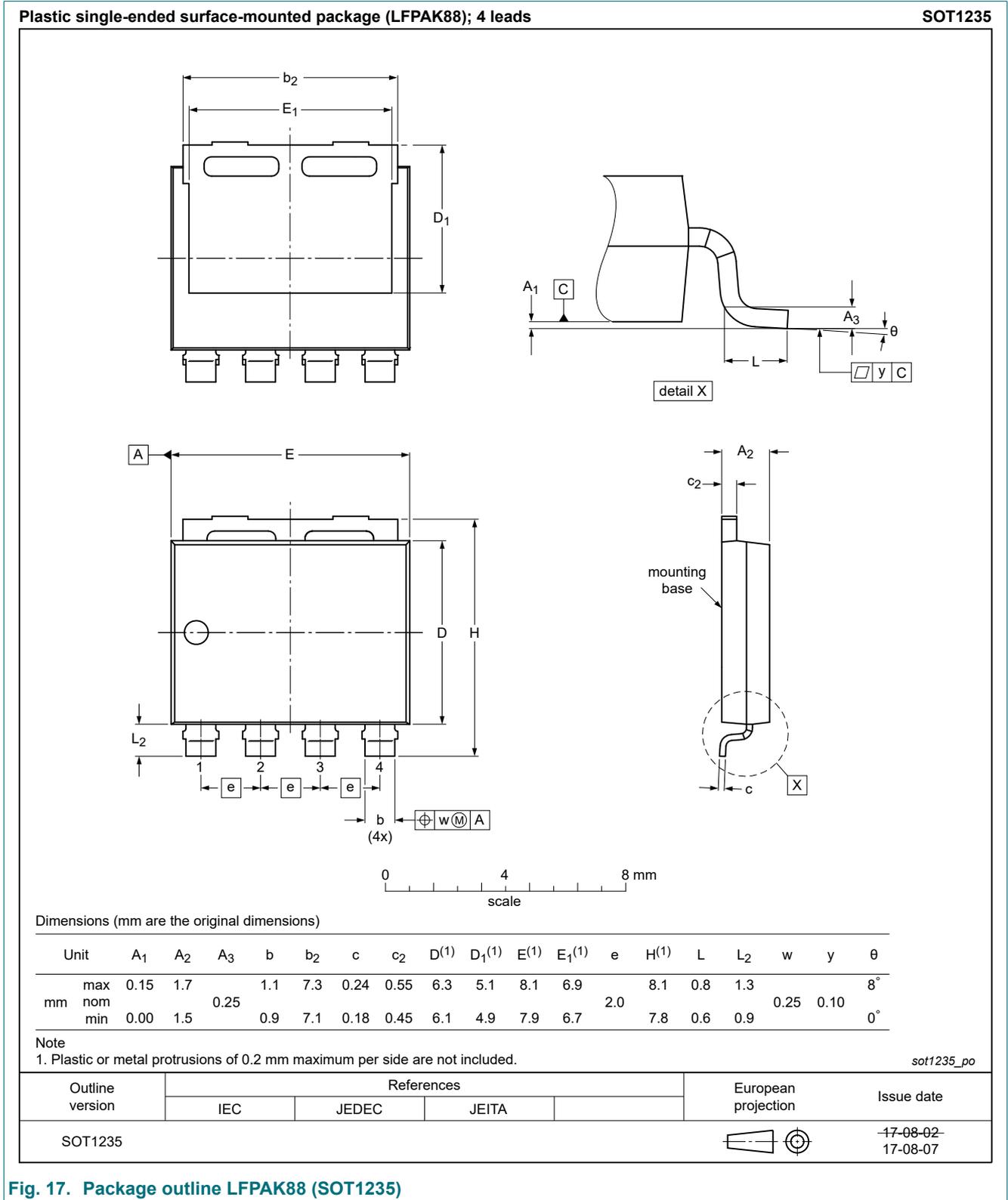
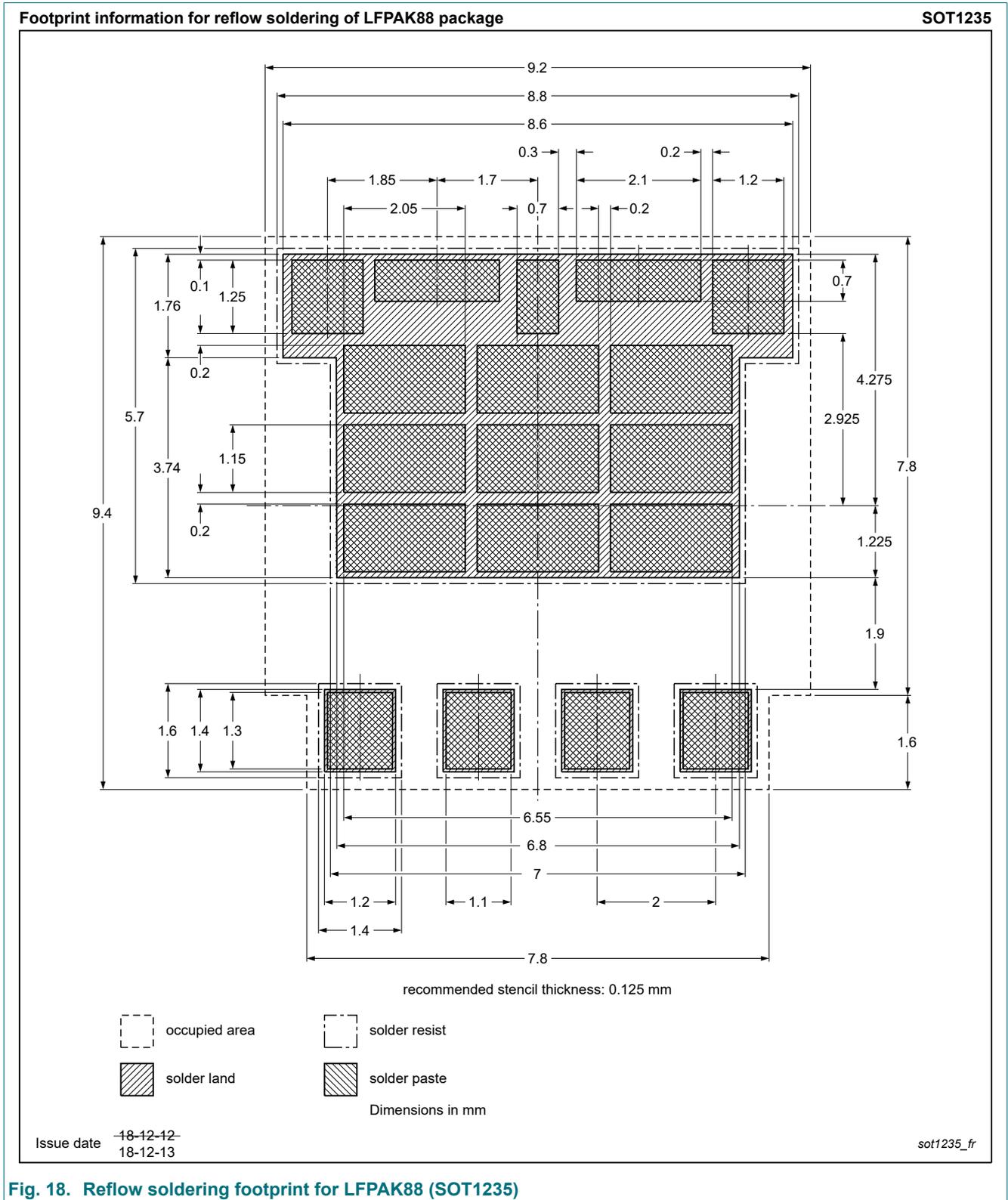


Fig. 17. Package outline LPAK88 (SOT1235)

## 12. Soldering



**Fig. 18. Reflow soldering footprint for LPAK88 (SOT1235)**

## 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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