

**PRODUCT SUMMARY** 

V<sub>DSS</sub>

R<sub>DS(on)</sub>

 $I_D$ 

Туре

Package

## VS-FA38SA50LCP

**Vishay Semiconductors** 

# Power MOSFET, 38 A

### FEATURES

- Fully isolated packageEasy to use and parallel
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- Low on-resistance
- Dynamic dV/dt rating
- Fully avalanche rated
- Simple drive requirements
- Low drain to case capacitance
- Low internal inductance
- UL approved file E78996
- Designed for industrial level
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

#### DESCRIPTION

Third Generation Power MOSFETs from Vishay Semiconductors provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-227 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 500 W. The low thermal resistance of the SOT-227 contribute to its wide acceptance throughout the industry.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain current at VGS 10 V	1-	T <sub>C</sub> = 25 °C	38	
Continuous drain current at V <sub>GS</sub> 10 V	ID	T <sub>C</sub> = 100 °C	24	A
Pulsed drain current	I <sub>DM</sub> <sup>(1)</sup>		150	
Power dissipation	PD	T <sub>C</sub> = 25 °C	500	W
Linear derating factor			4.0	W/°C
Gate to source voltage	V <sub>GS</sub>		± 20	V
Single pulse avalanche energy	E <sub>AS</sub> <sup>(2)</sup>		580	mJ
Avalanche current	I <sub>AR</sub> <sup>(1)</sup>		38	А
Repetitive avalanche energy	E <sub>AR</sub> <sup>(1)</sup>		50	mJ
Peak diode recovery dV/dt	dV/dt <sup>(3)</sup>		10	V/ns
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>Stg</sub>		- 55 to + 150	°C
Insulation withstand voltage (AC-RMS)	V <sub>ISO</sub>		2.5	kV
Mounting torque		M4 screw	1.3	Nm

#### Notes

<sup>(1)</sup> Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

 $^{(2)}$  Starting T\_J = 25 °C, L = 0.80 mH, R\_g = 25  $\Omega,$  I\_AS = 38 A (see fig. 12)

 $^{(3)}$   $I_{SD} \leq 38$  Å,  $dI/dt \leq 410$  Å/µs,  $V_{DD} \leq \breve{V}_{(BR)DSS}, \, T_J \leq 150~^\circ C$ 

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Pb-free BoHS

COMPLIANT



500 V

0.13 Ω

38 A

Modules - MOSFET

SOT-227



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## VS-FA38SA50LCP

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THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Junction and storage temperature range	T <sub>J</sub> , T <sub>Stg</sub>		- 55	-	150	°C
Junction to case	R <sub>thJC</sub>		-	-	0.25	°C/W
Case to heatsink	R <sub>thCS</sub>	Flat, greased surface	-	0.05	-	0/10
Weight			-	30	-	g
Mounting torque			-	-	1.3	Nm
Case style	SOT-227					

<b>ELECTRICAL CHARACTERISTCS</b> (T <sub>J</sub> = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1.0 mA	500	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	Reference to 25 °C, $I_D = 1 \text{ mA}$	-	0.66	-	V/°C
Static drain to source on-resistance	R <sub>DS(on)</sub> <sup>(1)</sup>	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 23 \text{ A}$	-	-	0.13	Ω
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	2.0	-	4.0	V
Forward transconductance	g <sub>fs</sub>	$V_{DS} = 25 \text{ V}, \text{ I}_{D} = 23 \text{ A}$	22	-	-	S
Durain to course lookense current	1	$V_{DS} = 500 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	50	
Drain to source leakage current	I <sub>DSS</sub>	$V_{DS} = 400 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$	-	-	500	μA
Gate to source forward leakage		V <sub>GS</sub> = 20 V	-	-	200	- 0
Gate to source reverse leakage	– I <sub>GSS</sub>	V <sub>GS</sub> = - 20 V	-	-	- 200	nA
Total gate charge	Qg	I <sub>D</sub> = 38 A	-	280	420	
Gate to source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 400 V		37	55	nC
Gate to drain ("Miller") charge	Q <sub>gd</sub>	$V_{GS}$ = 10 V; see fig. 6 and 13 <sup>(1)</sup>	-	150	220	1
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 250 V	-	42	-	
Rise time	t <sub>r</sub>	I <sub>D</sub> = 38 A	-	340	-	
Turn-off delay time	t <sub>d(off)</sub>	$R_g = 10 \Omega (ιντερναλ)$	-	200	-	ns
Fall time	t <sub>f</sub>	$R_D = 8 \Omega$ , see fig. 10 <sup>(1)</sup>	-	330	-	
Internal source inductance	L <sub>S</sub>	Between lead, and center of die contact	-	5.0	-	nH
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	-	6900	-	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 25 V$	-	1600	-	pF
Reverse transfer capacitance	C <sub>rss</sub>	f = 1.0 MHz, see fig. 5	-	580	-	1

#### Note

 $^{(1)}\,$  Pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$ 

SOURCE-DRAIN RATINGS AND CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS M		TYP.	MAX.	UNITS
Continuous source current (body diode)	IS	MOSFET symbol showing the integral reverse	-	-	38	A
Pulsed source current (body diode)	I <sub>SM</sub> <sup>(1)</sup>	p-n junction diode.	-	-	150	A
Diode forward voltage	V <sub>SD</sub> <sup>(2)</sup>	$T_J = 25 \text{ °C}, I_S = 38 \text{ A}, V_{GS} = 0 \text{ V}$	-	-	1.3	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 38 A; dl/dt = 100 A/µs <sup>(2)</sup>	-	830	1300	ns
Reverse recovery charge	Q <sub>rr</sub>	$r_{\rm J} = 25$ C, $r_{\rm F} = 36$ A, $u_{\rm F} u_{\rm f} = 100$ A/µs $\sim$		15	22	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by $L_{S} + L_{D}$ )				

#### Notes

<sup>(1)</sup> Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

<sup>(2)</sup> Pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

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<sup>1</sup> <sup>10</sup> <sup>100</sup> V<sub>DS</sub>, Drain-to-Source Voltage (V) Fig. 1 - Typical Output Characteristics



Fig. 2 - Typical Output Characteristics





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Gate to Source Voltage

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Fig. 7 - Typical Source Drain Diode Forward Voltage



Fig. 8 - Maximum Safe Operating Area



Fig. 9 - Basic Gate Charge Waveform



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Fig. 10 - Gate Charge Test Circuit



Fig. 11 - Switching Time Test Circuit



Fig. 12 - Switching Time Waveforms

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Fig. 14 - Unclamped Inductive Test Circuit







Fig. 16 - Maximum Avalanche Energy vs. Drain Current



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Fig. 17 - Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS}$  = 5V for Logic Level Devices

Fig. 18 - For N-Channel Power MOSFETs



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#### **ORDERING INFORMATION TABLE**

Device code



CIRCUIT CONFIGURATION					
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING			
Single switch no diode	S	G (2) $G (2)$ $G (2)$ $G (2)$ $G (2)$ $G (1-4)$ $C (3)$ $C$			

LINKS TO RELATED DOCUMENTS				
Dimensions	www.vishay.com/doc?95036			
Packaging information	www.vishay.com/doc?95037			



## **Outline Dimensions**

**Vishay Semiconductors** 

SOT-227

#### **DIMENSIONS** in millimeters (inches)



#### Notes

- Dimensioning and tolerancing per ANSI Y14.5M-1982
- Controlling dimension: millimeter



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