





Description

Vectron's VT-706 Temperature Compensated Crystal Oscillator (TCXO) is a quartz stabilized, Clipped sine wave or CMOS output, analog temperature compensated oscillator, operating off a 5.0 or 3.3 volt supply in a hermetically sealed 7.0 x 5.0 mm ceramic package.

Features

- 5.000 52.000MHz Output Frequency
- ±0.2ppm Temperature Stability
- Optional Frequency Tuning
- Fundamental Crystal Design
- Stratum 3 version available as a custom part number
- Gold over nickel contact pads
- Hermetically Sealed Ceramic SMD package
- Product is compliant to RoHS directive ¹⁰ and fully compatible with lead free assembly

Applications

- Femto Cells
- Base Stations
- IP Networking
- Global Positioning Systems
- Point to Point Radio
- Manpack Radio
- Test and Measurement

Block Diagram



Specifications

Parameter	Symbol	Min.	Тур	Max	Units	
Output Frequency ¹ , Ordering Option	f _o	5		52	MHz	
Supply Voltage ³ , Ordering Option	V _{DD}	+2	.8, +3.0, +3.3, +	5.0	V	
Supply Current	I _{DD}			3.5	mA	
Operating Temperature, Ordering Option	T _{OP}	0/55, -10/70, -	-20/70, -30/80, -	30/85, -40/85	°C	
	Frequen	icy Stability				
Stability Over T _{OP} ⁴ , Ordering Option	F _{STAB}	±0.05, ±0	0.10, ±0.20, ±0.2	28, ±0.50	ppm	
Frequency Tolerance ⁵	F _{TOL}			±2.0	ppm	
Power Supply Stability, ±5%	F _{PWR}			±0.1	ppm	
Load Stability, ±10%	F _{LOAD}			±0.05	ppm	
Aging / 1st year	F _{AGE}			±1.0	ppm	
Fi	requency Tuning	(EFC), Ordering O	ption	•		
Tuning Range ⁶	PR	±5.0	±5.0, ±8.0, ±10.0, ±12.0			
Tuning Slope			Positive			
Control Voltage to reach Pull Range	V _c	0.5	1.5	2.5	V	
Control Voltage Impedance		100			Kohm	
RF O	utput (Clipped Sir	ne Wave), Orderin	g Option			
Output Level High	V _o p-p	0.8			V	
Output Load	C		10k 10pF			
Start Up Time	t _{su}			2	ms	
	Phas	e Noise ⁷				
Phase Noise, 10.00MHz ⁷	Ø _N				dBc/Hz	
10Hz			-99			
100Hz 1kHz			-126 -145			
10kHz			-145			
100kHz			-155			

1. Refer to Table 8 for Standard Frequencies. Other Frequencies are available on request. Check with factory.

2. Output DC-cut capacitor is optional.

3. The VT-706 power supply pin (Pin4) should be filtered using a by-pass capacitor of 0.1uF for optimal performance.

4. Referenced to the midpoint between minimum and maximum frequency value over Operating Temperature Range.

5. Frequency measured at 25 °C, 1 hour after 2 IR reflows.

6. Referenced to Mid Control Voltage

7. Measured at ambient temperature using Agilent E5052B Signal Source Analyzer.

Symbol	Min.	Тур	Max	Units
f _o	5		52	MHz
V _{DD}	+2	.8, +3.0, +3.3, +	5.0	V
I _{DD}			6.0	mA
T _{OP}	0/55, -10/70, -	20/70, -30/80, -	30/85, -40/85	°C
Frequen	cy Stability			
F _{stab}	±0.05, ±0	0.10, ±0.20, ±0.2	28, ±0.50	ppm
F _{TOL}			±2.0	ppm
F _{PWR}			±0.1	ppm
F _{LOAD}			±0.05	ppm
F _{AGE}			±1.0	ppm
requency Tuning	(EFC), Ordering Op	otion		
PR	±5.0, ±8.0, ±10.0, ±12.0			ppm
		Positive		
V _c	0.5	1.5	2.5	V
	100			Kohm
RF Output (CMC	S), Ordering Optic	on		
V _{OH} V _{OI}	0.9*V _{DD}		0.1*V _{pp}	V
1			15	pF
	45		55	%
t _{su}			2	ms
			4	ns
Phase	e Noise ⁷			
0,		-102 -128 -147 -154		dBc/Hz
	$\begin{tabular}{ c c c } \hline V_{DD} \\ \hline I_{DD} \\ \hline I_{DD} \\ \hline T_{OP} \\ \hline Frequen \\ \hline F_{STAB} \\ \hline F_{TOL} \\ \hline F_{TOL} \\ \hline F_{DU} \\ \hline F_{LOAD} \\ \hline F_{AGE} \\ \hline \hline requency Tuning \\ \hline PR \\ \hline \hline V_{C} \\ \hline \hline \hline RF Output (CMC \\ \hline V_{OH} \\ \hline V_{OL} \\ \hline C_{L} \\ \hline \hline \\ \hline E_{SU} \\ \hline \hline \\ \hline \\ Phase \\ \hline \end{tabular}$	V_{DD} +2 I_{DD} T_{OP} 0/55, -10/70, - Frequency Stability F_{TOL} F_{TOL} F_{TOL} F_{LOAD} F_{AGE} $requency Tuning (EFC), Ordering Option V_{C} 0.5 V_{C} 0.5 V_{OH} 0.9*V_{DD} V_{OL} C_{L} 45 t_{SU} Phase Noise7 $	V_{DD} $+2.8, +3.0, +3.3, +.$ I_{DD} T_{OP} T_{OP} $0/55, -10/70, -20/70, -30/80,$ Frequency Stability F_{sTAB} $\pm 0.05, \pm 0.10, \pm 0.20, \pm 0.2$ F_{TOL} I F_{TOL} I F_{LOAD} I F_{AGE} I $requency Tuning$ (EFC), Ordering Option PR $\pm 5.0, \pm 8.0, \pm 10.0, \pm$ V_{C} 0.5 V_{C} 0.5 V_{C} 0.5 V_{C} 0.5 V_{C} 0.5 V_{C} 0.5 V_{OL} $0.9*V_{DD}$ V_{OL} V_{OL} C_{L} I V_{OH} $0.9*V_{DD}$ V_{OL} I V_{OL} I V_{OL} I V_{OL} I V_{OL} I	$\begin{tabular}{ c c c c c } \hline V_{DD} & +2.8, +3.0, +3.3, +5.0 \\ \hline I_{DD} & 6.0 \\ \hline T_{OP} & 0/55, -10/70, -20/70, -30/80, -30/85, -40/85 \\ \hline Frequency Stability & \\ \hline F_{STAB} & \pm 0.05, \pm 0.10, \pm 0.20, \pm 0.28, \pm 0.50 \\ \hline F_{TOL} & \pm 2.0 \\ \hline F_{TOL} & \pm 2.0 \\ \hline F_{PWR} & \pm 0.1 \\ \hline F_{LOAD} & \pm 0.1 \\ \hline F_{LOAD} & \pm 0.05 \\ \hline F_{AGE} & & \pm 1.0 \\ \hline requency Tuning (EFC), Ordering Option & \\ \hline PR & \pm 5.0, \pm 8.0, \pm 10.0, \pm 12.0 \\ \hline PR & \pm 5.0, \pm 8.0, \pm 10.0, \pm 12.0 \\ \hline PR & \pm 5.0, \pm 8.0, \pm 10.0, \pm 12.0 \\ \hline V_{C} & 0.5 & 1.5 & 2.5 \\ \hline 100 & & \\ \hline RF Output (CMOS), Ordering Option & \\ \hline V_{OL} & 0.9^{*V} DD & 0.1^{*V} DD \\ \hline C_{L} & 15 & \\ \hline C_{L} & 15 & 55 \\ \hline t_{SU} & 0.9^{*V} DD & 2 \\ \hline Phase Noise^7 & \\ \hline 0_{N} & -102 \\ -128 \\ -147 \\ -154 \\ \hline \end{tabular}$

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4. Referenced to the midpoint between minimum and maximum frequency value over Operating Temperature Range.

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6. Referenced to Mid Control Voltage.

7. Measured at ambient temperature using Agilent E5052B Signal Source Analyzer

Phase Noise Performance for 10MHz CMOS



Package Outline Drawing & Pad Layout



[SIDE VIEW]





Dimensions in mm



Table 3.	Table 3. Pinout						
Pin #	Symbol	Function					
1	Vc or NC TCXO Control Voltage or No Conne						
2	GND	Ground					
3	OUT RF Output						
4	V _{DD}	Supply Voltage					

Note:

0.1uF capacitor is a by-pass power supply filter capacitor placed between Pin4 (Vdd) and Ground for optimal performance.

Marking Information XXMXX - Frequency (Example: 10M000) YY - Year of Manufacture WW - Week of the Year T - Manufacturing Location

- Pin 1 Indicator

Maximum Ratings

Absolute Maximum Ratings and Handling Precautions

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Although ESD protection circuitry has been designed into the VT-706, proper precautions should be taken when handling and mounting, VI employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation.

ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Table 4. Maximum Ratings			
Parameter	Symbol	Rating	Unit
Storage Temperature	T _{store}	-55/125	۰C
Supply Voltage	V _{DD}	-0.6/6	V
Control Voltage	V _c	-0.6/V _{DD} +0.6	V
Enable/Disable Voltage	E/D	-0.6/V _{DD} +0.6	V
ESD, Human Body Model		1500	V
ESD, Charged Device Model		1000	V

Reliability

Table 5. Environmental Compliance					
Parameter	Condition				
Mechanical Shock	MIL-STD-883 Method 2002				
Mechanical Vibration	MIL-STD-883 Method 2007				
Temperature Cycle	MIL-STD-883 Method 1010				
Solderability	MIL-STD-883 Method 2003				
Fine and Gross Leak	MIL-STD-883 Method 1014				
Resistance to Solvents	MIL-STD-883 Method 2015				
Moisture Sensitivity Level	MSL1				
Contact Pads	Gold over Nickel				

IR Reflow

Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 6. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220°C.

Table 6. Reflow Profile		
Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	t _s	200 sec Max 150℃ 200℃
Ramp Up	R _{UP}	3°C/sec Max
Time above 217C	t	150 sec Max
Time to Peak Temperature	t _{25C to peak}	480 sec Max
Time at 260C	t _p	30 sec Max
Time at 240C	t _{P2}	60 sec Max
Ramp down	R _{DN}	6°C/sec Max

Solderprofile:



VCXO Function

VCXO Feature: The VT-706 is supplied with a VCXO function for applications were it will be used in a PLL, or the output frequency needs fine tune or calibration adjustments. This is a high impedance input, 100kOhm, and can be driven with an op-amp or terminated with adjustable resistors etc. **Pin1 should not be left floating on the VCXO optional device.**

Tape & Reel

Table 7. Tape and Reel Information												
	Tape Dimensions (mm)Reel Dimensions (mm)											
W	F	Do	Ро	P1	А	В	С	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	1.5	13	20.2	60	16.4	20.4	1000



Ordering Information



Example: VT-706-EFW-207A-19M2000000

* Add **_SNPBDIP** for tin lead solder dip Example: VT-706-EFW-207A-19M2000000_SNPBDIP

Standard Frequencies & Capability Chart

Table 8. Sta	Table 8. Standard Frequencies (MHz)								
10.000	12.800	16.384	19.200	19.440	20.000	25.000	26.000	40.000	50.000

Note: Other Frequencies are available on request.

Table 9. Cap	Table 9. Capability Chart [Clipped Sine & CMOS Output]						
	±0.05ppm	±0.10ppm	±0.20ppm	±0.28ppm	±0.50ppm		
0/55°C							
-10/70°C	•						
-20/70°C	•			•			
-30/85°C	•	•		•			
-40/85°C	•	•		•			

E = Can be provided.

- Under development. Please consult with factory.
- = Cannot be provided.

Revision History

Revision Date	Approved	Description
Sept 10, 2015	VN	Rev 0.0: VT-706 Preliminary Datasheet - Internal Verification (Factory Approval)
Sept 17, 2015	VN	Rev 0.1: VT-706 Preliminary Datasheet for Product Launch.
Sept 19, 2016	VN	Rev 0.2: Removed "Preliminary" from datasheet
Aug 10, 2018	FB	Rev 0.3: Updated logo and contact information, added "SNPBDIP" ordering option



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