250 MHz Dual DCL

ADATE205

FEATURES

Driver, comparator, and active load
250 MHz toggle rate
Inhibit mode function
Dynamic clamps
Operating voltage range: −1.5 V to +6.5 V
Output voltage swing: 200 mV to 8 V
Four range adjustable slew rate
True/complement data mode bit
100-lead thin quad flat package, exposed pad
Low per channel power
- **1.15 W with load off**
- **1.50 W with load programmed at 20 mA nominal**

Low leakage (<10 nA) in High-Z mode
Driver
- **50 Ω output resistance**
- **1.6 ns minimum pulse width for a 3 V step**

Load: −35 mA to +35 mA maximum current range

APPLICATIONS

Automatic test equipment
Semiconductor test systems
Board test systems
Instrumentation and characterization equipment

GENERAL DESCRIPTION

The ADATE205 is a complete, single-chip solution that performs the pin electronics functions of driver, comparator, and active load (DCL) for ATE applications. The active load can be powered down if not used.

The driver is a proprietary design that features three active modes: data high mode, data low mode, and term mode, as well as an inhibit state.

The driver has low leakage (<10 nA) in High-Z mode. The output voltage range is −1.5 V to +6.5 V to accommodate a wide variety of test devices.

The ADATE205 supports four programmable Tr/Tf times for applications where slower edge rates are required. The edge rate selection is done via two static digital CMOS select bits. The input data to the driver can be inverted using a single CMOS logic bit. This feature can be used for system calibration or applications where complement input data is needed.

FUNCTIONAL BLOCK DIAGRAM

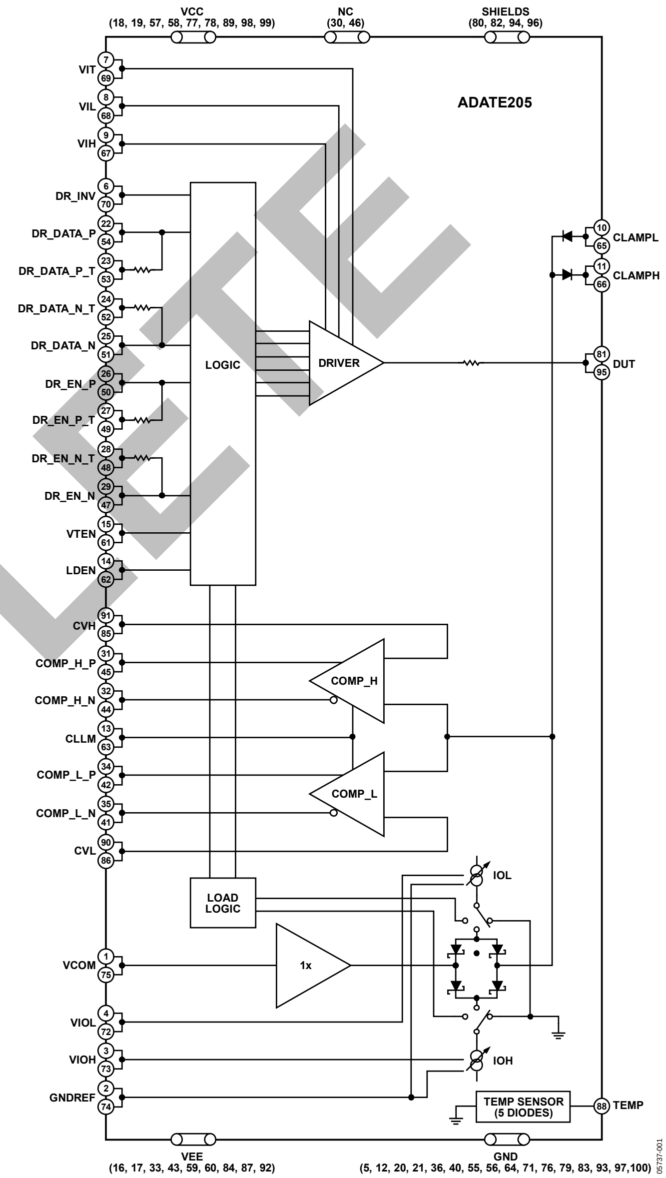

Figure 1.

Rev. A

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REVISION HISTORY

10/08—Rev. 0 to Rev. A
Changes to VCOM Buffer Offset Parameter, Table 1 ... 7

1/06—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CC} = 10 V, V_{EE} = −5 V, T_J = 75°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Single-Ended Logic Input Characteristics (VTEN, DRV_INV)					
Threshold Voltage		CMOS_VDD/2		V	
Voltage Range	0		5.5	V	
Bias Current	−10		+10	μA	V_{IN} = 0 V, 3.3 V
Single-Ended Logic Input Characteristics (SLEW0, SLEW1)					
Threshold Voltage		CMOS_VDD/2		V	
Voltage Range	0		5.5	V	
Bias Current	−10	+600 (@ 3.3 V)	+800	μA	V_{IN} = 0 V, 3.3 V
Bias Current		1		mA	V_{IN} = 5.5 V
Differential Logic Input Characteristics (DR_DATA_N, DR_DATA_P, DR_EN_N, DR_EN_P)					
Voltage Range	−2.0		+3.5	V	
Differential Voltage with LVPECL Levels	±250	±300		mV	
Bias Current	−10	+2	+10	μA	V_{IN} = 3.24 V, 3.495 V
VIH, VIL Reference Inputs					
Input Bias Current	−10	−2	+10	μA	Maximum value bias of reference sweep
VIT Reference Inputs					
Input Bias Current	−25	+12	+25	μA	Maximum value bias of reference sweep
DC Output Characteristics					
Logic Range, VIL, VIH, VIT	−1.5		+6.5	V	
Amplitude [VH to VL]			8	V	
Output Resistance	47.5		52.5	Ω	
PSRR, Drive or Term Mode		10		mV/V	V_{CC}, V_{EE} ±1%
Static Current Limit	−125	±110	+125	mA	Output to −1.5 V, VH = 6.5 V, VT = 0 V
Absolute Accuracy—VIH, VIL, VIT					
VIH Offset	−100	+30	+100	mV	Data = H, VH = 0 V, VL = −1.5 V, VT = 3 V
VIH Gain Error	0.98		1.02	V/V	Data = H, VH = 0 V to 5 V, VL = −1.5 V, VT = 3 V
VIH Linearity Error	−15	+5	+15	mV	Data = VH relative to line between 0 V to 5 V; full range of VIH = −1.4 V to +6.5 V
VIL Offset	−100	+30	+100	mV	
VIL Gain Error	0.98		1.02	V/V	Data = L, VL = 0 V to 5 V, VH = 6.5 V, VT = 3 V
VIL Linearity Error	−15	+5	+15	mV	Data = VH relative to line between 0 V to 5 V; full range of VIH = −1.4 V to +6.5 V
VIT Offset	−100	+30	+100	mV	Data = VT, VT = 0 V, VL = 0 V, VH = 3 V
VIT Gain Error	0.98		1.02	V/V	Data = VT, VT = 0 V to 5 V, VL = 0 V, VH = 3 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VIT Linearity Error	−15	+5	+15	mV	Data = VH relative to line between 0 V to 5 V; full range of VIH = −1.4 V to +6.5 V
Offset Tempco		80		μV/°C	65°C to 105°C
Driver Interaction					
VH Interaction to VL	−2		+2	mV	VIH = 5.0 V; VIL = −1.5 V, +4.7 V, +4.8 V, +4.9 V
VH Interaction to VT	−2		+2	mV	VIH = 3.0 V; VIT = −1.5 V, +2.9 V, +3.1 V, +6.5 V
VL Interaction to VH	−2		+2	mV	VIL = 0.0 V; VIH = 0.1 V, 0.2 V, 0.3 V, 6.5 V
VL Interaction to VT	−2		+2	mV	VIL = 0.0 V; VIT = −1.5 V, −0.1 V, +0.1 V, +6.5 V
VT Interaction to VH	−2		+2	mV	VIT = 1.5 V, VIL = −1.0 V; VIH = −0.8 V, +1.4 V, +1.6 V, +6.5 V
VT Interaction to VL	−2		+2	mV	VIT = 1.5 V, VIH = 6.0 V; IL = −1.5 V, +1.4 V, +1.6 V, +5.8 V
Rise/Fall Times at Device Under Testing (DUT)					
0.2 V Swing: Rise/Fall Time		300		ps	Terminated 20% to 80%, VIH = 400 mV, VIL = 0 V, VIT = 0 V
0.5 V Swing: Rise/Fall Time		500		ps	Terminated 10% to 90%, VIH = 1.0 V, VIL = 0 V, VIT = 0 V
1 V Swing: Rise/Fall Time		800		ps	Terminated 10% to 90%, VIH = 2.0 V, VIL = 0 V, VIT = 0 V
3 V Swing: Rise/Fall Time		1.1		ns	Unterminated 10% to 90%, VIH = 3.0 V, VIL = 0 V, VIT = 0 V
3 V Swing: Rise/Fall Time	700	800	920	ps	Terminated 20% to 80%, VIH = 3.0 V, VIL = 0 V, VIT = 0 V using DUT comparator
5 V Swing: Rise/Fall Time		1.8		ns	Unterminated 10% to 90%; VIH = 5.0 V, VIL = 0 V, VIT = 0 V
Minimum Pulse Width at DUT					
500 mV Swing[1]		500		ps	Terminated, VIH = 1.0 V, VIL = 0 V, VIT = 0 V
1.5 V Swing[1]		800		ps	Terminated, VIH = 3.0 V, VIL = 0 V, VIT = 0 V
Toggle Rate @ 3 V		250		MHz	Unterminated, 50/50 dc measured frequency when amplitude drops 10%
Dynamic Performance, Drive (VH and VL)					
Propagation Delay Time[2]		1.4		ns	Terminated, VIH = 3.0 V, VIL = 0.0 V, VIT = 0.0 V
Propagation Delay Tempco[2]		2.0		ps/°C	Terminated, VIH = 3.0 V, VIL = 0.0 V, VIT = 0.0 V, 65°C to 85°C
Delay Matching, Edge-to-Edge		20		ps	
Delay Change vs. Pulse Width[2]		30		ps	Terminated, VIH = 3.0 V, VIL = 0.0 V, VIT = 0.0 V, 1μs period, pulse width = 50 ns to 1 ns
Delay Change vs. Duty Cycle[2]		5		ps	Terminated, VIH = 3.0 V, VIL = 0.0 V, VIT = 0.0 V, 1 μs period; 10%, 50%, and 90% duty cycle

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Settling Time to 15 mV		8		ns	Terminated, VIH = 3 V, VIL = 0.0 V, VIT = 0.0 V
Settling Time to 4 mV		32		ns	Terminated, VIH = 3 V, VIL = 0.0 V, VIT = 0.0 V
Rise and Fall Time Temperature Coefficient					
500 mV Swing		2		ps/°C	Terminated 10% to 90%, VIH = 1.0 V, VIL = 0.0 V, VIT = 0.0 V, 65°C to 85°C
1 V Swing		2		ps/°C	Terminated 10% to 90%, VIH = 2.0 V, VIL = 0.0 V, VIT = 0.0 V, 65°C to 85°C
3 V Swing		2		ps/°C	Unterminated 10% to 90%, VIH = 3.0 V, VIL = 0.0 V, VIT = 0.0 V, 65°C to 85°C
5 V Swing		2		ps/°C	Unterminated 10% to 90%, VIH = 5.0 V, VIL = 0.0 V, VIT = 0.0 V, 65°C to 85°C
Overshoot and Preshoot 200 mV swing		1		%	Terminated, VIH = 400 mV
Overshoot and Preshoot 1 V swing		1		%	Terminated, VIH = 2 V
Overshoot and Preshoot 3 V swing		2		%	Unterminated
Overshoot and Preshoot 5 V swing		2		%	Unterminated
Dynamic Performance, Inhibit					
Delay Time, Active High to Inhibit[3]		3.1		ns	Terminated, VIH = 3.0 V, VIL = −1.0 V
Delay Time, Active Low to Inhibit[3]		2.1		ns	VH = 3.0 V, VL = −1.0 V, terminated 50 Ω
Delay Time, Inhibit to Active High[3]		2.5		ns	Terminated, VIH = 3.0 V, VIL = −1.0 V
Delay Time, Inhibit to Active Low[3]		3.9		ns	Terminated, VIH = 3.0 V, VIL = −1.0 V
I/O Spike		350		mV	Terminated, VIH = 0.0 V, VIL = 0.0 V, VIT = 0.0 V
CLAMPS					
VCPH, VCPL Clamp Inputs					
VCPH Voltage Range	CLAMPL		6.8	V	
VCPL Voltage Range	−1.8		CLAMPH	V	
Input Bias Current	−50	−2	+50	µA	Maximum value bias of reference sweep = −1.8 V to +6.8 V
Absolute Accuracy VCPH, VCPL					
VCPH Offset	−100	+55	+100	mV	Driver = INH, VCPH = 0 V
VCPH Gain Error		1		V/V	
VCPH Linearity Error		+10		mV	Driver = INH, relative to line between 0 V to 4.5 V, VCPH = −1.5 V to +6.5 V, VCPL = −1.8 V
VCPL Offset	−100	+55	+100	mV	Driver = INH, VCPL = 0 V
VCPL Gain Error		1		V/V	
VCPL Linearity Error		+10		mV	Driver = INH, relative to line between 0 V to 4.5 V, VCPL = −1.5 V to +6.5 V, VCPH = 6.5 V
COMPARATOR DC SPECIFICATIONS[4]					
DC Input Characteristics (VOH, VOL)					
Bias Current	−10	+5	+10	µA	VOH and VOL = −1.5 V to +6.5 V
Voltage Range	−1.5		+6.5	V	
Differential Voltage	−8.0		+8.0	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Offset	−15		+15	mV	Common mode = 0 V
Gain Error		1		% FSR	V_{IN} = −1.5 V to +6.5 V
Linearity Error		3		mV	V_{IN} = −1.5 V to +6.5 V
Single-Ended Logic Input Characteristics					
Threshold Voltage (CLLM)		CMOS_VDD/2		V	
Voltage Range	0		5.5	V	
Bias Current	−10	+160	+200	μA	V_{IN} = 0 V, 3.3 V
Bias Current		260		μA	V_{IN} = 5.5 V
Digital Output Characteristics (VOH, VOL Levels)					
Logic 1	3.1	3.26	3.4	V	Terminated 50 Ω to 3.3 V
Logic 0	2.7	2.86	3.1	V	Terminated 50 Ω to 3.3 V
Differential Levels	350	400	450	mV	Terminated 50 Ω to 3.3 V
COMPARATOR AC SPECIFICATIONS					
Propagation Delay					
Input to Output		500		ps	V_{IN} = 3 V p-p, 2 V/ns
Propagation Delay Tempco		1.0		ps/°C	V_{IN} = 3 V p-p, 2 V/ns
Propagation Delay Change with Respect to					
PD vs. Duty Cycle		40		ps	V_{IN} = 0 V to 3 V, 2 V/ns, driver in VTERM, VIT = 0 V, period = 10 ns; dc = 1 ns, 5 ns, 9 ns
Slew Rate: 1 V/ns, 2 V/ns, 3 V/ns		30		ps	V_{IN} = 0 V to 3 V, driver in VTERM, VIT = 0 V; slew rates = 1 V/ns, 2 V/ns, 3 V/ns
Amplitude: 500 mV, 1.0 V, 3.0 V		30		ps	V_{IN} = 0 V to 500 mV, 0 V to 1 V, 0 V to 3 V, 2 V/ns, driver in VTERM, VIT = 0 V
Equivalent Input Rise Time		225		ps	V_{IN} = 0 V to 1 V, <50 ps, 20% to 80% rise time, driver in VTERM = 0 V
Pulse-Width Linearity		20		ps	V_{IN} = 0 V to 3 V, 2 V/ns; pulse width = 3 ns, 4 ns, 5 ns, 10 ns; driver in VTERM, VIT = 0 V
Settling Time		5.5		ns	Settling to ±8 mV, V_{IN} = 0 V to 3 V, driver in VTERM, VIT = 0 V
Minimum Pulse Width		1		ns	2 V terminated, 1 V at the comparator, driver in VTERM, VIT = 0 V, 1 μs period, pulse width = 50 ns to 1 ns
Hysteresis		6		mV	V_{IN} = 100 mV, sweep CVL and CVH
Comparator Propagation Delay Matching, HCOMP to LCOMP		50		ps	HCOMP rise to LCOMP rise, HCOMP fall to LCOMP fall
LOAD DC SPECIFICATIONS					
Single-Ended Logic Input Characteristics					
Threshold Voltage (LDEN)		CMOS_VDD/2		V	
Voltage Range	0		5.5	V	
Bias Current	−10		+10	μA	V_{IN} = 0 V, 3.3 V
Input Characteristics					
VIOL Current Program Range	0.0		3.5	V	VDUT = −1.5 V, +6.5 V IOL = 0 mA to 35 mA
VIOH Current Program Range	0.0		3.5	V	VDUT = −1.5 V, +6.5 V, IOH = 0 mA to 35 mA
VIOH, VIOL Input Bias Current	−10		+10	μA	VIOL = 0 V, 3.5 V; VIOH = 0 V, 3.5 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VDUT Range	−1.5		+6.5	V	|VDUT − VCOM| > 1.0 V
VDUT Range	−1.5		+6.5	V	VDUT − VCOM > 1.0 V, IOH = 0 mA to 35 mA
VDUT Range	−1.5		+6.5	V	VCOM − VDUT > 1.0 V, IOL = 0 mA to 35 mA
Output characteristics					
Gain	9.5	10	10.5	mA/V	Slope of line between 5 mA and 30 mA
Load Offset, IOH, IOL_T	−200		+200	μA	IOH and IOL programmed at 20 mV (200 μA)
Load Nonlinearity, IOH, IOL_T	−50		+50	μA	Relative to a line from 5 mA to 30 mA; IOL, IOH from 200 μA to 35 mA
Output Current Tempco, IOH, IOL_T		±3		μA/C	Measured at IOH, IOL = 30 mA
VCOM Buffer (Through Bridge)					
VCOM Buffer Offset	−50	+3	+50	mV	IOL, IOH = 20 mA, VCOM = 0 V
VCOM Buffer Bias Current	−10	+1	+10	μA	VCOM = −1.5 V to +6.5 V
VCOM Buffer Gain	0.99	1	1.01	V/V	IOL, IOH = 20 mA, VCOM = −1.5 V to +6.5 V
VCOM Buffer Linearity Error	−10	+1	+10	mV	IOL, IOH = 20 mA, VCOM = −1.5 V to +6.5 V, relative to a line at 0 V and 5 V
Dynamic Performance					
Propagation Delay—I_{MAX} to INHIBIT		2.3		ns	VTT = 2 V, VCOM = 4 V/0 V, IOL = 20 mA, IOH = 20 mA
INHIBIT to I_{MAX}		2.3		ns	VTT = 2 V, VCOM = 4 V/0 V, IOL = 20 mA, IOH = 20 mA
TOTAL FUNCTION					
Output Leakage Current	−1.5	+0.28	+1.5	μA	Driver = INH, VDUT swept from −1.5 V to +6.5 V
Output Leakage Current, Low Leakage Mode	−200	+10	+200	nA	Driver = INH, VDUT swept from −1.5 V to +6.5 V
Output Capacitance		2		pF	
Power Supplies[5]					
Total Supply Range			15.5	V	
Positive Supply, V_{CC}	9.75	10.0	10.25	V	
Negative Supply, V_{EE}	−5.25	−5.0	−4.75	V	
Positive Supply Current, V_{CC}	160	180	205	mA	Load enabled at 20 mA, driver is set to VIL = 0 V
Negative Supply Current, V_{EE}	210	240	270	mA	Load enabled at 20 mA, driver is set to VIL = 0 V
Total Power Dissipation	2	3	4	W	Load enabled at 20 mA, driver is set to VIL = 0 V
Positive Supply Current Load Disabled, V_{CC}	115	135	170	mA	Load enabled at 0 mA, driver is set to VIL = 0 V
Negative Supply Current Load Disabled, V_{EE}	160	190	220	mA	Load enabled at 0 mA, driver is set to VIL = 0 V
Total Power Dissipation	1.3	2.3	2.8	W	Load enabled at 0 mA, driver is set to VIL = 0 V
Temperature Sensor Gain Factor		10		mV/°C	Five diodes in series

[1] 1 μs period, pulse width = 50 ns to 500 ps, pulse width measured when amplitude drops 10%.
[2] Measured at 50% of input amp to 50% of output amp.
[3] t_{PD} measured from the 50% of enable signal to 50% of output.
[4] The low leakage mode of the comparator, controlled by VLLM input, reduces the leakage due to the comparator input. The comparator operates in this mode, but its bandwidth is compromised and is not guaranteed.
[5] Under no circumstances should the input voltages exceed the supply voltages.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Current for V_{CC}	205 mA
Maximum Current for V_{EE}	270 mA
Positive Supply Voltage (V_{CC} to GND)	+10.5 V
Negative Supply Voltage (V_{EE} to GND)	−5.5 V
Operating Temperature (Junction)	+150°C
Storage Temperature Range	−65°C to +150°C
ESD (Human Body Model)	±1500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

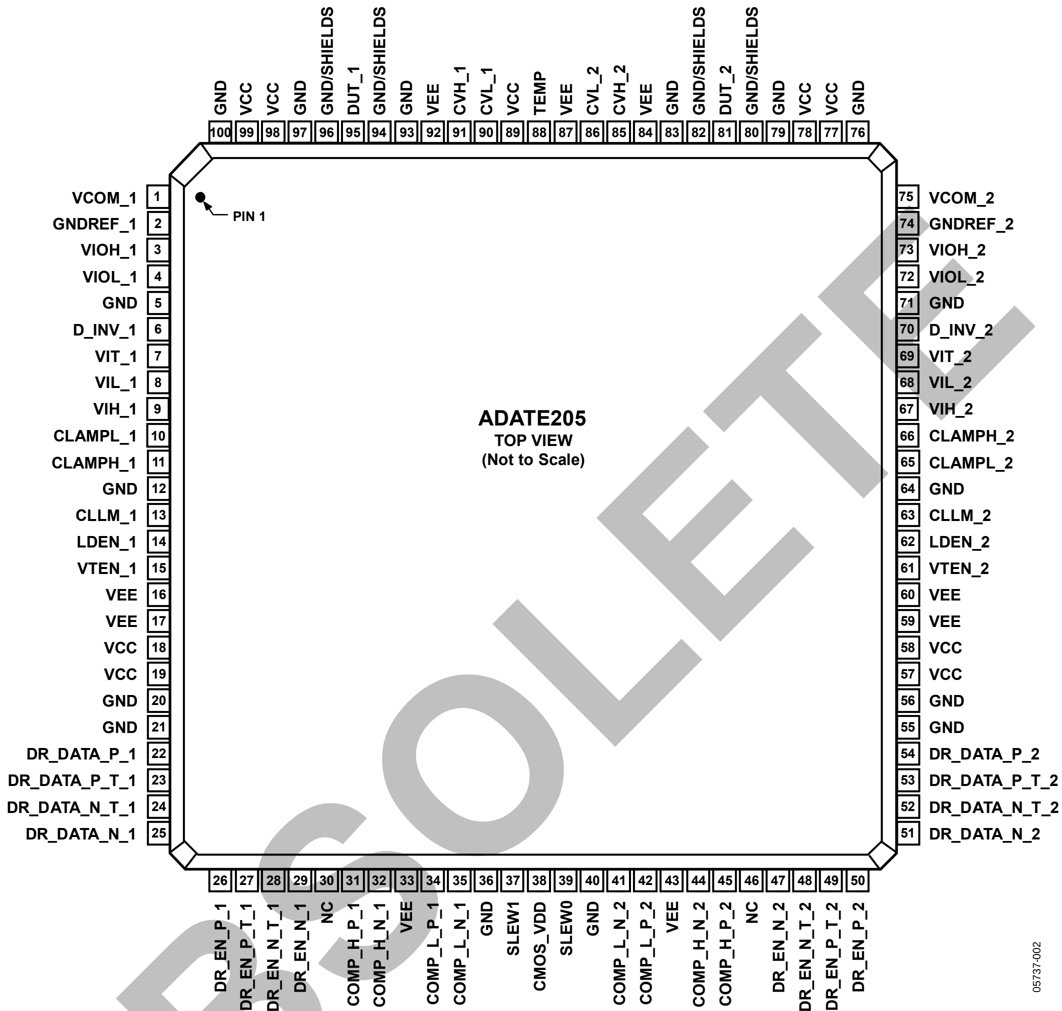

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCOM_1	Commutation Reference Voltage.
2	GNDREF_1	Reference GND for VIOL, VIOH.
3	VIOH_1	Program Voltage for IOH (Sink).
4	VIOL_1	Program Voltage for IOL (Source).
5, 12, 20, 21, 36, 40, 55, 56, 64, 71, 76, 79, 83, 93, 97, 100	GND	Device Ground.
6	D_INV_1	Driver Invert.
7	VIT_1	Driver Term Voltage Reference.
8	VIL_1	Driver Low Voltage Reference.
9	VIH_1	Driver High Voltage Reference.
10	CLAMPL_1	Low Clamp.
11	CLAMPH_1	High Clamp.
13	CLLM_1	Comparator Low Leakage Mode.
14	LDEN_1	Determines Whether LD Responds to DR_EN_1 or is Disabled (see Table 4).
15	VTEN_1	Low Speed Control Signal. When high, DR_EN_1 forces driver output to VIT. Otherwise, DR_EN_1 forces driver to High Impedance (see Table 4).
16, 17, 33, 43, 59, 60, 84, 87, 92	VEE	Negative Power Supply.
18 19, 57, 58, 77, 78, 89, 98, 99	VCC	Positive Power Supply.
22	DR_DATA_P_1	High Speed Data Inputs. Sets high/low state of driver output (see Table 4).
23	DR_DATA_P_T_1	Termination Resistors for HS Inputs. Opposite end of each 50 Ω termination resistor goes to the appropriate signal.
24	DR_DATA_N_T_1	Termination Resistors for HS Inputs. Opposite end of each 50 Ω termination resistor goes to the appropriate signal.
25	DR_DATA_N_1	Complement of DR_DATA_P_1.
26	DR_EN_P_1	High Speed Enable Inputs. Multifunction depending on status of VTEN_1 and LDEN_1. Causes driver to enter/leave inhibit; driver to enter/leave termination mode; load to leave/enter inhibit (see Table 4).
27	DR_EN_P_T_1	Termination Resistors for HS Inputs. Opposite end of each 50 Ω termination resistor goes to the appropriate signal.
28	DR_EN_N_T_1	Termination Resistors for HS Inputs. Opposite end of each 50 Ω termination resistor goes to the appropriate signal.
29	DR_EN_N_1	Complement of DR_EN_P_1.
30, 46	NC	No Connect.
31	COMP_H_P_1	High Comparator Outputs.
32	COMP_H_N_1	Complement of COMP_H_P_1.
34	COMP_L_P_1	Low Comparator Outputs.
35	COMP_L_N_1	Complement of COMP_L_P_1.
37, 39	SLEW1, SLEW0	Logic Signals Controlling Driver Slew Rates for Both Drivers. 00 codes for maximum slew voltage; 11 codes for minimum slew voltage.
38	CMOS_VDD	CMOS Supply (Internal ÷ 2 = Single-Ended Logic Reference).
41	COMP_L_N_2	Complement of COMP_L_P_1.
42	COMP_L_P_2	Low Comparator Outputs.
44	COMP_H_N_2	Complement of COMP_H_P_1.
45	COMP_H_P_2	High Comparator Outputs.

Pin No.	Mnemonic	Description
47	DR_EN_N_2	Complement of DR_EN_P_2.
48	DR_EN_N_T_2	Complement of DR_EN_N_T_2.
49	DR_EN_P_T_2	Termination Resistors for HS Inputs. Opposite end of each 50 Ω termination resistor goes to the appropriate signal.
50	DR_EN_P_2	High Speed Enable Inputs. Multifunction depending on status of VTEN_2 and LDEN_2. Causes driver to enter/leave inhibit; driver to enter/leave termination mode; load to leave/enter inhibit (see Table 4).
51	DR_DATA_N_2	Complement of DR_DATA_P_2.
52	DR_DATA_N_T_2	Complement of DR_DATA_P_T_2.
53	DR_DATA_P_T_2	Termination Resistors for HS Inputs. Opposite end of each 50 Ω termination resistor goes to the appropriate signal.
54	DR_DATA_P_2	High Speed Data Inputs. Sets high/low state of driver output (see Table 4).
61	VTEN_2	Low Speed Control Signal. When high, DR_EN_2 forces driver output to VT; otherwise, DR_EN_2 forces driver to high impedance (see Table 4).
62	LDEN_2	Determines Whether LD Responds to DR_EN_2 or is Disabled (see Table 4).
63	CLLM_2	Comp Low Leakage Mode.
65	CLAMPL_2	Low Clamp.
66	CLAMPH_2	High Clamp.
67	VIH_2	Driver High Voltage Reference.
68	VIL_2	Driver Low Voltage Reference.
69	VIT_2	Driver Term Voltage Reference.
70	D_INV_2	Driver Invert.
72	VIOL_2	Program Voltage for IOL (Source).
73	VIOH_2	Program Voltage for IOH (Sink).
74	GNDREF_2	Reference GND for VIOL, VIOH.
75	VCOM_2	Commutation Reference Voltage.
80, 82, 94, 96	GND/SHIELDS	Device Ground or Pin Shield.
81	DUT_2	Output/Input Pin.
85	CVH_2	Window High Reference Level.
86	CVL_2	Window Low Reference Level.
88	TEMP	Temperature Sense, Five Diode String, Reference to GND.
90	CVL_1	Window Low Reference Level.
91	CVH_1	Window High Reference Level.
95	DUT_1	Output/Input pin.

TYPICAL PERFORMACE CHARACTERISTICS

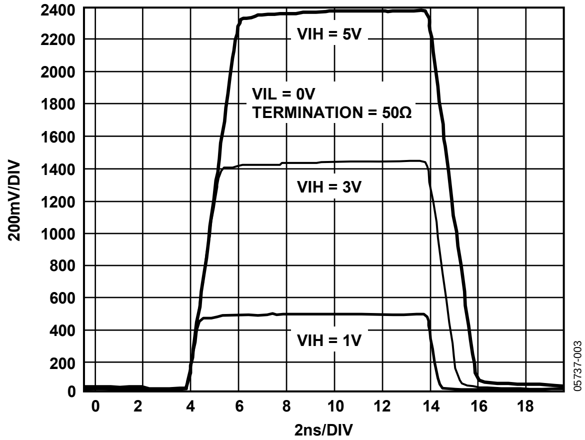

Figure 3. Driver Large Signal Response

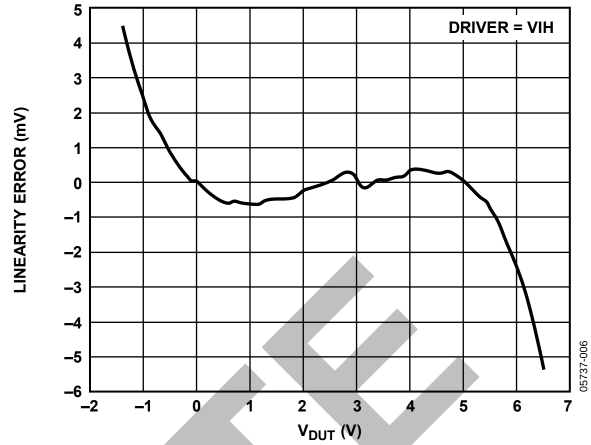

Figure 6. Driver VIH Linearity vs. Output

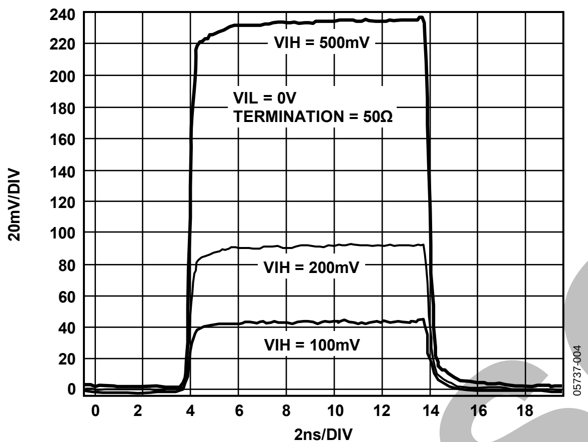

Figure 4. Driver Small Signal Response

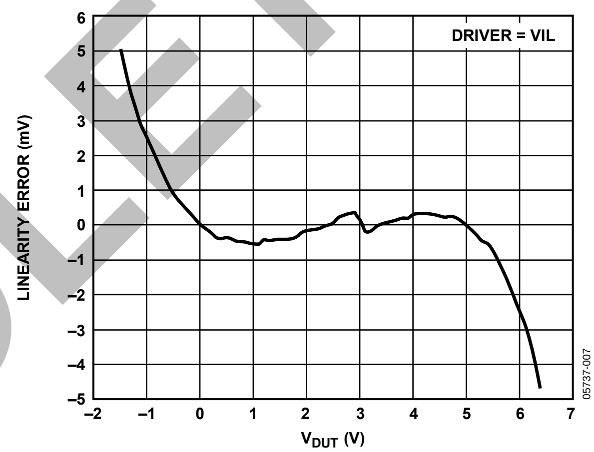

Figure 7. Driver VIL Linearity vs. Output

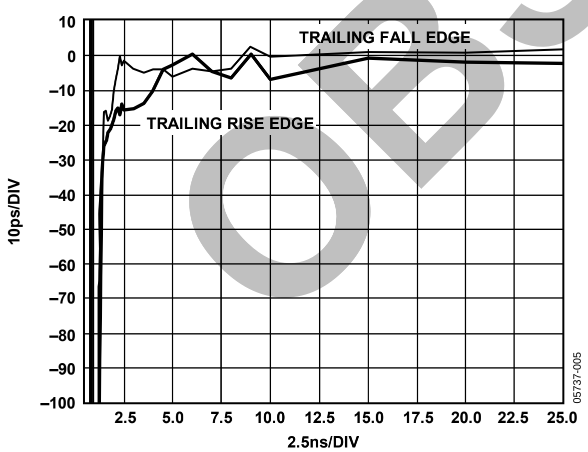

Figure 5. Driver Trailing Edge Timing Error vs. Pulse Width

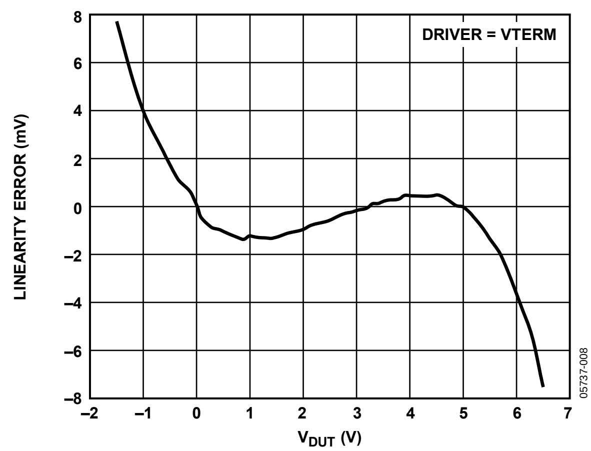

Figure 8. Driver VTERM Linearity vs. Output

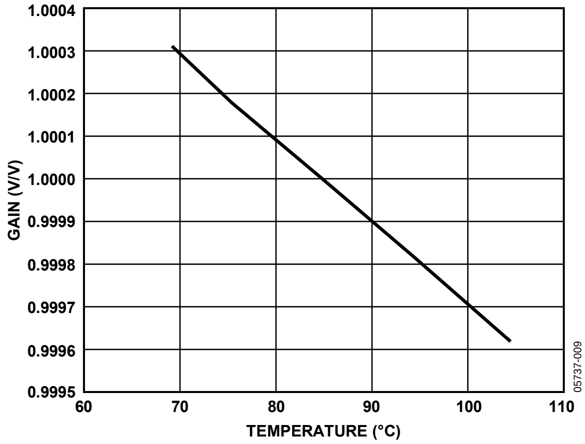

Figure 9. Driver Gain vs. Temperature

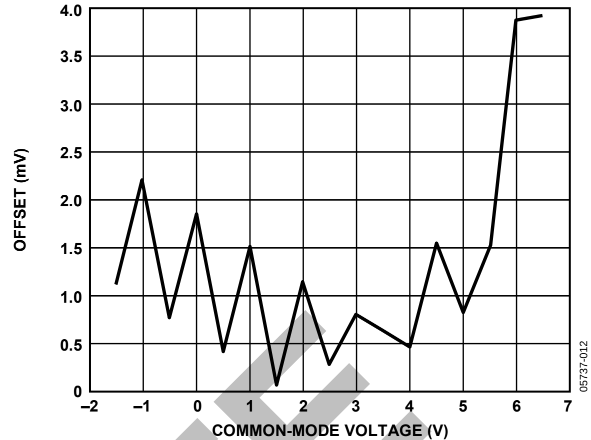

Figure 12. Comparator Offset vs. Common-Mode Voltage

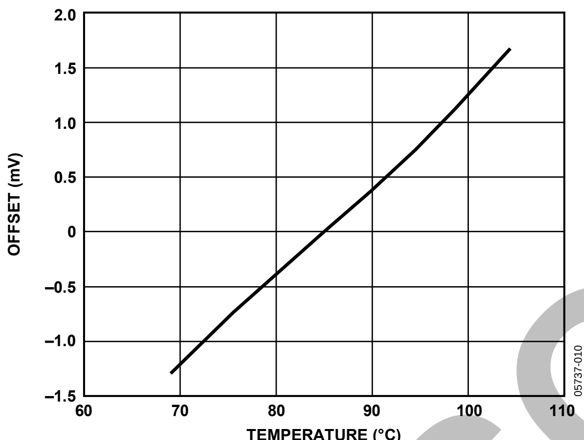

Figure 10. Driver Offset vs. Temperature

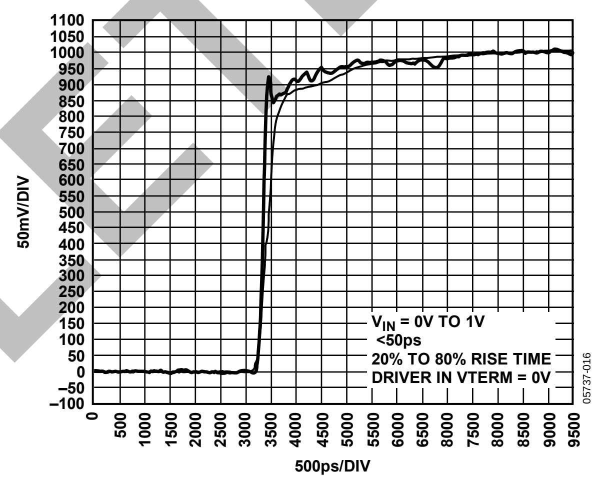

Figure 13. Comparator Schmoo at 1 ns Rise and Fall Time

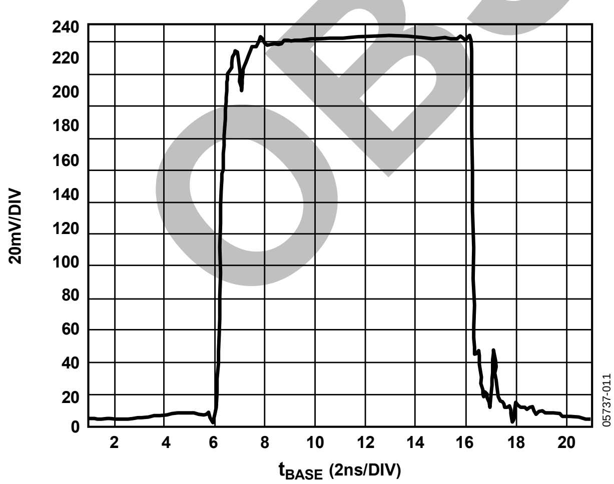

Figure 11. Comparator Differential Output Response

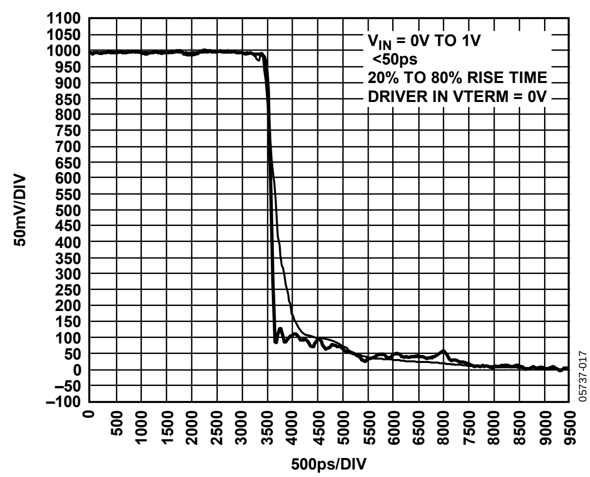

Figure 14. Comparator Schmoo at 600 ps Rise and Fall Time

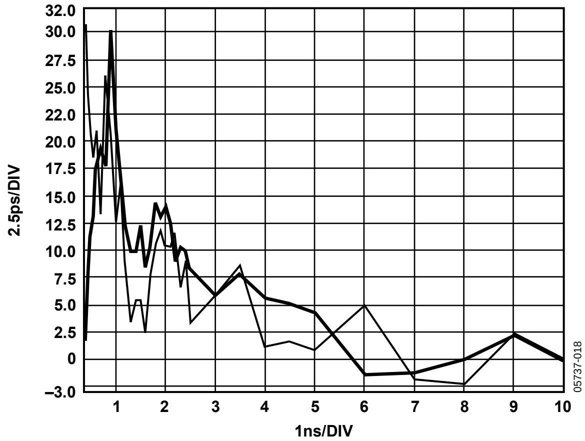

Figure 15. Comparator t_{PD} vs. Pulse Width

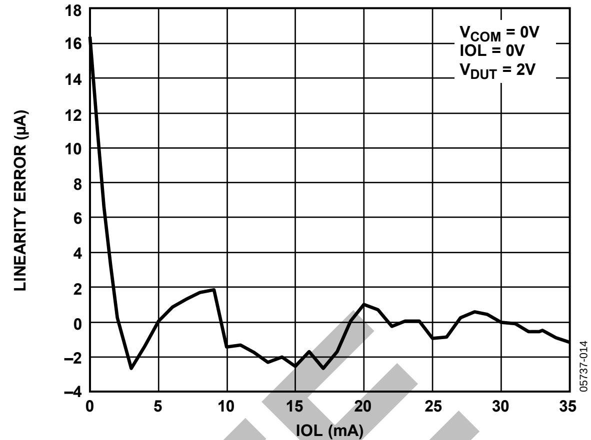

Figure 17. Active Load Linearity vs. IOH

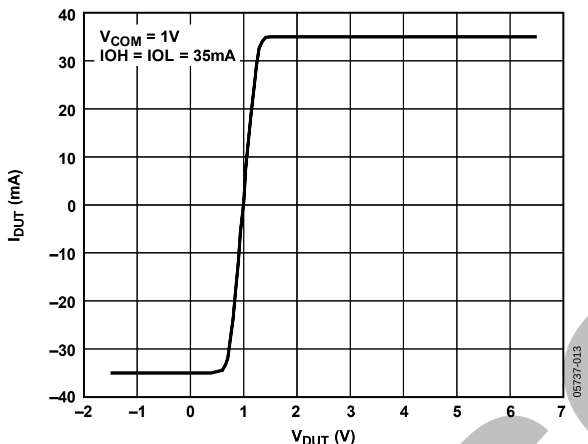

Figure 16. Active Load Commutation Region

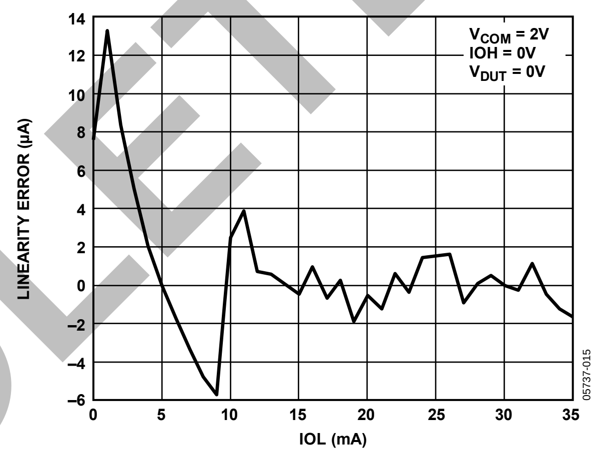

Figure 18. Active Load Linearity vs. IOL

THEORY OF OPERATION

The ADATE205 has two general classes of logic inputs: differential inputs for controlling functions that generally need to be operated at high speed, and single-ended CMOS inputs for setting operating modes or other low speed functions. The differential inputs have a wide common-mode range that allows them to be used with a variety of logic families. The differential inputs can also be used single-ended, with one input from each pair of inputs tied to a fixed reference, but this makes precise timing more difficult to achieve.

These differential input pins provide 50 Ω input termination resistors for use as desired. The single-ended inputs have an input range compatible with most logic families and are high impedance to make driving them very easy. The switching threshold for the single-ended inputs is preset to one-half of the voltage at the CMOS_VDD pin.

Table 4. Driver and Load Modes

LDEN (CMOS Single-Ended)	VTEN (CMOS Single-Ended)	DR_EN (High Speed Differential)	DR_DATA (High Speed Differential)	Driver Status	Load Status
0	0	0	X	High-Z	High-Z
0	0	1	0	VIL	High-Z
0	0	1	1	VIH	High-Z
0	1	0	X	VIT	High-Z
0	1	1	0	VIL	High-Z
0	1	1	1	VIH	High-Z
1	0	0	X	High-Z	ON
1	0	1	0	VIL	High-Z
1	0	1	1	VIH	High-Z

Table 5. Comparator Low Leakage Mode

CLLM (CMOS Single-Ended)	Typical DUT Pin Bias Current
0	1 µA
1	10 nA

Table 6. Rise/Fall Time Selection 3 V, 10% to 90%, Unterminated

Slew 1	Slew 0	Tr/Tf (ns)
0	0	1.4
0	1	1.9
1	0	2.8
1	1	5.6

Table 7. Comparator Logic Function

DUT Pin Voltage		Output States			
		COMP_L_P	COMP_L_N	COMP_H_P	COMP_H_N
>CVL	>CVH	1	0	1	0
>CVL	<CVH	1	0	0	1
<CVL	>CVH	0	1	1	0
<CVL	<CVH	0	1	0	1

OUTLINE DIMENSIONS

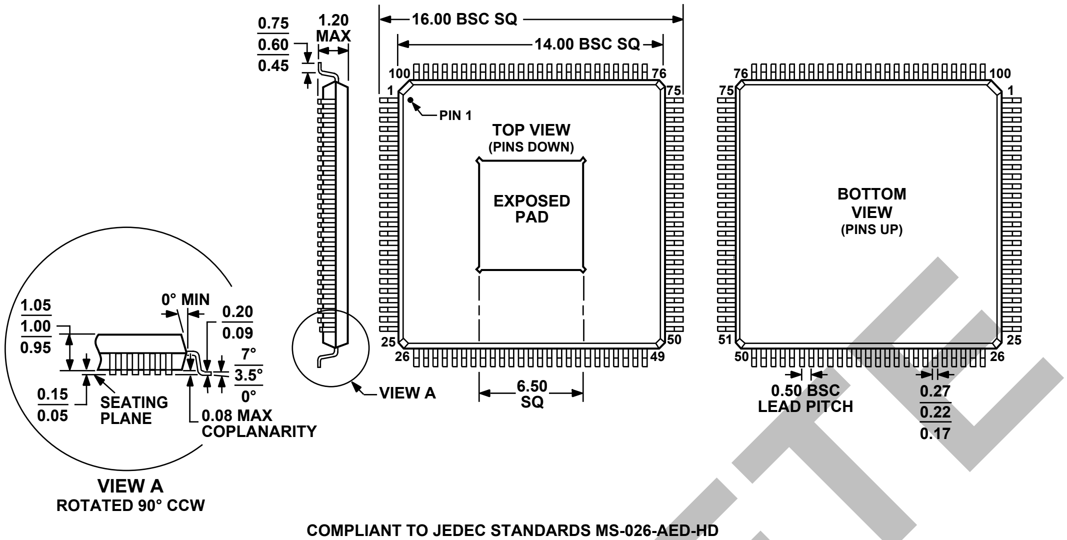

Figure 19. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADATE205BSV	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-2

D05737-0-10/08(A)