System Power Supply LSIs for use in automotive Electronics

# Multifunction System Power Supply IC (with Watchdog Timer)

## BD4911FM

ESD Resistance 4kV Now available

Pb Free ROHM Electronic Components

RoHS Directive Compliance

### ●Description

The BD4911FM multiple-output system power supply features microcontroller output and is capable of operating at super-low dark current levels. With a built-in reset, with a microcontroller delay, BATTERY/ACCESSORY voltage detection, and mute function, WDT (Watch Dog Timer)function, the BD4911FM is ideal for car audio and satellite navigation systems.

### ●Features

1) Main regulator Vo1 can be switched between 5.0 V and 3.3 V output using the SEL input voltage, and can be used with an external boost transistor.
   Sub-regulator Vo2 generates 3.3 V output.
   Both regulators feature an output current of 150 mA.
2) Built-in WDT reset; monitor time can be set with the CTW capacitor.
   WDT operation can be switched on and off using INH input.
3) Circuit current during standby operation (WDT off): 100 μA (TYP)
4) Built-in reduced power detection circuits for Vo1 and Vo2 output
5) Built-in elevated output detection circuit for Vo1
6) The IC monitors the BuM voltage and outputs it to the BuDET1 and BuDET2 pins.
7) The IC monitors the ACCM voltage and outputs it to the ACCM pin when BuDET1 and BuDET2 are low.
8) Built-in mute circuit. Pulse width can be set with the CE capacitor.
9) Built-in power-on reset function for which RESET output can be set with the CTP capacitor.
10) Vo1 generates low-saturation voltage type PMOS output.
11) Built-in overcurrent protection circuit
12) Built-in overvoltage protection circuit
13) Built-in thermal shutdown circuit
14) The 28-pin HSOP-M28 package is ideal for space-saving designs.

### ●Applications

Car audio and satellite navigation systems

Ver.B Oct.2005

●**Absolute Maximum Ratings** (Ta = 25°C)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply Voltage 1 | VIN1 | -0.3 to 36 | V |
| Supply Voltage 2 | VIN2 | -0.3 to 36 | V |
| Power Dissipation | Pd | 2200 (*1) | mW |
| Operating Temperature Range | Topr | -40 to +85 | °C |
| Storage Temperature Range | Tstg | -55 to +150 | °C |
| Peak Supply Voltage 1 | VIN1 Peak | 50 (*2) | V |
| Peak Supply Voltage 2 | VIN2 Peak | 50 (*2) | V |
| Surge Applied Current 1 | IACC (S+) | +3 (*2) | mA |
| Surge Applied Current 2 | IACC (S-) | -12 (*3) | mA |
| Maximum Junction Temperature | Tjmax | 150 | °C |

*1: When mounted on a PCB (70 mm × 70 mm × 1.6 mm glass epoxy).

*2: tr ≥ 1 ms, Bias voltage/current is less than 200 ms or shorter

*3: tr ≥ 1 ms, Bias voltage/current 60 ms or shorter

●**Recommended operating ranges** (Ta = 25°C)

| Parameter | Symbol | Limits | | | Unit | Comment |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Recommended Power Supply Voltage Range 1 | VIN1 | Vo1+1.2 | 13.2 | 16.0 | V | When using built-in transistor. |
| | VIN1 | Vo1 + 0.5 + eternal TrVBE | 13.2 | 16.0 | V | When using external boost transistor. |
| Recommended Power Supply Voltage Range 2 | VIN2 | 4.5 | 13.2 | 16.0 | V | |
| Recommended Power Supply Voltage Range 3 | Vo1 | 1.2 | — | 5.2 | V | RESET, DET1 |
| Recommended Power Supply Voltage Range 4 | Vo1 | 2.5 | — | 5.2 | V | BuDET, ACCDET, MUTE, WDT |
| Recommended Power Supply Voltage Range 5 | Vo2 | 1.2 | — | 3.4 | V | DET2 |

*Electrical characteristics are not guaranteed (especially when operating on reduced voltage).

●**External element setting time** (Ta = 25°C)

| Parameter | Symbol | Equation (TYP) | Unit | Recommendation | Unit | Condition |
|---|---|---|---|---|---|---|
| Runaway Operation Detection Time 1 | TWD1 | 700 × CTW (µF) | mS | 0.1 to 2.2 | µF | SEL > 1.5 V |
| Runaway Operation Detection Time 2 | TWD2 | 462 × CTW (µF) | mS | 0.1 to 2.2 | µF | SEL < 1.0 V |
| Runaway Operation Reset Time 1 | TWR1 | 340 × CTW (µF) | mS | 0.1 to 2.2 | µF | SEL > 1.5 V |
| Runaway Operation Reset Time 2 | TWR2 | 260 × CTW (µF) | mS | 0.1 to 2.2 | µF | SEL < 1.0 V |
| Power-on Reset Time | TPR | 1000 × CTP (µF) | mS | 0.047 to 0.22 | µF | |
| CD Delay Time | Td | 100 × CD (µF) | mS | 0.047 to 0.22 | µF | |
| MUTE Pulse Width | Tm | 1 × CE (µF) | S | 0.1 to 2.2 | µF | |
| BuM Detection Voltage (rising) | VTHBu | 1.252 × (R1+R2)/R2 | V | R1: 0.5 to 2 | MΩ | |
| BuM Detection Voltage (falling) | VTLBu | 1.184 × (R1+R2)/R2 | V | R2: 0.1 to 0.5 | MΩ | |
| ACCM Detection Voltage (rising) | VTHACC | 1.252 × (R3 + R4)/R4 | V | R3: 50 to 200 | kΩ | |
| ACCM Detection Voltage (falling) | ATLACC | 1.184 × (R3+R4)/R4 | V | R4: 10 to 50 | kΩ | |

●**Electrical characteristics** (Unless otherwise specified, Ta = 25°C, VIN1 = VIN2 = 13.2 V)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| [Overall] | | | | | | |
| VIN1 Supply Current | IVIN1 | 65 | 95 | 125 | μA | ACC = 0 V, WDINH = H |
| VIN2 Supply Current | IVIN2 | 5 | 10 | 20 | μA | ACC = 0 V, WDINH = H |
| Total Supply Current | IVINA | 65 | 100 | 135 | μA | ACC = 0 V, WDINH = H |
| | IVINB | 65 | 130 | 195 | μA | ACC = 13.2 V |
| Overvoltage Detection Voltage | VOVP | 28 | 31 | 34 | V | All regulator output off |
| Overvoltage Detection Hysteresis Width | VOVPHY | 0.5 | 1 | 1.5 | V | All regulator output reset |
| [Main Regulator (REG1)] | | | | | | |
| VO1 Output Voltage 1 | VO1-1 | 4.8 | 5.0 | 5.2 | V | VIN1 = 6.2 V to 16 V, Io1 = 0 mA to 150 mA, SEL > 1.5 V |
| VO1 Line Regulation 1 | ΔVO1l-1 | — | 1 | 30 | mV | VIN1 = 6.2 V to 16 V, SEL > 1.5 V |
| VO1 Load Regulation 1 | ΔVO1L-1 | — | 7 | 50 | mV | Io1 = 0 mA to 150 mA, SEL > 1.5 V |
| VO1 Output Voltage 2 | VO1-2 | 3.168 | 3.3 | 3.432 | V | VIN1 = 4.5 to 16 V, Io1 = 0150 mA, SEL < 1.0 V |
| VO1 Line Regulation 2 | ΔVO1l-2 | — | 1 | 30 | mV | VIN1 = 4.5 V to 16 V, SEL < 1.0 V |
| VO1 Load Regulation 2 | ΔVO1L-2 | — | 7 | 30 | mV | Io1 = 0 mA to 150 mA, SEL < 1.0 V |
| Minimum VO1 Output | VO1-L | 2.5 | — | — | V | VIN1 = 3.0 V, Io1 = 0 mA |
| Short Protection Start Current | Io1max | 150 | 400 | 600 | mA | |
| Power Supply Ripple Rejection Ratio | RRVO1 | 45 | 55 | — | dB | fin = 120 Hz, -10 dBV, Io1 = 150 mA |
| VO1 Sink Current | IVO1in | 35 | 90 | 145 | μA | Vo1 = 5 V, VIN1 = ACC = OPEN, WDINH = SEL = 5 V |
| [External Boost Transistor Current-limiting Circuit (OCP)] | | | | | | |
| OCP Input Current | IOCP | 0 | 0.1 | 1.0 | μA | VOCP = VIN1 = 16 V |
| OCP Detection Voltage | VOCP1 | 360 | 400 | 440 | mV | Voltage differential with VIN1 |
| OCP Detection Voltage (During Output Ground Fault) | VOCP2 | 20 | 32 | 50 | mV | Vo1 = 0 V, voltage differential with VIN1 |
| [Elevated Output Detection Circuit (COMP)] | | | | | | |
| Elevated Output Detection Voltage 1 | VOVER1 | 5.30 | 5.49 | 5.68 | V | SEL > 1.5 V |
| Elevated Output Detection Voltage 2 | VOVER2 | 3.5 | 3.62 | 3.75 | V | SEL < 1.0 V |
| Elevated Output Detection Output | VCOMP | — | 0.1 | 0.4 | V | VO1 > 5.68 V, Io = 100 μA |
| Output Off Delay Time | TmVoff | — | — | 50 | μS | Vo1: 3.1→4.8 V (tr = 0.01 V/μS) VIN1 = 4.8 V, Ro = 1 kΩ |
| [Sub-regulator (REG2)] | | | | | | |
| VO2 Output Voltage | VO2 | 3.168 | 3.3 | 3.432 | V | VIN1 = VIN2 = 4.5 V to 16V, Io2 = 0 mA to 150 mA, |
| VO2 Line Regulation | ΔVO2l | — | 1 | 30 | mV | VIN1 = VIN2 = 4.5 V to 16V |
| VO2 Load Regulation | ΔVO2L | — | 7 | 30 | mV | Io2 = 0 mA to 150 mA |
| Minimum VO2 Output | VO2-L | 2.5 | — | — | — | VIN1 = VIN2 = 3.0 V, Io2 = 0 mA |
| Short Protection Start Current | Io2max | 150 | 400 | 600 | mA | |
| Power Supply Ripple Rejection Ratio | RRVO2 | 45 | 55 | – | dB | fin = 120 Hz, -10 dBV, Io2 = 150 mA |
| [Regulator Voltage Selection Circuit (SEL)] | | | | | | |
| SEL Threshold | VTHSEL | 1.20 | 1.25 | 1.30 | V | |
| SEL Input Current | ISEL | 1 | 2 | 4 | μA | VSEL = 5 V |
| [VO1 Reduced-voltage Detection Circuit (DET1)] | | | | | | |
| VO1 Detection Voltage 1 | VTLP1-1 | 4.00 | 4.15 | 4.30 | V | Vo1 falling, SEL > 1.5 V |
| Reset Voltage 1 | VTHP1-1 | 4.10 | 4.35 | 4.60 | V | Vo1 rising, SEL > 1.5 V |
| Hysteresis Width 1 | VHSP1-1 | 0.1 | 0.2 | 0.3 | V | SEL > 1.5 V |
| VO1 Detection Voltage 2 | VTLP1-2 | 2.85 | 2.95 | 3.05 | V | Vo1 falling, SEL < 1.0 V |
| Reset Voltage 2 | VTHP1-2 | 2.92 | 3.09 | 3.26 | V | Vo1 rising, SEL < 1.0 V |
| Hysteresis Width 2 | VHSP1-2 | 0.07 | 0.14 | 0.21 | V | SEL < 1.0 V |
| DET1 Output On Resistance | RDET1 | — | 270 | 600 | Ω | IDET1 = 1 mA |
| DET1 Output Saturation Voltage | VDET1L | — | 0.1 | 0.4 | V | IDET1 = 2 μA, Vo1 = 1.2 V |

⦿ This IC is not designed to be radiation-resistant.

●**Electrical characteristics** (Unless otherwise specified, Ta = 25°C, VIN1 = VIN2 = 13.2 V)

| Parameter | Symbol | Limits Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| [VO2 Reduced-voltage Detection Circuit (DET2)] | | | | | | |
| VO2 Detection Voltage | VTLP2 | 2.85 | 2.95 | 3.05 | V | Vo2 falling |
| Reset Voltage | VTHP2 | 2.92 | 3.09 | 3.26 | V | Vo2 rising |
| Hysteresis Width | VHSP2 | 0.07 | 0.14 | 0.21 | V | |
| DET2 Output On Resistance | RDET2 | — | 270 | 600 | Ω | IDET2 = 1 mA |
| DET2 Output Saturation Voltage | VDET2L | — | 0.1 | 0.4 | V | IDET2 = 2 μA, Vo1 = 1.2 V |
| [Power-on Reset Timer (CTP, RESET)] | | | | | | |
| CTP Charge Resistance 1 | RCTP1 | 0.6 | 0.9 | 1.2 | MΩ | When RESET is low (while charging). |
| CTP Charge Resistance2 | RCTP2 | 5.5 | 8.5 | 11.5 | kΩ | When RESET is high (after charging is complete). |
| CTP Rising Threshold | VTHP1 | 3.00 | 3.33 | 3.66 | V | SEL > 1.5 V |
| | VTHP2 | 1.98 | 2.2 | 2.42 | V | SEL < 1.0 V |
| CTP Falling Threshold | VTLP1 | 1.50 | 1.67 | 1.83 | V | SEL > 1.5 V |
| | VTLP2 | 0.9 | 1.0 | 1.1 | V | SEL < 1.0 V |
| Power-on Reset Time | TPR | 60 | 100 | 140 | mS | CTP = 0.1 μF |
| Reset On Delay Time | TDR | 10 | 50 | 100 | μS | CTP = 0.1 μF |
| RESET Output On Resistance | RRST | — | — | 100 | Ω | IRST = 1 mA |
| RESET Low Output Voltage | VRSTL | — | — | 0.4 | V | IRST = 2 μA, Vo1 = 1.2 V |
| [Watchdog Timer (WDT, WDINH, CTW)] | | | | | | |
| Runaway Operation Detection Time 1 | TWD1 | 420 | 700 | 980 | mS | CT = 1 μF, VO1 = 5 V; Time from final WDT signal input to RESET inversion |
| Runaway Operation Detection Time 2 | TWD2 | 277.2 | 462.0 | 646.8 | mS | CT = 1 μF, VO1 = 3.3 V |
| Runaway Operation Reset Time 1 | TWR1 | 204 | 340 | 476 | mS | CT = 1 μF, VO1 = 5 V |
| Runaway Operation Reset Time 2 | TWR2 | 156 | 260 | 364 | mS | CT = 1 μF, VO1 = 3.3 V |
| CTW Charge Current (Source) | IHCTW | 3.3 | 4.7 | 6.1 | μA | |
| CTW Discharge Current (Sink) | ILCTW | 3.4 | 4.8 | 6.2 | μA | |
| CTW Rapid Discharge Resistance | RCTWon1 | — | 16 | 50 | Ω | When WDT signal input is active. |
| | RCTWon2 | — | 0.5 | 2.5 | kΩ | ACC: L, WDINH: H |
| CTW Rising Threshold | VTHW1 | 3.00 | 3.33 | 3.66 | V | SEL > 1.5 V |
| | VTHW2 | 1.98 | 2.20 | 2.42 | V | SEL < 1.0 V |
| CTW Falling Threshold | VTLW1 | 1.50 | 1.67 | 1.83 | V | SEL > 1.5 V |
| | VTLW2 | 0.9 | 1.0 | 1.1 | V | SE L ≤ 1.0 V |
| WDT Rrising Threshold | VTHWDT1 | 3.00 | 3.33 | 3.66 | V | SEL > 1.5 V |
| | VTHWDT2 | 1.98 | 2.20 | 2.42 | V | SEL < 1.0 V |

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●**Electrical characteristics** (Unless otherwise specified, Ta = 25°C, VIN1 = VIN2 = 13.2 V)

| Parameter | Symbol | Limits Min. | Limits Typ. | Limits Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| WDT Falling Threshold | VTLWDT1 | 1.50 | 1.67 | 1.83 | V | SEL > 1.5 V |
| | VTLWDT2 | 0.9 | 1.0 | 1.1 | V | SEL < 1.0 V |
| WDT Input Current | IWDT | 0.5 | 1.0 | 2.0 | μA | VWDT = 5 V, SEL > 1.5 V |
| WDT Ddge Pulse Width | TPULSE | 100 | 190 | 300 | μS | |
| WDINH Input Voltage At High Level | VIH | 0.8X Vo1 | — | — | V | |
| WDINH Input Voltage Low Level | VIL | — | — | 0.3X Vo1 | V | |
| WDT Input Current | IWDINH | 1 | 2 | 4 | μA | VWDINH = 5 V, SEL < 1.0 V |
| [Bu Voltage Detection Circuit (BuM, BuDET)] | | | | | | |
| BuM Detection Voltage (Rising) BuDET: H→L, AccDET: H→L | VTHB | 1.214 | 1.252 | 1.290 | V | IC without heat sink |
| BuM Detection Voltage (Falling) BuDET: L→H, AccDET: L→H | VTLB | 1.148 | 1.184 | 1.220 | V | IC without heat sink |
| BuDET1 High Output Voltage | VBDTH1 | Vo1 -0.4 | Vo1 -0.2 | — | V | Iout = -5 mA |
| BuDET1 Low Output Voltage | VBDTL1 | — | 0.15 | 0.40 | V | Iout = 5 mA |
| BuDET2 High Output Voltage | VBDTH2 | Vo2 -0.4 | Vo2 -0.2 | — | V | Iout = -5 mA |
| BuDET2 Low Output Voltage | VBDTL2 | — | 0.15 | 0.40 | V | Iout = 5 mA |
| BuM Input Current | IBM1 | 0 | 4 | 110 | nA | BuM = 1 V |
| | IBM2 | 0 | 20 | 110 | nA | BuM = 2 V |
| [MUTE One-shot Pulse Generation Circuit (MUTE, CE)] | | | | | | |
| MUTE Pulse Width | Tm1 | 0.6 | 1.0 | 1.4 | S | CE = 1 μF, SEL > 1.5 V |
| | Tm2 | 0.6 | 1.0 | 1.4 | S | CE = 1 μF, SEL < 1.0 V |
| MUTE Pulse On Dalay Time | Td1 | 0 | 5 | 10 | μS | CE = 1 μF, SEL > 1.5 V |
| | Td2 | 0 | 8 | 16 | μS | CE = 1 μF, SEL < 1.0 V |
| CE Charge Resistance 1 | RTM1 | 0.7 | 1.0 | 1.3 | MΩ | When MUTE is on (resistance while charging). |
| CE Charge Resistance 2 | RTM2 | 8.0 | 11.5 | 15.0 | kΩ | When MUTE is off (resistance when stabilized after charging). |
| CE Rapid Discharge Resistance | RCEon | — | 4 | 20 | Ω | Must satisfy Td. |
| CE Output Saturation Voltage | VCEL | — | 0.1 | 0.3 | V | CE output on, ICE = 0 μA |
| CE-CMP Threshold (rising) | VTHCE1 | 3.00 | 3.33 | 3.66 | V | SEL > 1.5 V |
| | VTHCE2 | 1.98 | 2.2 | 2.42 | V | SEL < 1.0 V |
| CE-CMP Threshold (falling) | VTLCE1 | 1.50 | 1.67 | 1.83 | V | SEL > 1.5 V |
| | VTLCE2 | 0.9 | 1.0 | 1.1 | V | SEL < 1.0 V |
| MUTE Output Saturation Voltage | VMUTEL | — | 0.2 | 0.4 | V | IMUTE = 5 mA |
| [ACC Voltage Detection & Delay Circuit (ACCM, CD, ACCDET)] | | | | | | |
| ACCM Detection Voltage (Rising) | VTHA | 1.214 | 1.252 | 1.290 | V | IC without heat sink, BuM = H |
| ACCM Detection Voltage (Falling) | VTLA | 1.148 | 1.184 | 1.220 | V | IC without heat sink, BuM = H |
| ACCM Positive Clamp Voltage | VHACC | 8 | 11 | 14 | V | IACCM = +5 mA |
| ACCM Negative Clamp Voltage | VLACC | -0.30 | -0.15 | 0 | V | IACCM = -12 mA |
| ACCM Input Current 1 | IACC1 | -5 | -1 | 0 | μA | ACCM = 0 V |
| ACCM Input Current 2 | IACC2 | 0 | 10 | 110 | nA | ACCM = 2 V |
| CD Delay Time | TdLH | 6 | 10 | 14 | mS | CD = 0.1 μF |
| | TdHL | 6 | 10 | 14 | mS | CD = 0.1 μF |
| CD Charge Resistance | ICDH | 60 | 90 | 120 | kΩ | |
| CD Discharge Resistance | ICDL | 60 | 90 | 120 | kΩ | |
| CD-CMP Threshold (Rising) | VTHCD1 | 3.00 | 3.33 | 3.66 | V | SEL > 1.5 V |
| | VTHCD2 | 1.98 | 2.2 | 2.42 | V | SEL < 1.0 V |
| CD-CMP Threshold (Falling) | VTLCD1 | 1.50 | 1.67 | 1.84 | V | SEL > 1.5 V |
| | VTLCD2 | 0.9 | 1.0 | 1.1 | V | SEL < 1.0 V |
| ACCDET Output Saturation Voltage | VADTL | — | 0.2 | 0.4 | V | IADT = 5 mA |

⦿ This IC is not designed to be radiation-resistant.

●**Reference data** (Unless otherwise specified, VIN1 = VIN2 = 13.2 V)

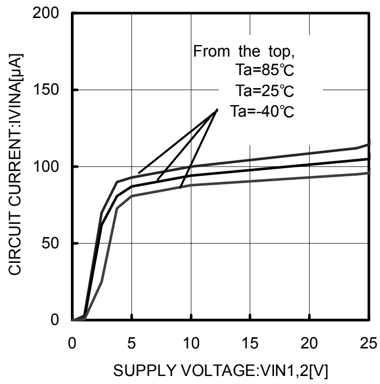



Fig.1 Total Circuit Current A

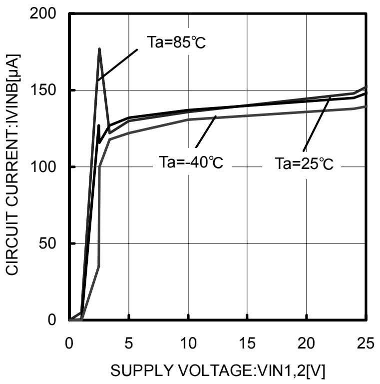



Fig.2 Total Circuit Current B

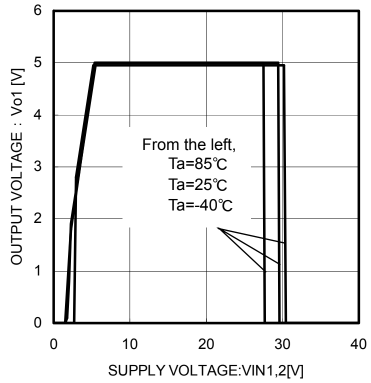



Fig.3 Vo1 Line Regulation

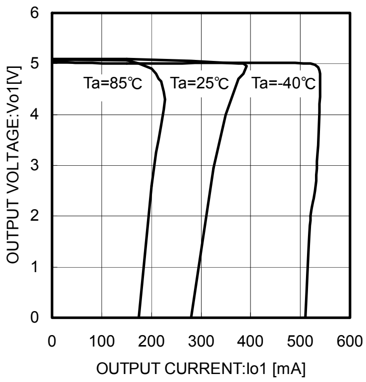



Fig.4 Vo1 Load Regulation

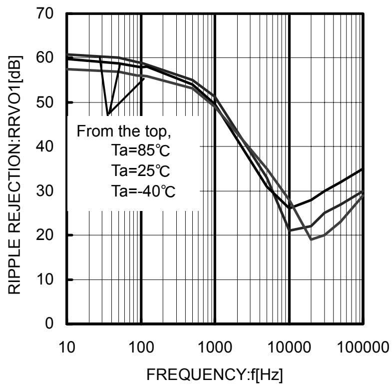



Fig.5 VO1 Ripple Rejection
VO1 = 5V

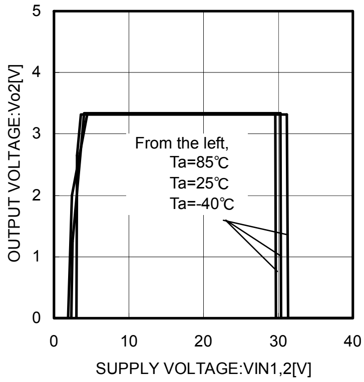



Fig.6 Vo2 Line Regulation

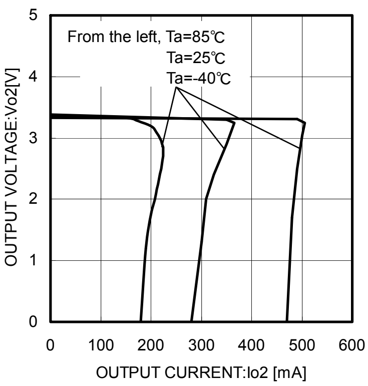



Fig.7 Vo2 Load Regulation

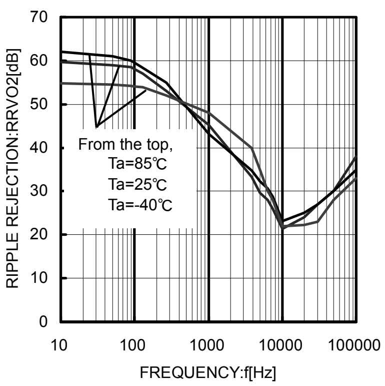



Fig.8 VO2 Ripple Rejection

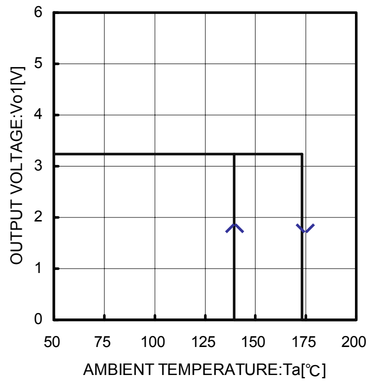



Fig.9 Thermal Shutdown Circuit

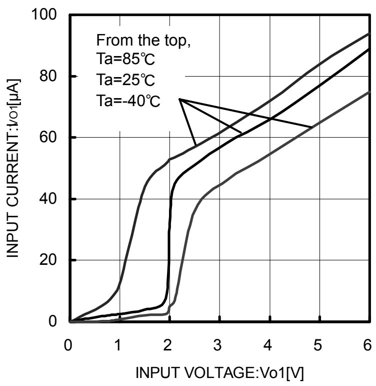



Fig.10 VO1 Sink Current

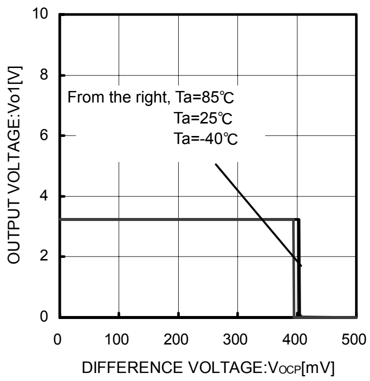



Fig.11 OCP Detection Voltage

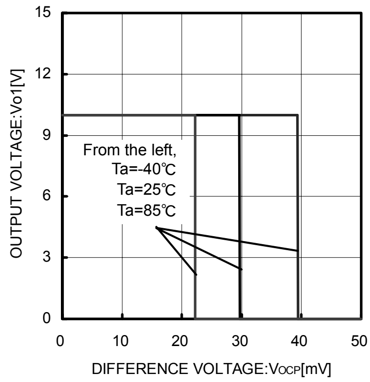



Fig.12 External OCP
Detection Voltage

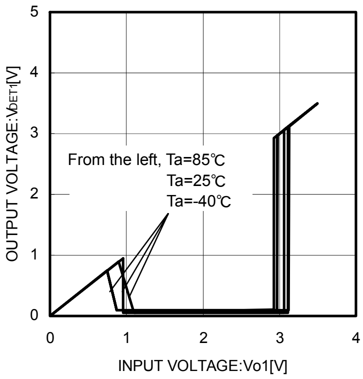



Fig.13 Vo1 Output Detection Voltage

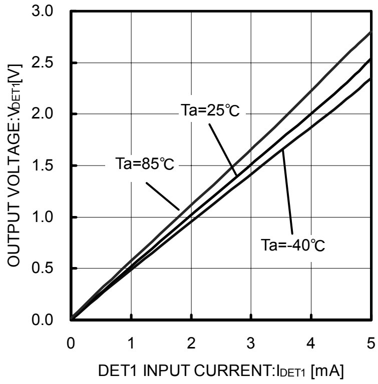



Fig.14 DET1 Output Voltage

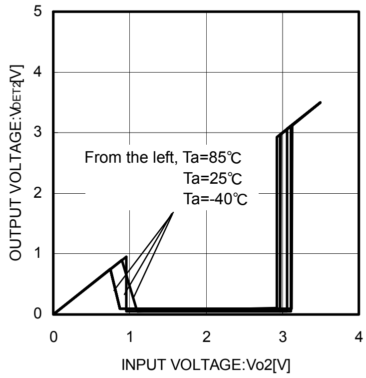



Fig.15 Vo2 Output Detection Voltage

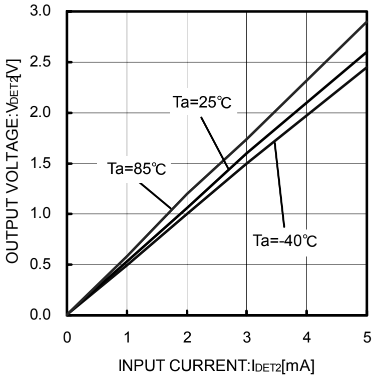



Fig.16 DET2 Output Voltage

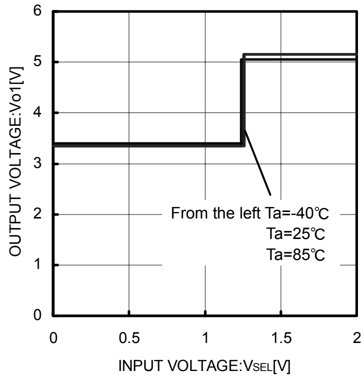



Fig.17 SEL Threshold Voltage

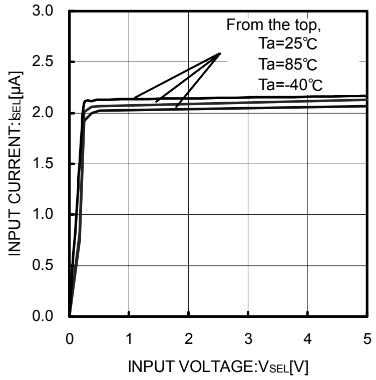



Fig.18 SEL Input Current

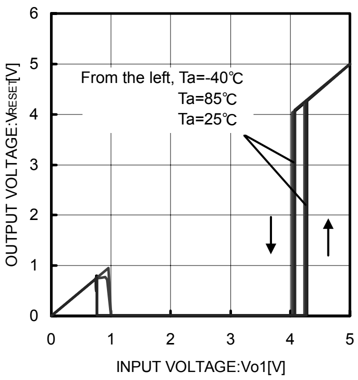



Fig.19 RESET Threshold Voltage

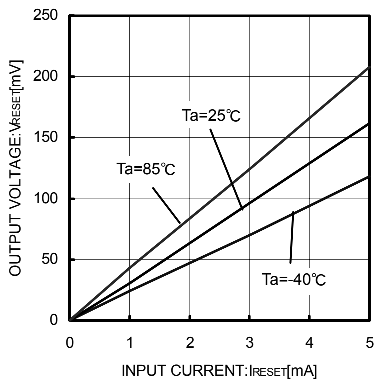



Fig.20 RESET Output Voltage

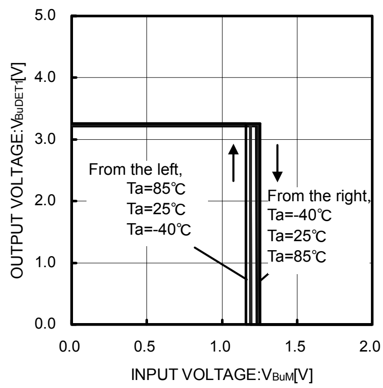



Fig.21 BuDET1 Detection Voltage

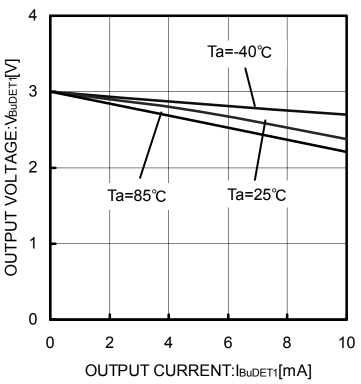



Fig.22 BuDET1 High Output Voltage

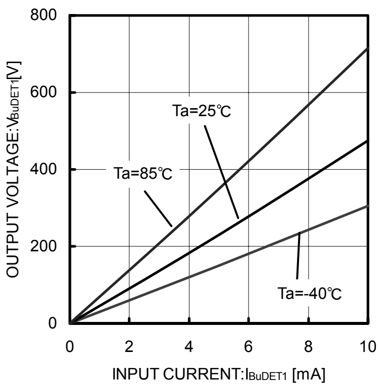



Fig.23 BuDET1 Low Output Voltage

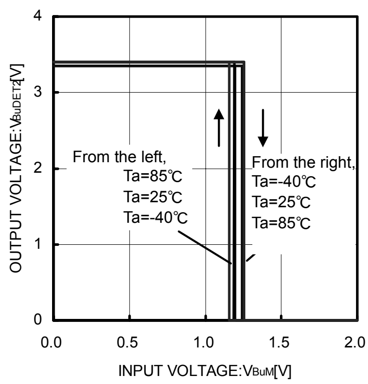



Fig.24 BuDET2 Detection Voltage

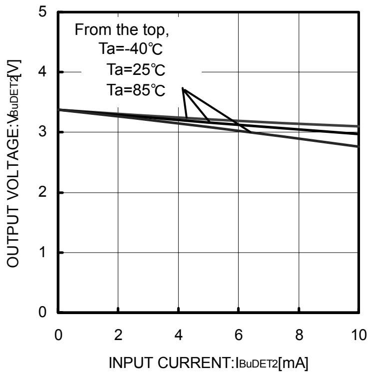



Fig.25 BuDET2 High Output Voltage

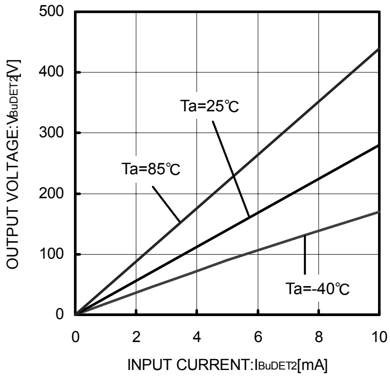



Fig.26 BuDET2 Low Output Voltage

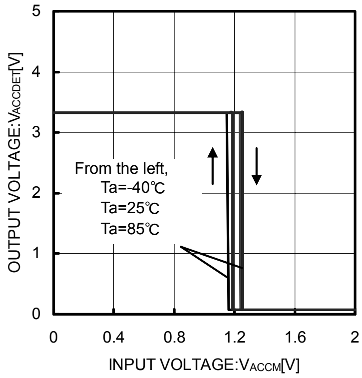



Fig.27 ACCDET Detection Voltage

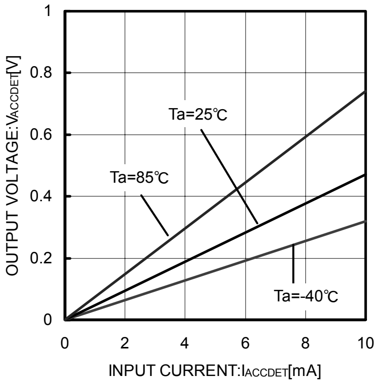



Fig.28 ACCDET Output Voltage

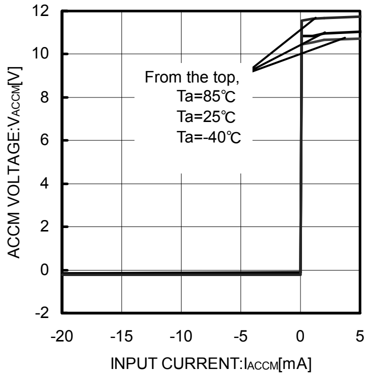



Fig. 29 ACCM Positive/Negative Clamp Voltage

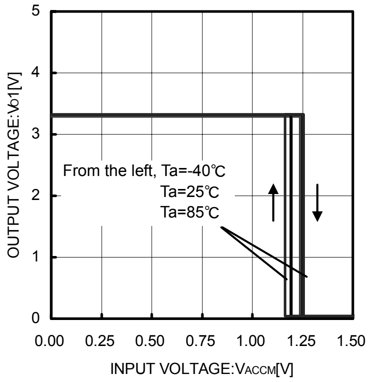



Fig.30 ACC Detection Voltage

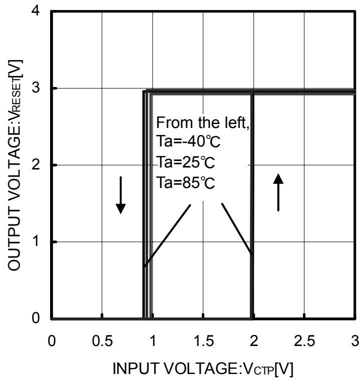



Fig.31 CTP Threshold Voltage 1 (SEL = L)

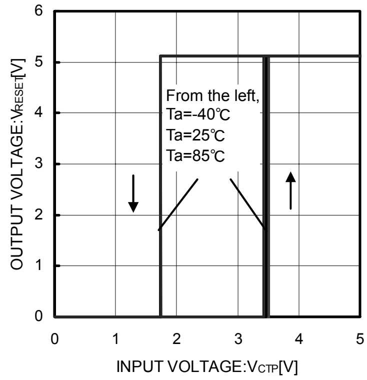



Fig.32 CTP Threshold Voltage 2 (SEL = H)

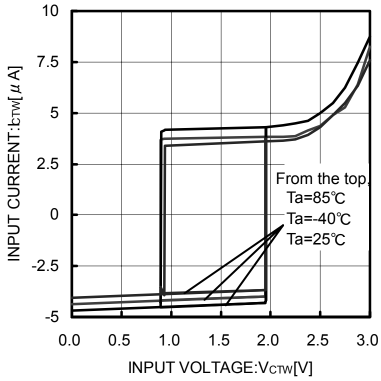



Fig.33 CTW Threshold 1 (SEL = L)

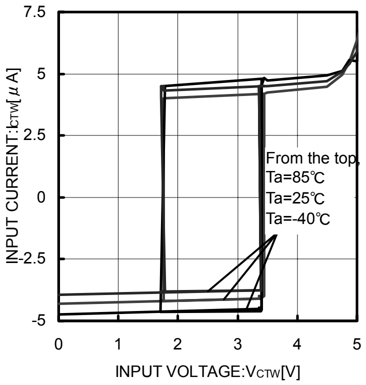



Fig.34 CTW Threshold 2 (SEL = H)

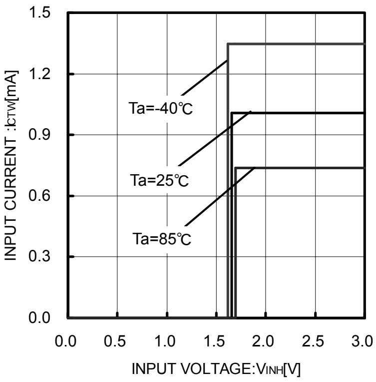



Fig.35 INH Threshold 1 (SEL = L)

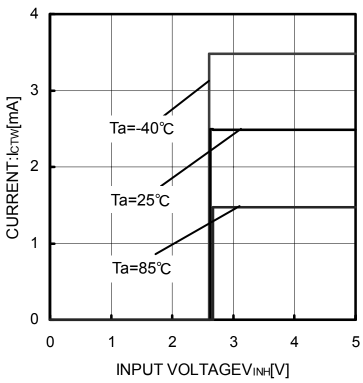



Fig.36 INH Threshold 2 (SEL = H)

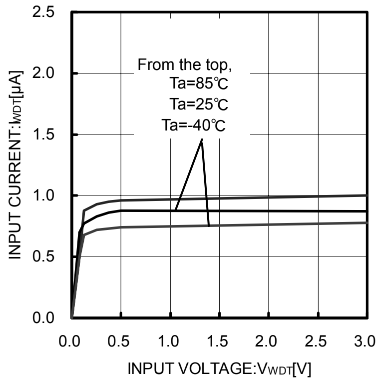



Fig.37 WDT Input Current 1
(SEL = L)

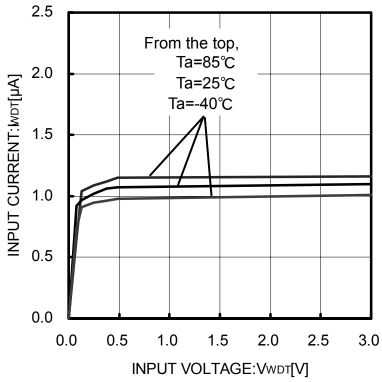



Fig.38 WDT Input Current 2
(SEL = H)

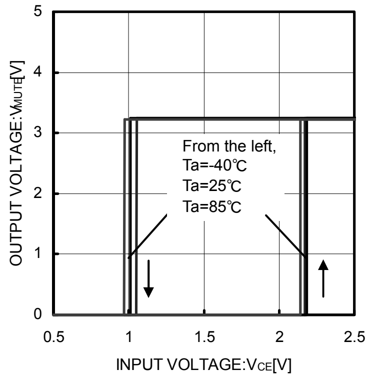



Fig.39 CE-CMP Threshold 1
(SEL = L)

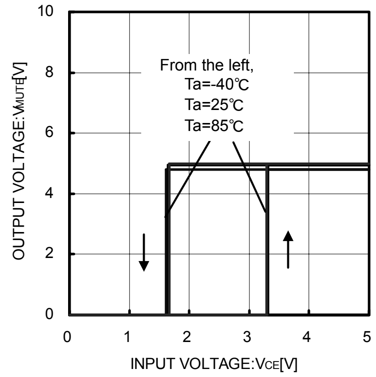



Fig.40 CE-CMP Threshold 2
(SEL = H)

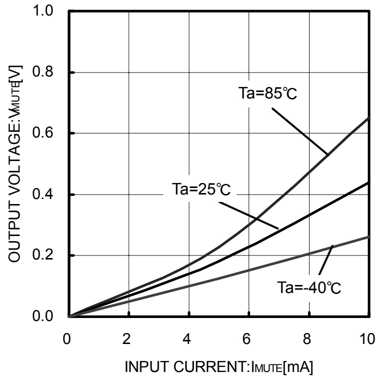



Fig.41 MUTE Output Voltage

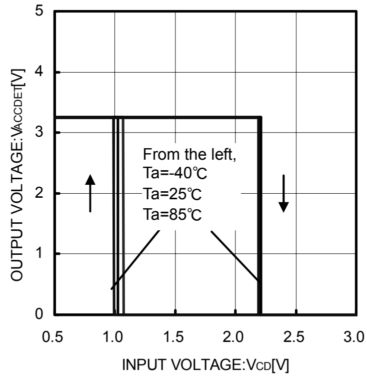



Fig.42 CD-CMP Threshold 1
(SEL = L)

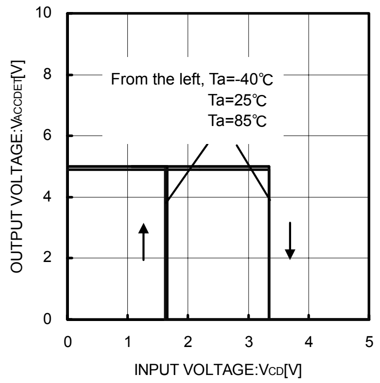



Fig.43 CD-CMP Threshold 2
(SEL = H)

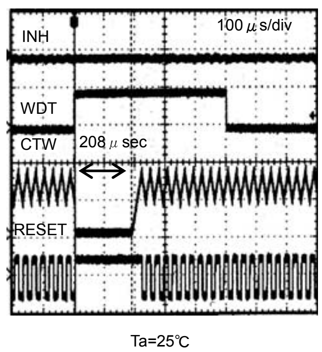



Fig.44 WDT Edge Pulse Width

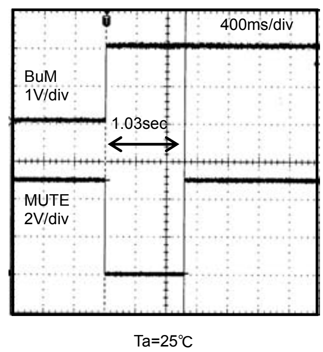



Fig.45 MUTE Timer Time (Low→High)

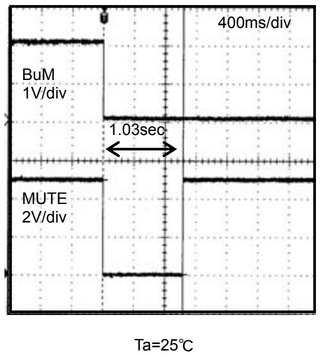



Fig.46 MUTE Timer Time (High→Low)

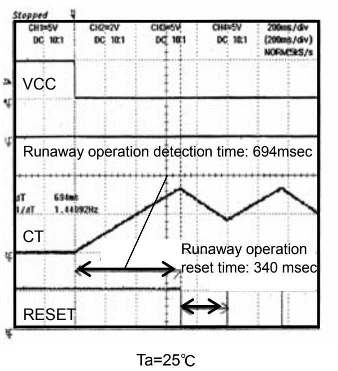



Fig.47 Runaway Operation
RESET Time

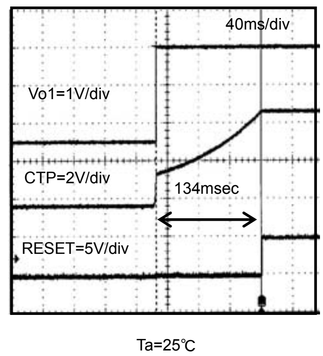



Fig.48 Power-on Reset Time

●**Block diagram, IC package & timing chart**

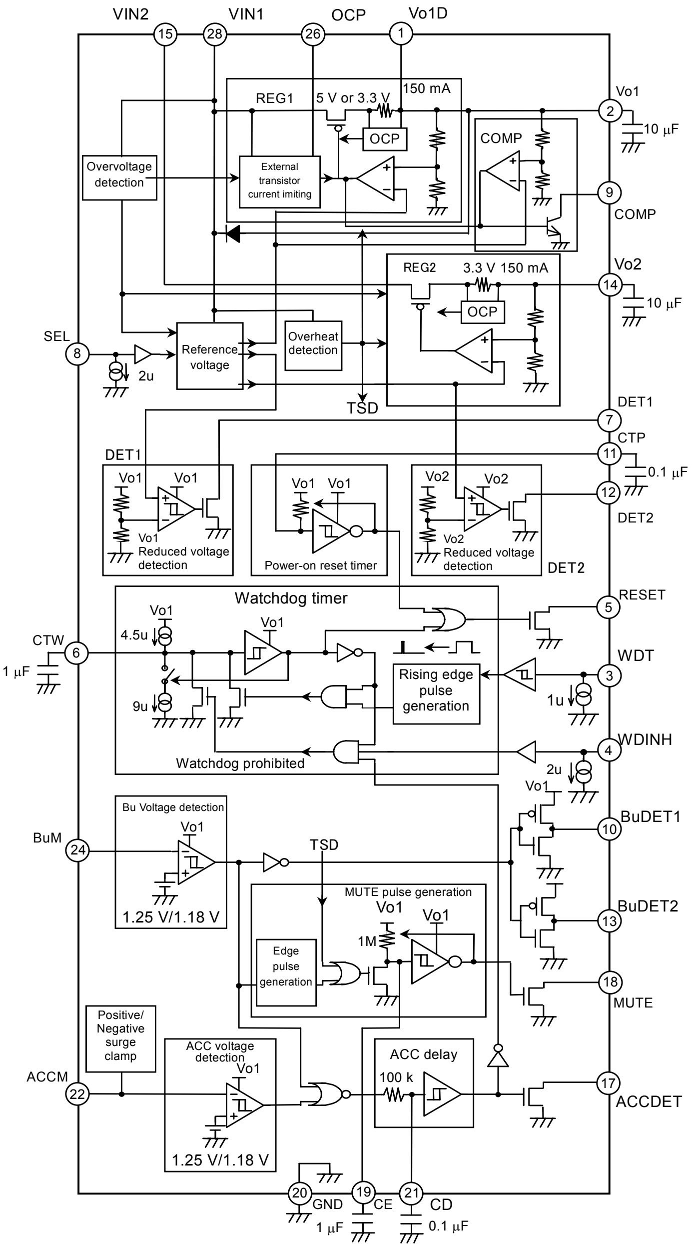



Fig.49 Block Diagram

| No. | Pin name | Function |
|---|---|---|
| 1 | Vo1D | Main regulator built-in boost transistor output pin |
| 2 | Vo1 | Main regulator output voltage monitor/Vo1 circuit power supply pin |
| 3 | WDT | Watchdog pulse signal input pin |
| 4 | WDINH | Watchdog prohibit signal input pin (prohibits WDT when ACC is low or WDINH is high). Reset signal output pin |
| 5 | RESET | Reset signal output pin |
| 6 | CTW | Runaway operation detection time setting capacitor connection pin |
| 7 | DET1 | Vo1 reduced-voltage detection signal output pin |
| 8 | SEL | Main regulator output voltage and reduced-voltage detection voltage selection input pin |
| 9 | COMP | Elevated output detection output |
| 10 | BuDET1 | +B drop detection signal output pin (Vo1 at high output) |
| 11 | CTP | Power-on reset time setting capacitor connection pin |
| 12 | DET2 | Vo2 reduced-voltage detection signal output pin |
| 13 | BuDET2 | +B drop detection signal output pin (Vo2 at high output) |
| 14 | Vo2 | Sub-regulator output pin |
| 15 | VIN2 | Sub-regulator input pin |
| 16 | N.C. | NC pin |
| 17 | ACCDET | ACC voltage detection signal output pin |
| 18 | MUTE | MUTE output pin |
| 19 | CE | MUTE pulse width setting capacitor connection pin |
| 20 | GND | GND pin |
| 21 | CD | ACCDET delay time setting capacitor connection pin |
| 22 | ACCM | Acc voltage monitor input pin |
| 23 | N.C. | NC pin |
| 24 | BuM | Battery voltage monitor input pin |
| 25 | N.C. | NC pin |
| 26 | OCP | Main regulator external boost transistor current limit setting resistance connection pin |
| 27 | N.C. | NC pin |
| 28 | VIN1 | Main regulator connection pin |
| FIN | FIN | Heat dissipation fin (sub) (Connect to GND pin.) |

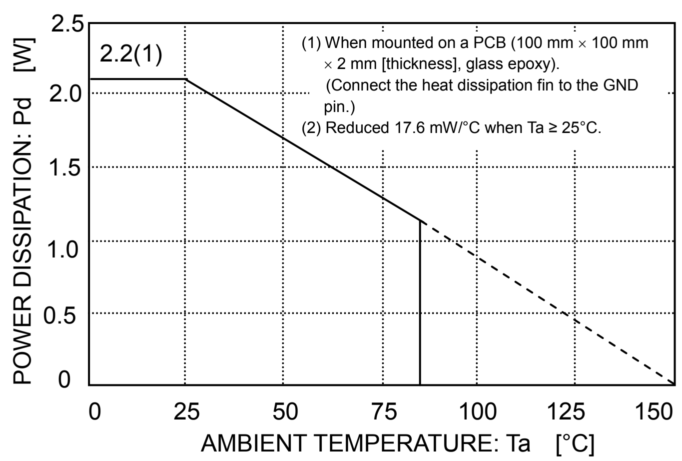
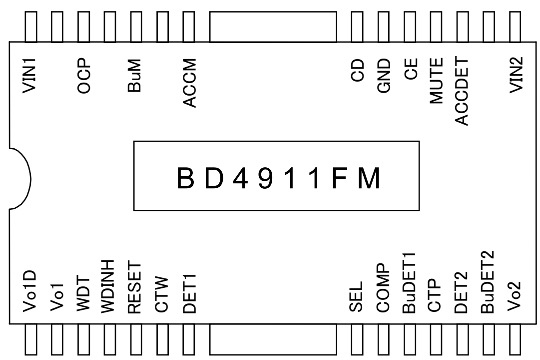



Fig.50 Power Dissipation Characteristics




UNIT: (mm)

Fig.51 Pin Assign Diagram

## ●Block diagram, IC package & timing chart

### ○I/O Timing Chart

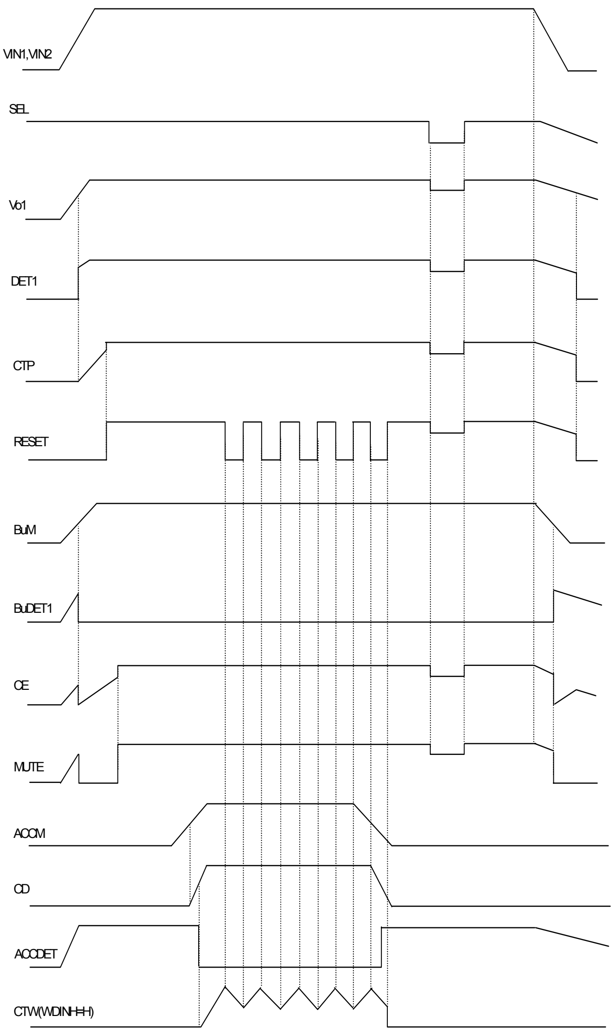



Fig.52

### ○Watchdog timer and runaway operation reset timing chart 1

Prohibit watchdog when the following conditions are both satisfied. ACC: Low level and WDINH: High level.

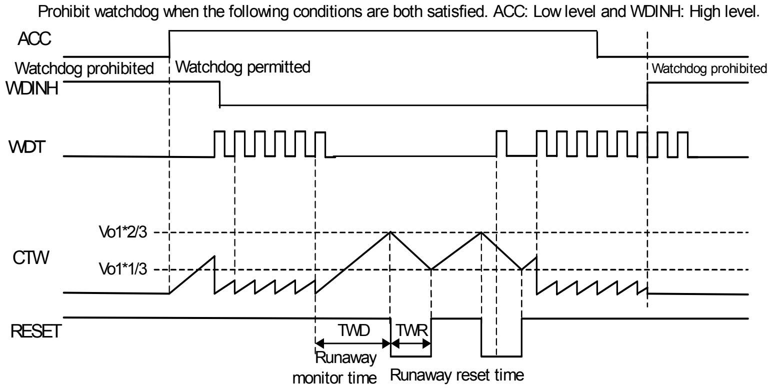



Fig.53

### ○Watchdog timer and runaway operation reset timing chart 2

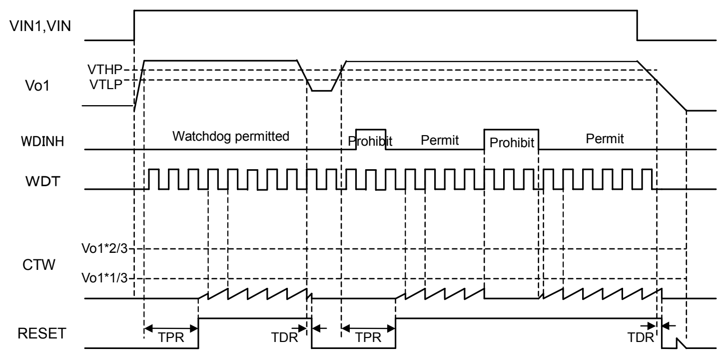



Fig.54

### ○Power-on reset and reduced-voltage reset timing chart

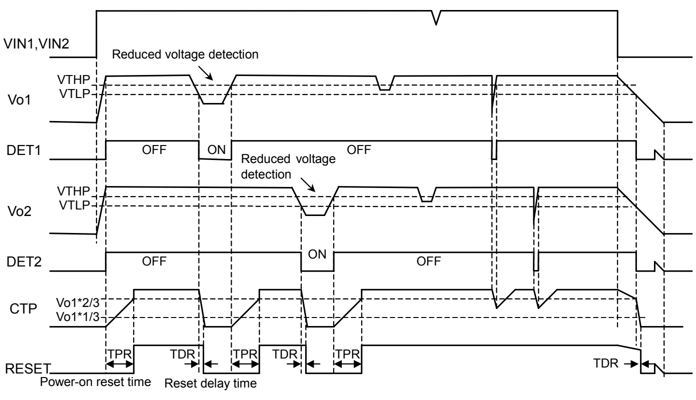



Fig.55

### ○BuDET1, BuDET2, ACCDET, and MUTE timing chart

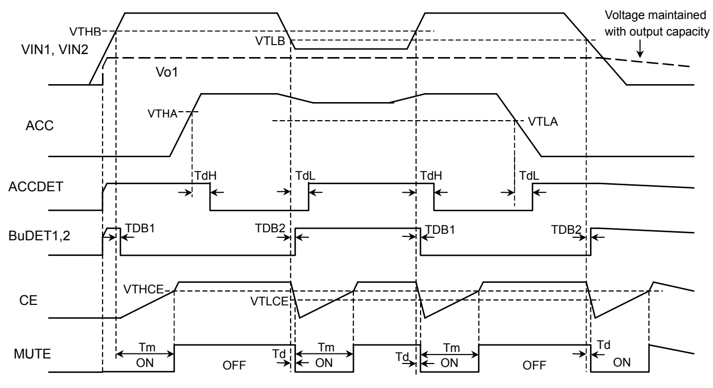
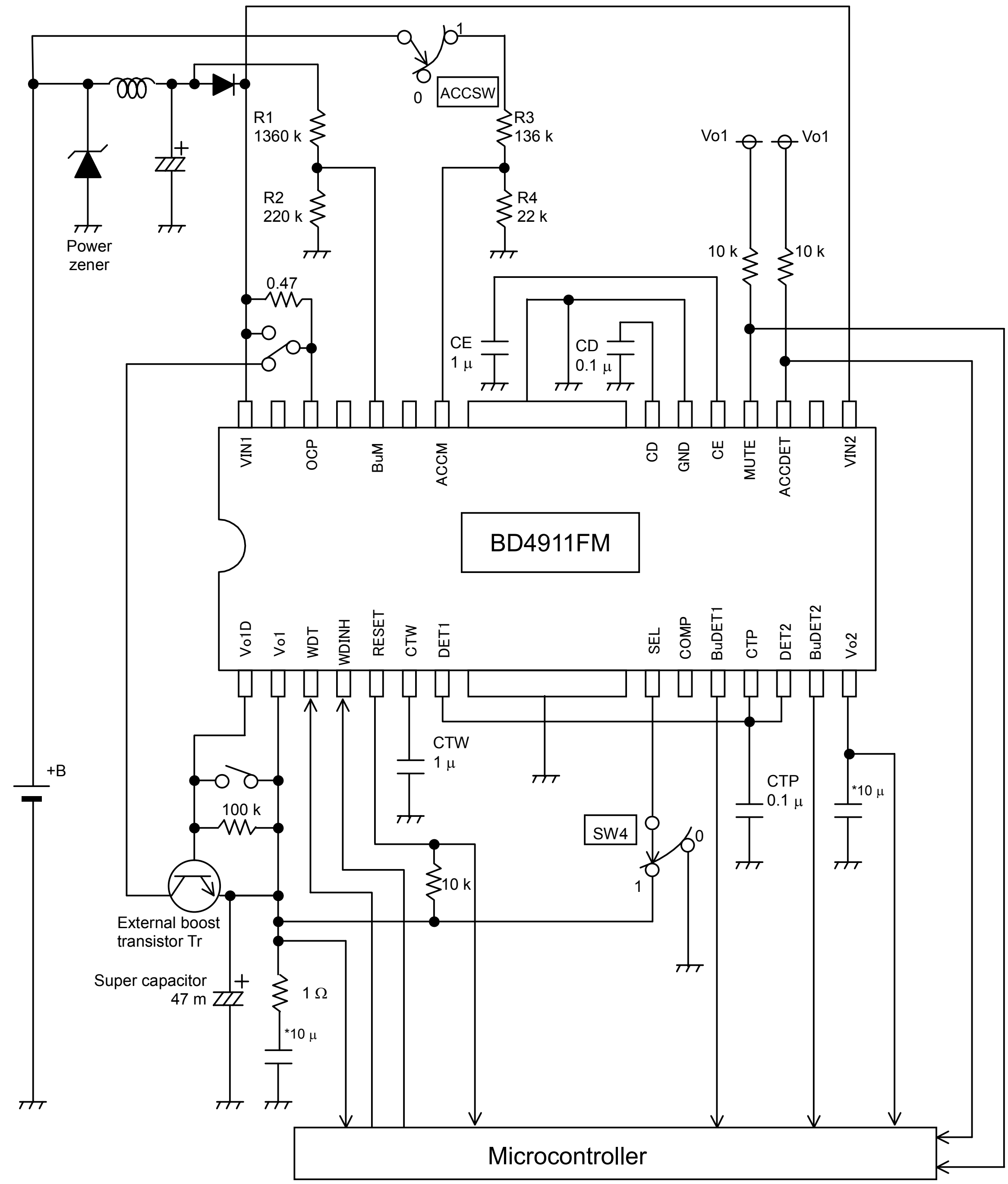



Fig.56

●**Application circuits example**




| | SW4 |
|---|---|
| When Vo1 outputs 5 V | 1 |
| When Vo1 outputs 3.3 V | 0 |

(Unit) Resistor: Ω
Capacitor: F

*Select the output capacitance carefully after referring to all operating precautions.

Fig.57 Application Circuits example

## ●Operation Notes

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. GND voltage
   The potential of GND pin must be minimum potential in all operating conditions.

3. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

5. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6. Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

7. Regarding input pin of the IC
   This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
   
   When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
   
   When GND > Pin B, the P-N junction operates as a parasitic transistor.
   
   Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

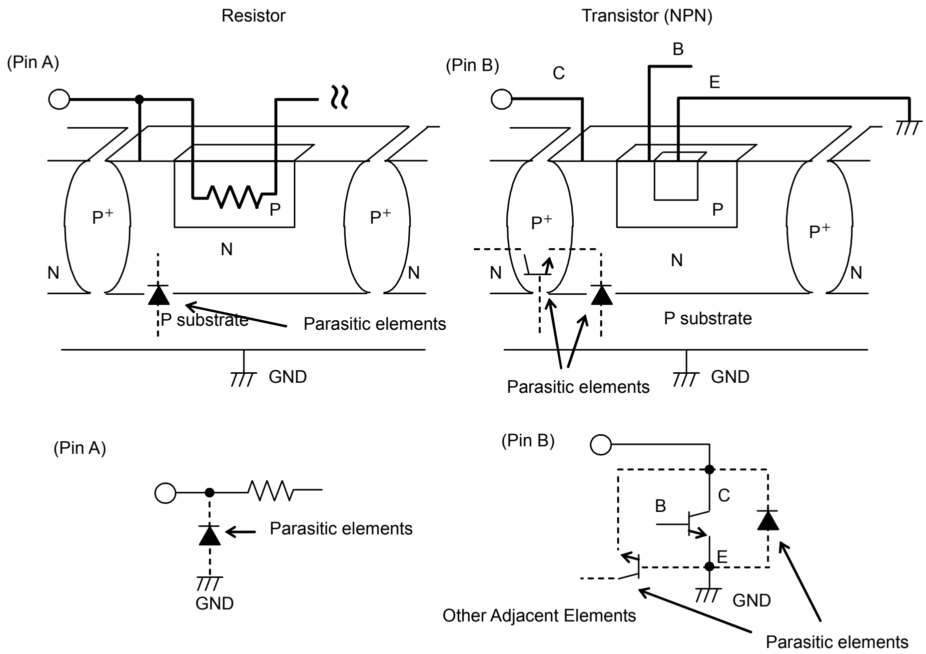



Fig.58 Example of a Simple Monolithic IC Architecture

8. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

9. Recommended operating ranges

Proper circuit functionality is guaranteed within the operating temperature range for power supply voltages that fall within the recommended ranges.
Although standard electrical characteristics values are not guaranteed, characteristics values will not vary suddenly within these ranges.

10. Output capacitors

Capacitors for stopping oscillation must be placed between each output pin and the GND pin.
It is recommended to use a 10 μF ceramic capacitor (B characteristics). When using an external boost transistor, the ceramic capacitor described above should be connected in series with a 1 Ω resistor. Abrupt input voltage and load fluctuations can affect output voltages. Output capacitor capacitance values should be determined after sufficient testing of the actual application.

11. Applications or inspection processes with modes where the potentials of the VIN pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements. For example, such damage might occur when VIN is shorted with the GND pin while an external capacitor is charged. Use capacitors that fall within the range listed for each pin in Table 1. It is recommended to insert a diode to prevent back current flow in series with VIN, or bypass diodes between VIN and each pin. If the VIN pin carries a lower voltage than the GND pin, insert a protective diode between the VIN and GND pins.

| Output pin | Output capacitor |
|---|---|
| Vo1 | 10 μF to 2200 μF |
| Vo2 | 10 μF to 2200 μF |

Table 1

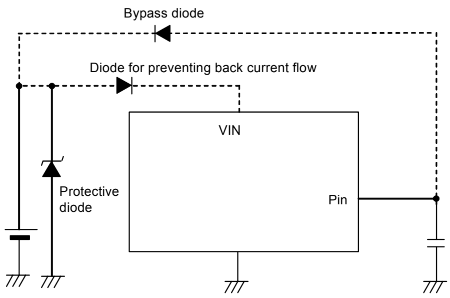



Fig.59

12. Overcurrent protection circuits

The IC incorporates a built-in overcurrent protection circuit for each output pin. Each circuit is specifically designed for the current capacity of the corresponding pin and acts to prevent damage to the IC when an overcurrent flows.
The protection circuits use drooping type current limiting (when using the built-in transistor) or dropping fold-back type current limiting (when using the external boost transistor). They are designed to limit current flow by not latching up in the event of a large and instantaneous current flow originating from a large capacitor or other component. Their design allows for sufficient safety margins. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits (for example, applications where the IC is continuously connected to a load that significantly exceeds the output current capacity).
Use caution regarding thermal design, as the output current capacity varies negatively with the temperature characteristics.

13. Overvoltage protection circuit

Overvoltage protection is designed to turn off all output voltages when the voltage differential between the VIN and GND pins exceeds approximately 31 V (at room temperature). Use caution when determining the power supply voltage range to use.

14. Thermal shutdown circuit (TSD)
    This IC incorporates a built-in thermal shutdown circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature Tj will trigger the thermal shutdown circuit to turn off all output power elements. The circuit will automatically reset once the chip's temperature Tj drops.
    Operation of the thermal shutdown circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the thermal shutdown circuit.
15. Ground precautions
    Pattern routes connecting the ground points, indicated in application circuits example, to the GND pin should be sufficiently short and should be positioned to avoid electrical interference.

16. Bypass capacitor between the VIN and GND pins
    It is recommended to insert a 0.47 μF to 10 mF bypass capacitor between the VIN and GND pins. Capacitance values vary with application. Capacitors should be tested in actual implementations, and designs should allow for sufficient margins. Failure to use the optimum capacitance value may lead to output oscillation and other issues.

17. Applications with modes where the potentials of the input pins (VIN1, VIN2) and GND pins and other output pins may be reversed from their normal states may cause damage to the IC's internal circuitry. In particular, it is recommended to create a bypass route with diodes or other components when loads including large inductance components are connected where BEMF may be generated during startup or when output is turned off.

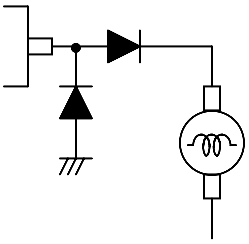


Fig.60

18. Always verify the characteristics of example application circuits prior to their use. When changing other external circuit b constants, allow for sufficient margins after considering the variability of both the ROHM IC and external components, including both static and transient characteristics.

●**Selecting a model name when ordering**

| B | D | 4 | 9 | 1 | 1 | | F | M | | | – | E | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

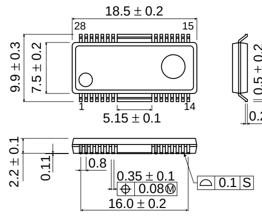
Part number
BD4911

Package type
FM: HSOPM28

Taping type
E2 = Reel-wound embossed taping
(HSOPM28)

## HSOP-M28

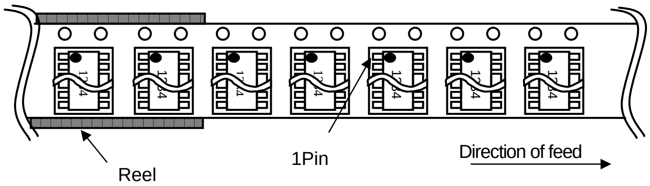
<Dimension>




(Unit:mm)

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 1500pcs |
| Direction of feed | E2<br>(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |




※When you order , please order in times the amount of package quantity.

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