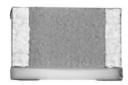


# **High Precision Wraparound Thin Film Chip Resistors**

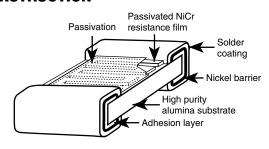


## **LINKS TO ADDITIONAL RESOURCES**

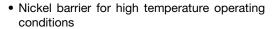


Utilizing proven expertise in thin film resistors, Vishay provides a chip manufactured according to CECC with the same reliability and stability found in QPL resistors. These chips are available in a wide range of sizes, values, and performance characteristics.

### CONSTRUCTION



### **FEATURES**





 Tight TCR < 10 ppm/°C, and in lot tracking < 5 ppm/°C in (-55 °C, +155 °C temperature range)



- Very low noise < 35 dB and voltage coefficient 0.1 ppm/V</li>
- Non-inductive
- Laser trimmed down to 0.1 %
- Wraparound resistance less than 0.01  $\Omega$
- Antistatic waffle-pack or tape and reel packaging available
- High stability (0.05 % 1000 h at Pn at +70 °C)
- Withstand moisture resistance test of AEC-Q200
- According to CECC 40401-010
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912"><u>www.vishav.com/doc?99912</u></a>

# Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

STANDARD ELECTRICAL SPECIFICATIONS						
MODEL	SIZE	RESISTANCE RANGE (1) (2) Ω	RATED POWER Pn W	LIMITING ELEMENT VOLTAGE (UL) V	TOLERANCE ± %	TEMPERATURE COEFFICIENT ± ppm/°C
RV	0505	100 to 260K	0.125	50	0.1, 0.5, 1, 2, 5	10, 25
RV	0603	100 to 260K	0.125	50	0.1, 0.5, 1, 2, 5	10, 25
RV	0805	100 to 300K	0.200	50	0.1, 0.5, 1, 2, 5	10, 25
RV	1206	100 to 1M	0.330	75	0.1, 0.5, 1, 2, 5	10, 25

## Notes

- (1) Extended resistance range on request
- (2) For ohmic range versus tolerance and TCR, see detailed table

CLIMATIC SPECIFICATIONS		
Operating temperature range	-55 °C to +155 °C	
Storage temperature range	-55 °C to +155 °C	

MECHANICAL SPECIFICATIONS			
Resistive material	Nichrome		
Substrate material	Alumina		
Plating	Tin lead over nickel or tin silver over nickel or gold over nickel		
Marking resistance to solvents	Per CECC specs		

OHMIC RANGE VS. TOLERANCE AND TCR				
CASE SIZE	OHMIC RANGE $\Omega$	TOLERANCE %	TCR ppm/°C	
0505	100 < 500	0.5; 1; 2; 5	10, 25	
0505	500 to 260K	0.1; 0.5; 1; 2; 5	10, 25	
0603	100 < 500	0.5; 1; 2; 5	10, 25	
0603	500 to 260K	0.1; 0.5; 1; 2; 5	10, 25	
0805	100 < 500	0.5; 1; 2; 5	10, 25	
0805	500 to 300K	0.1; 0.5; 1; 2; 5	10, 25	
1206	100 < 500	0.5; 1; 2; 5	10, 25	
1206	500 to 1M	0.1; 0.5; 1; 2; 5	10, 25	

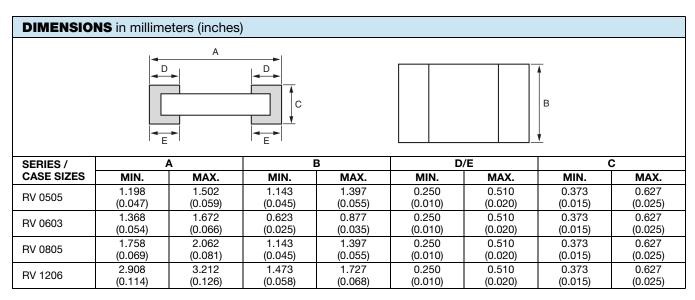


# Vishay Sfernice

TECHNICAL SPECIFICATIONS				
TEST	SPECIFICATIONS	CONDITIONS		
Absolute TCR	E: ± 25 ppm/°C / Y: ± 10 ppm/°C	-55 °C to +155 °C		
Absolute tolerance	$\pm 0.1 \%, \pm 0.5 \%, \pm 1 \%, \pm 2 \%, \pm 5 \% (R \ge 500 \Omega)$			
Absolute tolerance	$\pm 0.5 \%$ , $\pm 1 \%$ , $\pm 2 \%$ , $\pm 5 \%$ ( $R \ge 100 \Omega$ )			
Voltage coefficient	0.1 ppm/V			
Noise	-35 dB typical			
Thermal EMF	< 0.1 μV/°C			
Load life stability	± (0.1 % Rn <sup>(1)</sup> ± 0.05 Ω)	1000 h Pn at +70 °C		

#### Note

(1) Rn: nominal resistance



# **POPULAR OPTION**

AEC-Q200 moisture resistance

Option to order: 0058: specific production process to withstand 85 °C / 85 % RH at Pn/10

ENVIRONMENTAL TEST				
TEST	CONDITIONS	VALUES AND DRIFTS (△R/R ± %)		
1231	CONDITIONS	CECC REQUIREMENTS	TYPICAL PERFORMANCE	
Overload	6.25 x rated power / 2 s (or 2 UL)	$0.05~\%~{ m Rn}^{~(2)} + 0.05~\Omega$	0.01 % Rn <sup>(2)</sup>	
Climatic sequences (1)	-55 °C / +155 °C 5 moisture cycles	0.1 % Rn <sup>(2)</sup> + 0.05 Ω	0.02 % Rn <sup>(2)</sup>	
Thermal shock <sup>(1)</sup>	-55 °C / +155 °C 5 cycles 30 min	$0.05~\%~{ m Rn}^{~(2)} + 0.05~\Omega$	0.02 % Rn <sup>(2)</sup>	
Load life (1)	+70 °C/Pn 1000 h	0.1 % Rn <sup>(2)</sup> + 0.05 Ω	0.05 % Rn <sup>(2)</sup>	
Resistance to solder heat	+260 °C/ 10 s	$0.05~\%~{ m Rn}^{~(2)} + 0.05~\Omega$	0.02 % Rn <sup>(2)</sup>	
	+40 °C / 93 % HR Pn/10	0.1 % Rn <sup>(2)</sup> + 0.05 Ω	0.01 % Rn <sup>(2)</sup>	
Moisture resistance (1)	AEC-Q200 <sup>(3)</sup> 85 °C / 85 % RH / Pn/10 1000 h	0.5 % + 0.05 Ω	Max. < 0.3 % + 0.05 Ω	
High temperature storage	1000 h at + 155 °C	0.1 % Rn <sup>(2)</sup> + 0.05 Ω	0.05 % Rn <sup>(2)</sup>	
Bending <sup>(1)</sup>	10 bends / 2 mm / 5 s	0.05 % Rn <sup>(2)</sup> + 0.05 Ω	0.02 % Rn <sup>(2)</sup>	

## Notes

<sup>(1)</sup> Test requiring parts to be mounted on PCB will be performed with the requirement that termination alloy will be the same as solder paste alloy. Gold termination will be tested as B termination

<sup>(2)</sup> Rn: nominal resistance Pn: nominal power

<sup>(3)</sup> Option to order: 0058







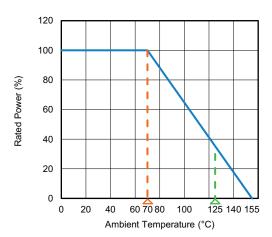
SPECIFIC CONDITIONS DUE TO TERMINATION TYPE				
TEST	CONDITIONS		VALUES AND DRIFTS	
IESI	B; G	N	VISHAY REQUIREMENTS	TYPICAL PERFORMANCE
Solderability	+235 °C/2 s Sn60Pb40 alloy	+245 °C/3 s Sn97Ag3 alloy	VISUAL INSPECTION	
High T° reflow profile	N/A	+255 °C/40 s (on parts)	0.02 % Rn <sup>(1)</sup> + 0.05 Ω	

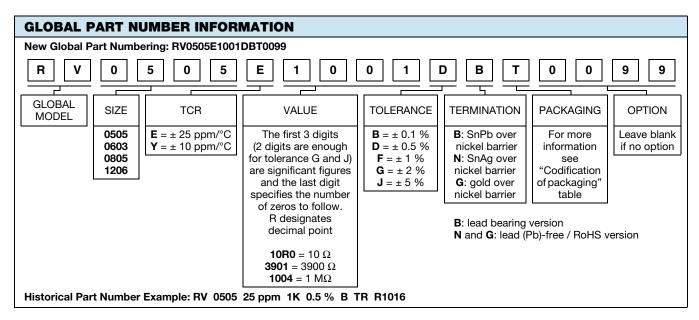
### Note

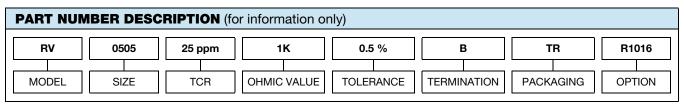
(1) Rn: nominal resistance Pn: nominal power

PAC	PACKAGING INFORMATION				
	NUMBER OF PIECES PER PACKAGE				
SIZE	WAFFLE PACK	TAPE AND REEL		TAPE	
	(2" x 2")	MIN.	MAX.	WIDTH	
0505	100		4000		
0603	100	100	5000	8 mm	
0805	100	100	4000	(0.315")	
1206	140		4000		

# **DERATING CURVE**











# Vishay Sfernice

CODIFICATION OF PACKAGING				
CODE 18	PACKAGING			
WAFFLE PACK				
W	100 min., 1 mult.			
WA	100 min., 100 mult. (available only in size 1206)			
PLASTIC TAPE (Standard	for all sizes.)			
Т	100 min., 1 mult.			
TA	100 min., 100 mult.			
ТВ	250 min., 250 mult.			
TC	500 min., 500 mult.			
TD	1000 min., 1000 mult.			
TE	2500 min., 2500 mult.			
TF	Full tape (quantity depending on size of chips)			
PAPER TAPE (Available for 0603, 0805, and 1206. Please consult Vishay Sfernice for other sizes.)				
PT	100 min., 1 mult.			
PA	100 min., 100 mult.			
PB	250 min., 250 mult.			
PC	500 min., 500 mult.			
PD	1000 min., 1000 mult.			
PE	2500 min., 2500 mult.			
PF	Full tape (quantity depending on size of chips)			



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