

SN54AHC367, SN74AHC367 HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS424E – JUNE 1998 – REVISED FEBRUARY 2002

- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

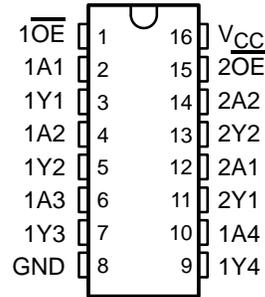
description

The 'AHC367 devices are hex buffers and line drivers designed for 2-V to 5.5-V V_{CC} operation.

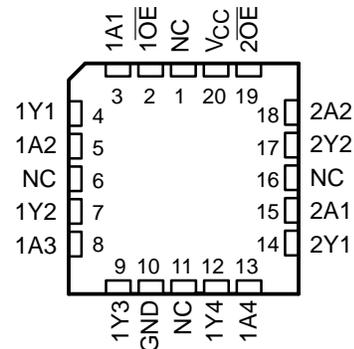
These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'AHC367 devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ($1OE$ and $2OE$) inputs. When OE is low, the device passes noninverted data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHC367 . . . J OR W PACKAGE
SN74AHC367 . . . D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC367 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC367N	SN74AHC367N
	SOIC – D	Tube	SN74AHC367D	AHC367
		Tape and reel	SN74AHC367DR	
	SSOP – DB	Tape and reel	SN74AHC367DBR	HA367
	TSSOP – PW	Tape and reel	SN74AHC367PWR	HA367
	TVSOP – DGV	Tape and reel	SN74AHC367DGV	HA367
–55°C to 125°C	CDIP – J	Tube	SNJ54AHC367J	SNJ54AHC367J
	CFP – W	Tube	SNJ54AHC367W	SNJ54AHC367W
	LCCC – FK	Tube	SNJ54AHC367FK	SNJ54AHC367FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
N package	67°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		SN54AHC367		SN74AHC367		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5		V
		V _{CC} = 3 V		2.1		
		V _{CC} = 5.5 V		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		V
		V _{CC} = 3 V		0.9		
		V _{CC} = 5.5 V		1.65		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50		μA
		V _{CC} = 3.3 V ± 0.3 V		-4		
		V _{CC} = 5 V ± 0.5 V		-8		
I _{OL}	Low-level output current	V _{CC} = 2 V		50		μA
		V _{CC} = 3.3 V ± 0.3 V		4		
		V _{CC} = 5 V ± 0.5 V		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		ns/V
		V _{CC} = 5 V ± 0.5 V		20		
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC367		SN74AHC367		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I _{OZ}	V _I = V _{CC} or GND, V _O = V _{CC} or GND, OE = V _{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	μA
C _i	V _I = V _{CC} or GND	5 V		3	10				10	pF
C _o	V _O = V _{CC} or GND	5 V		5.1						pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC367		SN74AHC367		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	4.7*	8.3*	1*	10*	1	10	ns	
t_{PHL}				4.7*	8.3*	1*	10*	1	10		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	5.1*	10.5*	1*	12.5*	1	12.5	ns	
t_{PZL}				5.1*	10.5*	1*	12.5*	1	12.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4*	10.5*	1*	12.5*	1	12.5	ns	
t_{PLZ}				4.9*	10.5*	1*	12.5*	1	12.5		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	6.1	11.8	1	13.5	1	13.5	ns	
t_{PHL}				6.2	11.8	1	13.5	1	13.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.4	14	1	16	1	16	ns	
t_{PZL}				6.8	14	1	16	1	16		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.2	13.6	1	15.5	1	15.5	ns	
t_{PLZ}				7.3	13.6	1	15.5	1	15.5		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC367		SN74AHC367		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.4*	5.9*	1*	7*	1	7	ns	
t_{PHL}				3.6*	5.9*	1*	7*	1	7		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	3.6*	7.2*	1*	8.5*	1	8.5	ns	
t_{PZL}				3.8*	7.2*	1*	8.5*	1	8.5		
t_{PHZ}	OE	Y	$C_L = 15\text{ pF}$	2.6*	7.2*	0*	8.5*	0	8.5	ns	
t_{PLZ}				2.6*	7.2*	0*	8.5*	0	8.5		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	4.3	7.9	1	9	1	9	ns	
t_{PHL}				4.5	7.9	1	9	1	9		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	4.6	9.2	1	10.5	1	10.5	ns	
t_{PZL}				4.9	9.2	1	10.5	1	10.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	3.4	9.2	0	10.5	0	10.5	ns	
t_{PLZ}				4.5	9.2	0	10.5	0	10.5		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHC367			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.2		V
$V_{IH(D)}$	High-level dynamic input voltage		3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

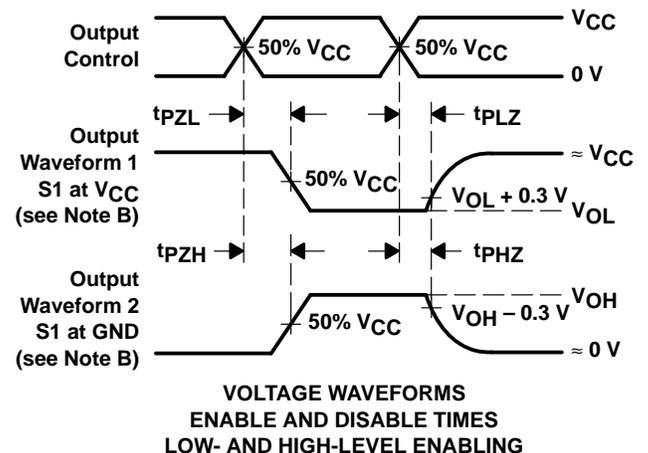
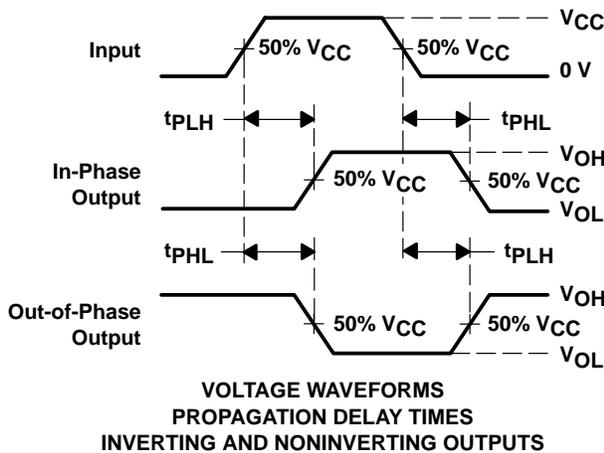
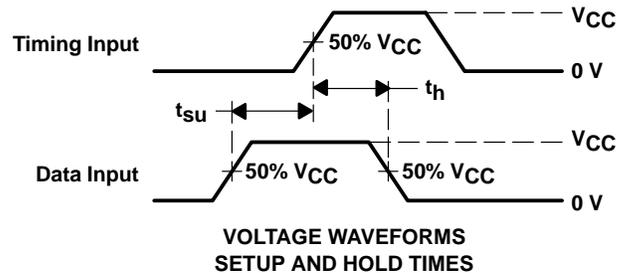
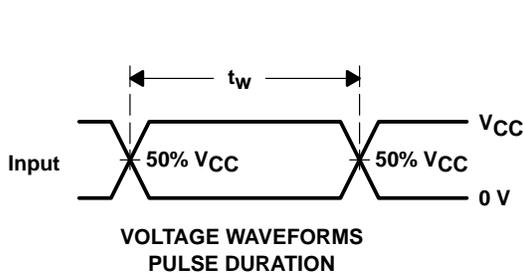
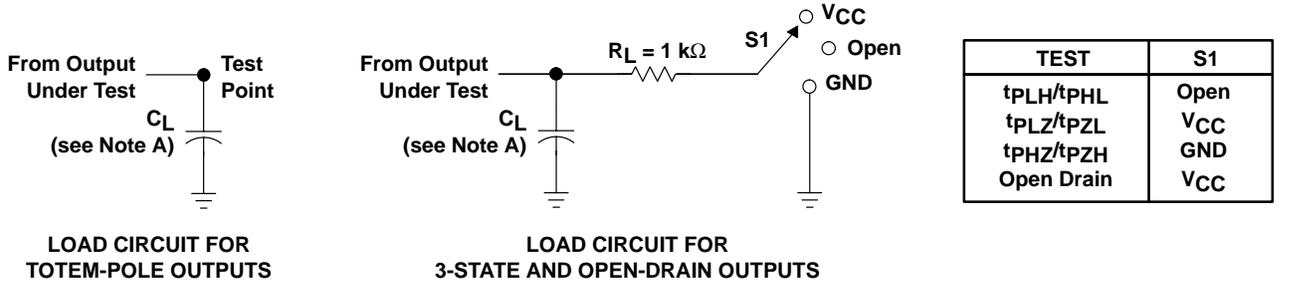


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operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled No load, $f = 1\text{ MHz}$	22.4	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC367D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC367	Samples
SN74AHC367DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC367	Samples
SN74AHC367N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC367N	Samples
SN74AHC367PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA367	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

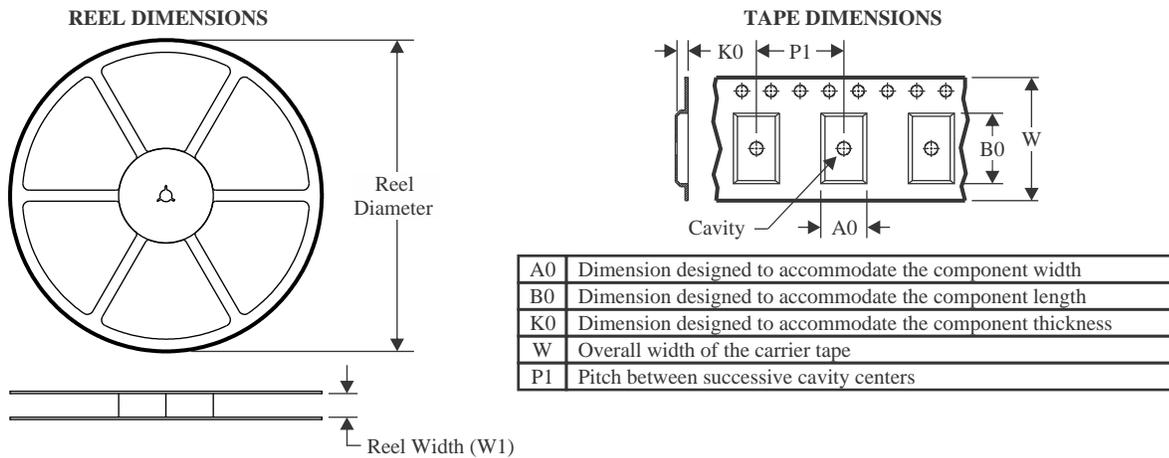
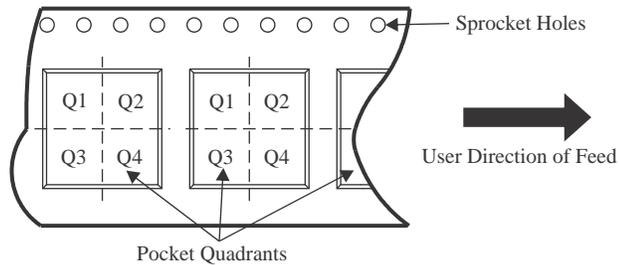
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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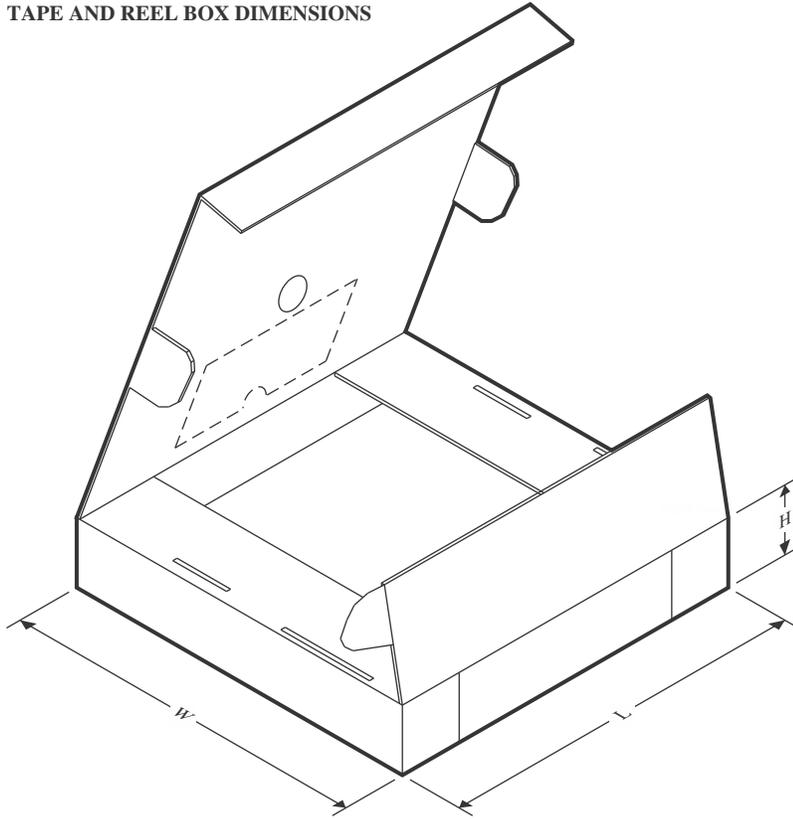
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

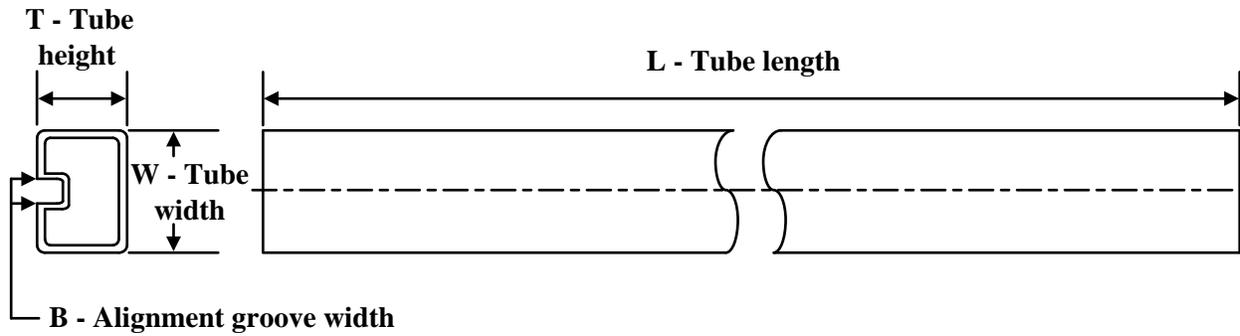
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC367DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC367PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC367DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC367PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

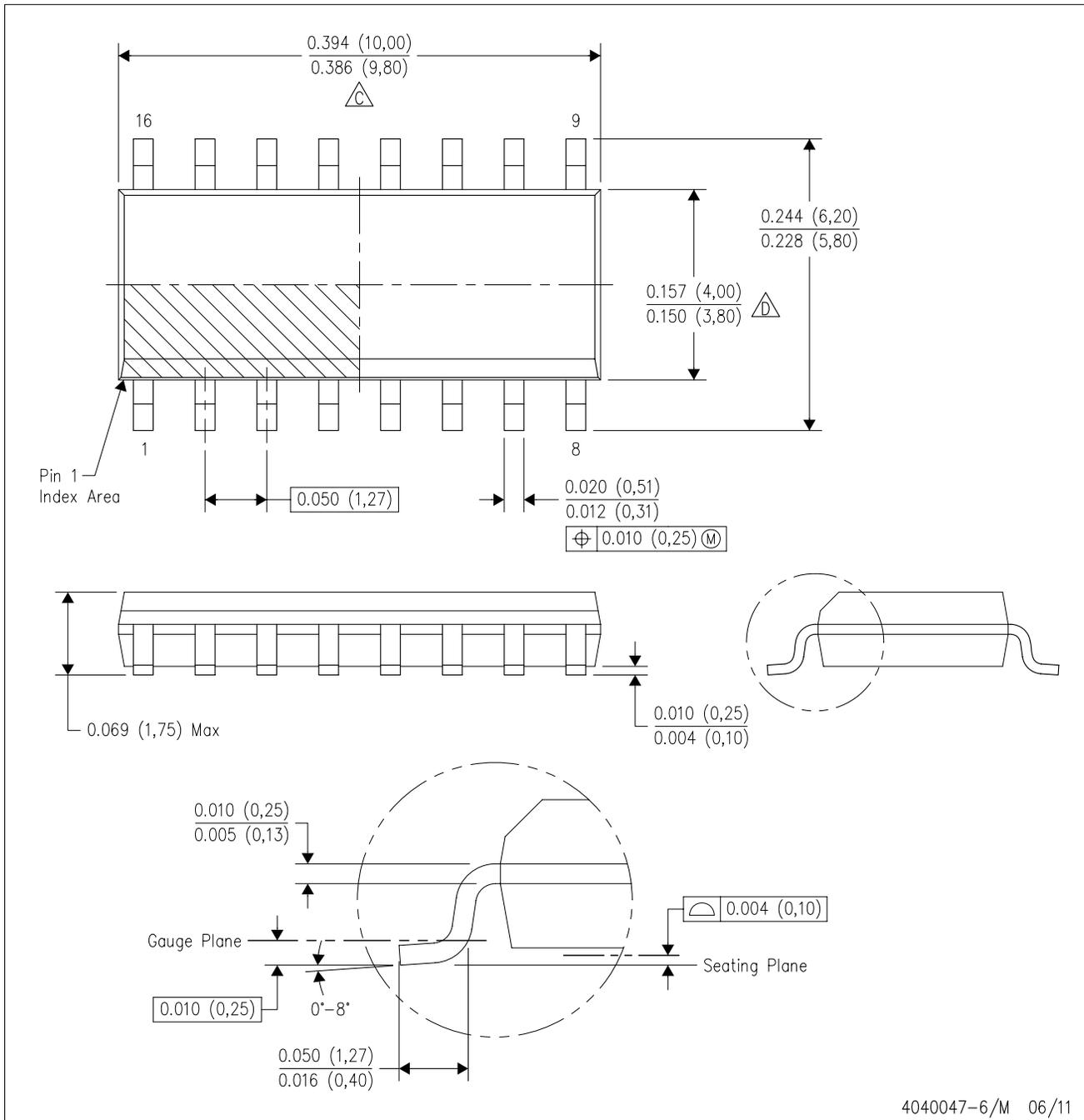
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC367D	D	SOIC	16	40	507	8	3940	4.32
SN74AHC367N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC367N	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

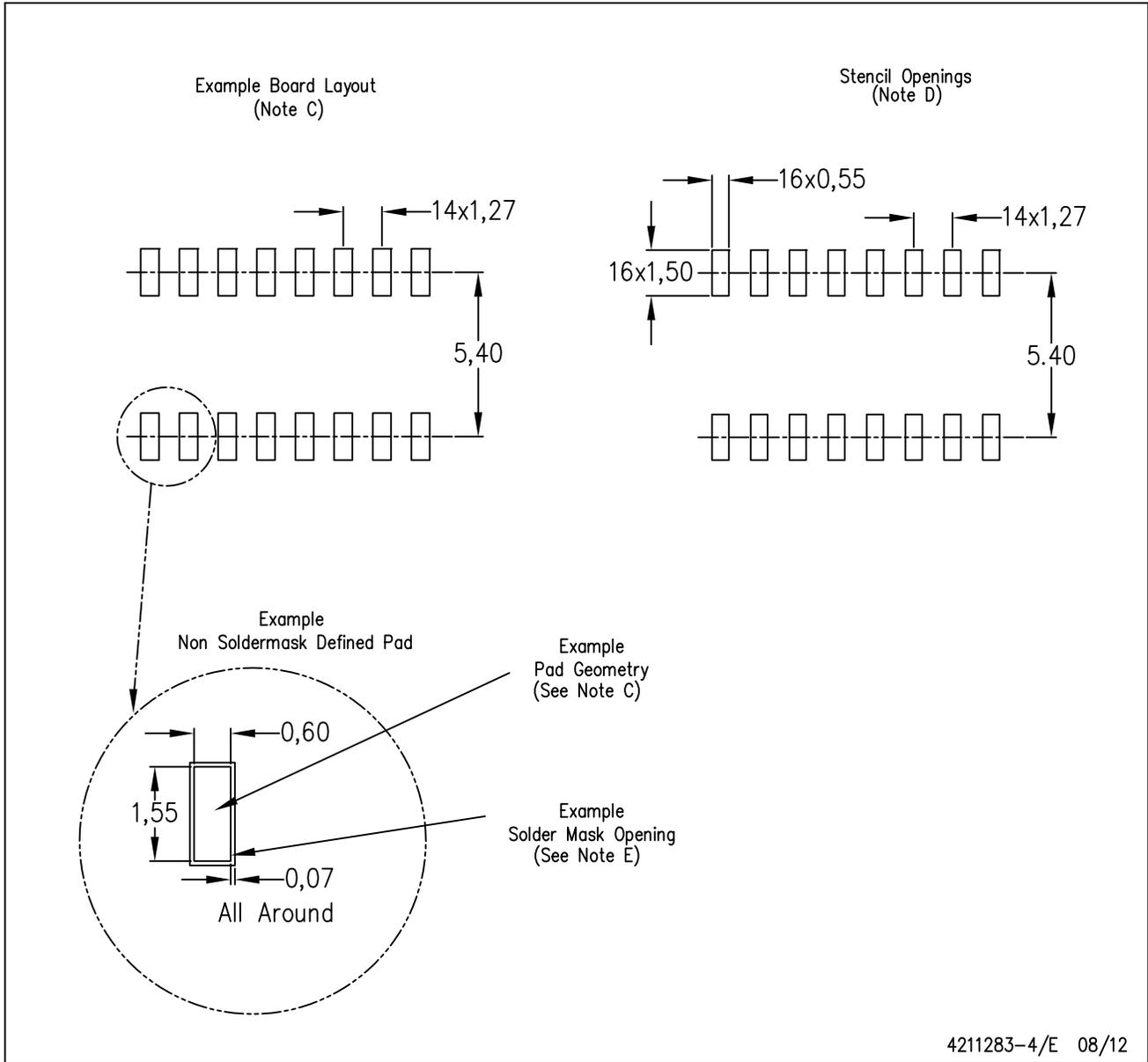
PLASTIC SMALL OUTLINE



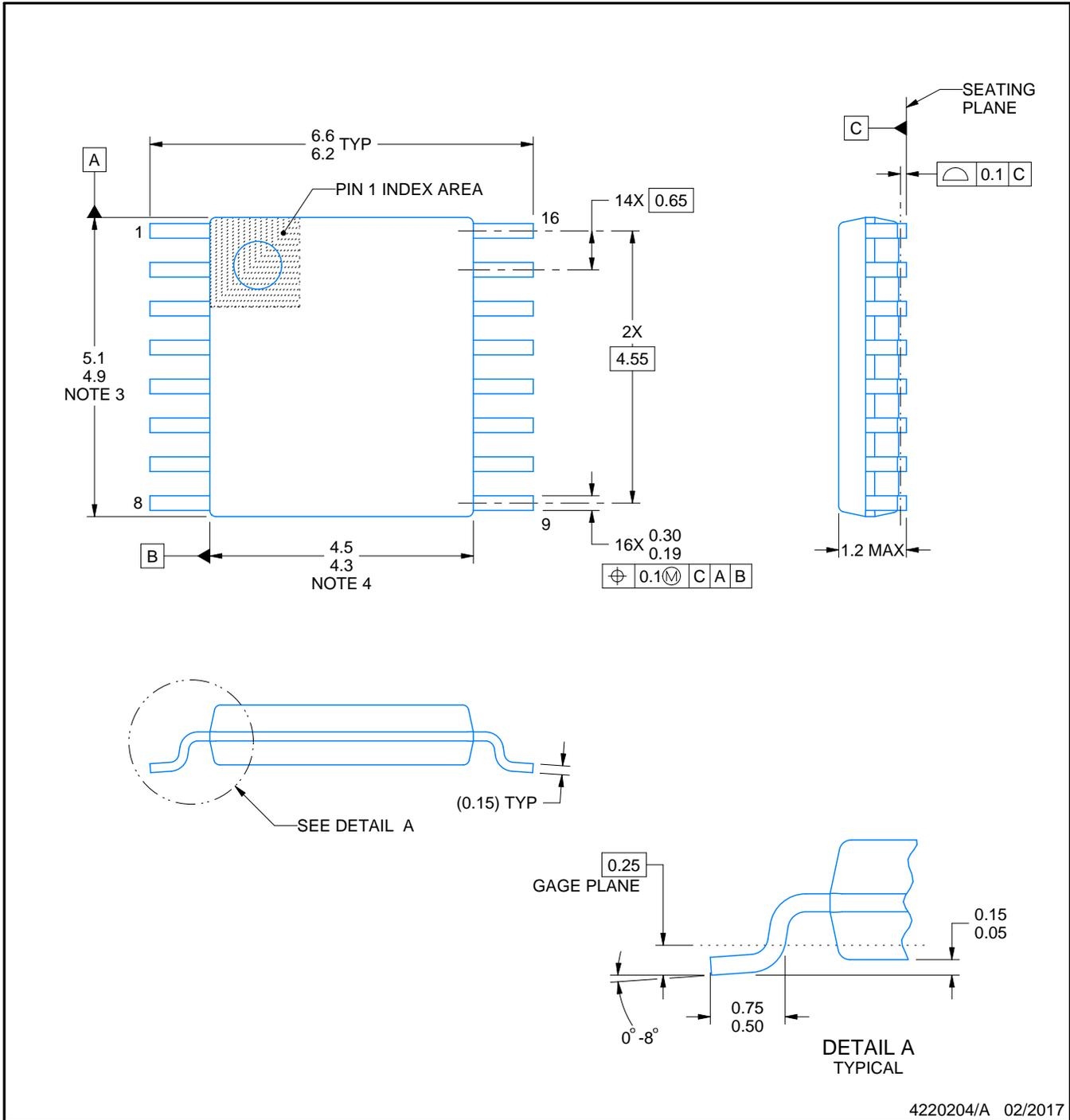
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

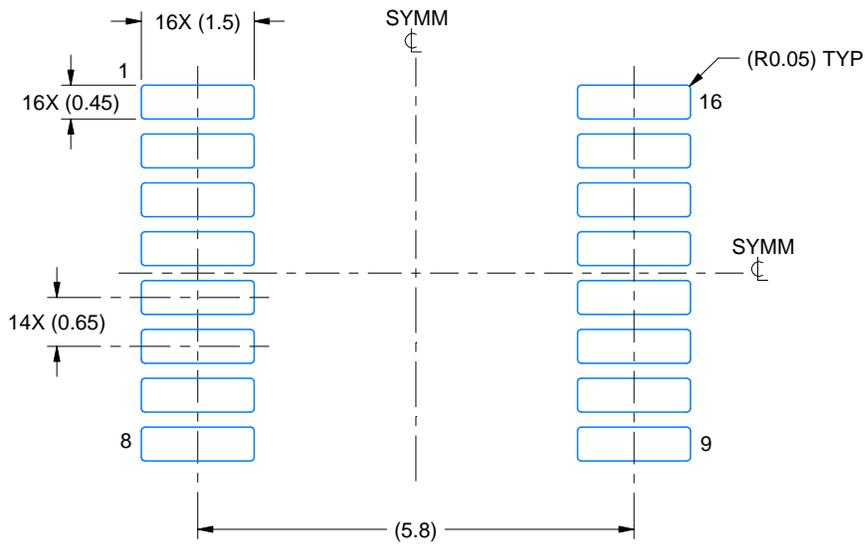
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

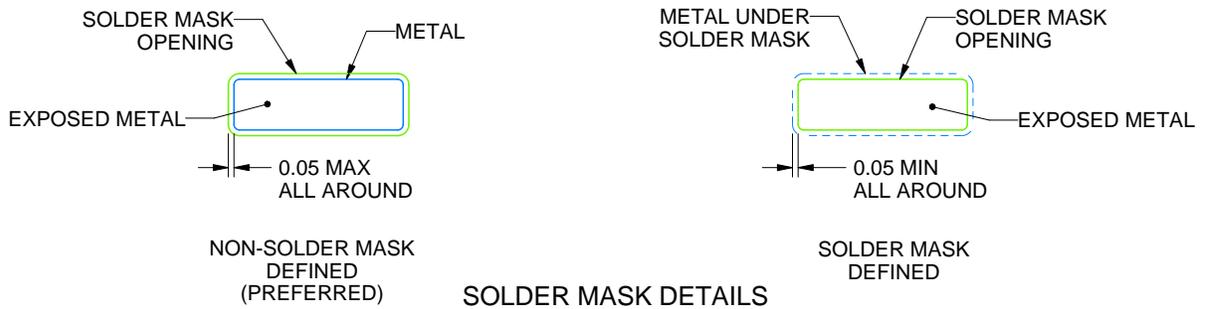
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

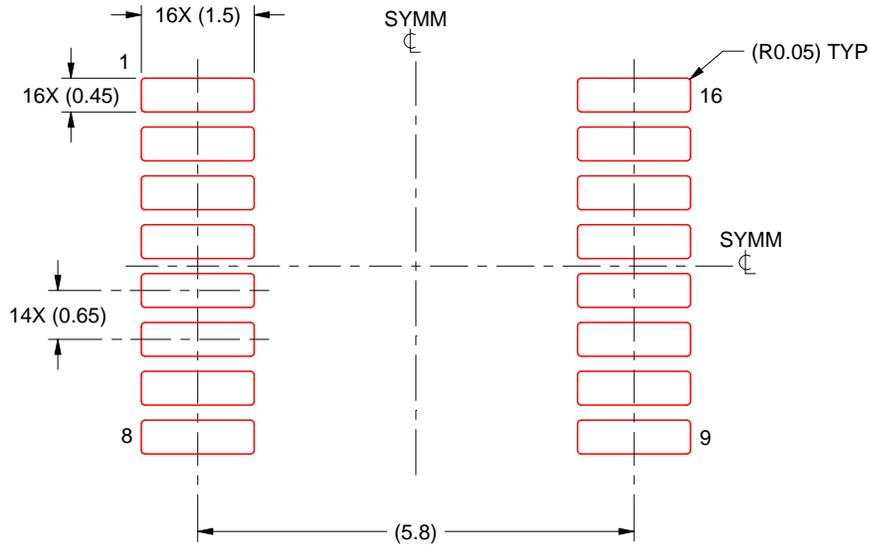
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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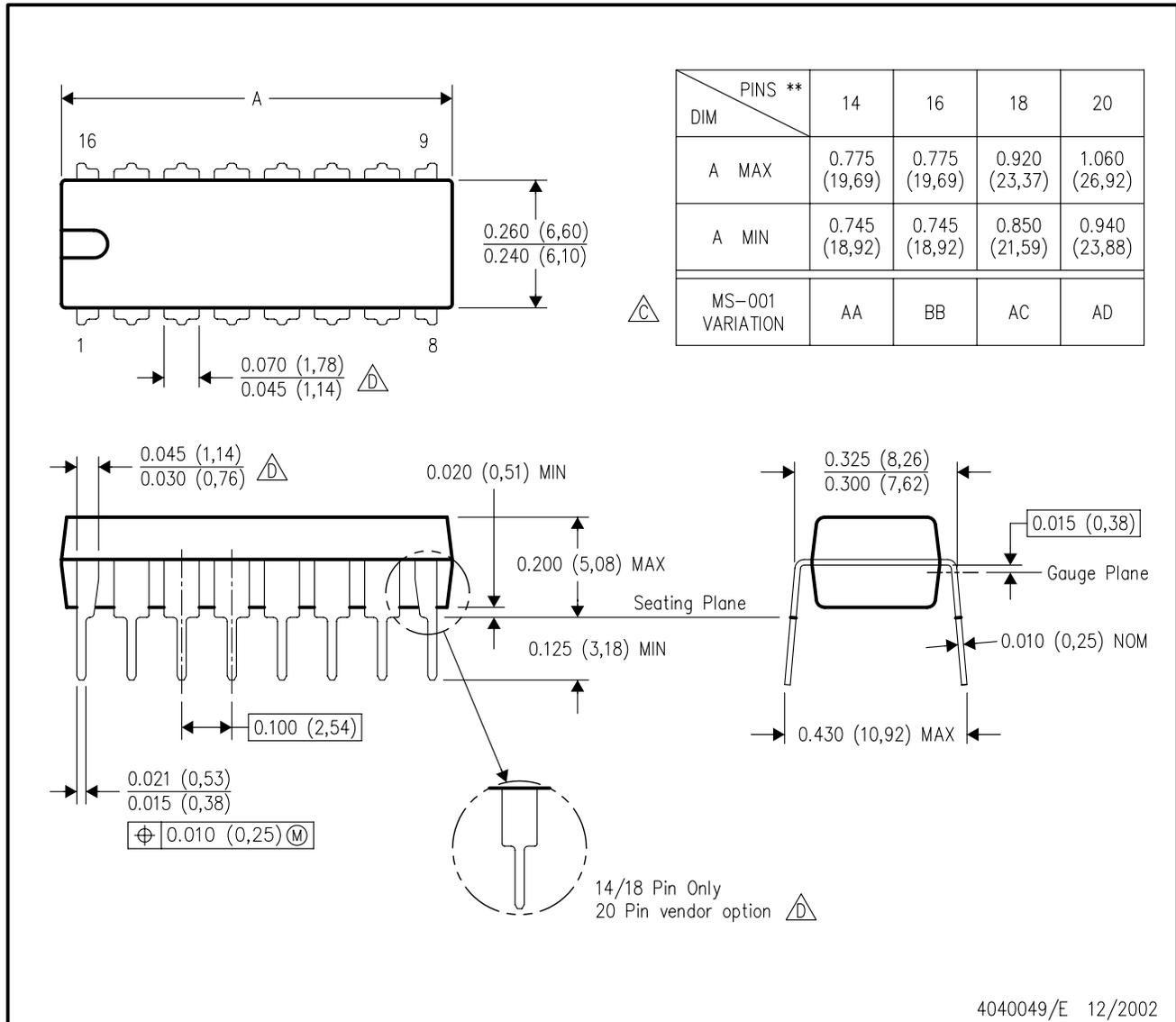
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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