

## FDS6982

## **Dual N-Channel, Notebook Power Supply MOSFET**

### **General Description**

This part is designed to replace two single SO-8 MOSFETs in synchronous DC:DC power supplies that provide the various peripheral voltage rails required in notebook computers and other battery powered electronic devices. FDS6982 contains two unique 30V, N-channel, logic level, PowerTrench® MOSFETs designed to maximize power conversion efficiency.

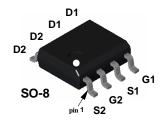
The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized for low conduction losses (less than  $20m\Omega$  at V  $_{GS}=4.5 V).$ 

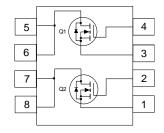
### **Applications**

- Battery powered synchronous DC:DC converters.
- Embedded DC:DC conversion.

### **Features**

- Q2: 8.6A, 30V.  $R_{DS(on)} = 0.015 \ \Omega \ @ \ V_{GS} = 10V$   $R_{DS(on)} = 0.020 \ \Omega \ @ \ V_{GS} = 4.5V$
- Q1: 6.3A, 30V.  $\begin{aligned} R_{DS(on)} &= 0.028 \; \Omega \; @ \; V_{GS} = 10V \\ R_{DS(on)} &= 0.035 \; \Omega \; @ \; V_{GS} = 4.5V \end{aligned}$
- Fast switching speed.
- $\bullet$  High performance trench technology for extremely low  $R_{\mbox{\tiny DS(ON)}}.$





### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Q2	Q1	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	30	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	<u>+</u> 20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	8.6	6.3	Α
	- Pulsed		30	20	
P <sub>D</sub>	Power Dissipation for Dual Operation		2	2	
	Power Dissipation for Single Operation	(Note 1a)	1.0	6	
		(Note 1b)	1		
		(Note 1c)	0.0	9	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range		-55 to	+150	∘C

### **Thermal Characteristics**

$R_{ heta^{JA}}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta^{JC}}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	∘C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity	
FDS6982	FDS6982	13"	12mm	2500 units	

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Off Cha	racteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	Q2 Q1	30 30			V
<u>ΔBV<sub>DSS</sub></u> ΔΤ <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$	Q2 Q1		27 26		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	All			1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	All			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V	All			-100	nA
$V_{GS(th)}$ $\Delta V_{GS(th)}$	Gate Threshold Voltage  Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$ $I_D = 250 \mu A$ , Referenced to 25°C	Q2 Q1 Q2	1	2.2 1.6	3	V mV/°(
On Cha	racteristics (Note 2)						
ΔT <sub>J</sub>	Temperature Coefficient		Q1		-4		mv/°0
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 8.6 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 8.6 \text{ A}, T_J = 125^{\circ}\text{C}$ $V_{GS} = 4.5 \text{ V}, I_D = 7.5 \text{ A}$	Q2		0.012 0.018 0.016	0.015 0.024 0.020	Ω
		$V_{GS} = 10 \text{ V}, I_D = 6.3 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 6.3 \text{ A}, T_J = 125^{\circ}\text{C}$ $V_{GS} = 4.5 \text{ V}, I_D = 5.6 \text{ A}$	Q1		0.021 0.038 0.028	0.028 0.047 0.035	Ω
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	Q2 Q1	30 20			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 8.6 \text{ A}$ $V_{DS} = 5 \text{ V}, I_{D} = 6.3 \text{ A}$	Q2 Q1		50 40		S
Dynami	c Characteristics						
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz	Q2 Q1		2085 760		pF
Coss	Output Capacitance		Q2 Q1		420 160		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1	Q2		160		pF

Electrical Characteristics (continued) T <sub>A</sub> = 25°C unless otherwise noted							
Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Switching Characteristics (Note 2)							
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, I_{D} = 1 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	Q2 Q1		15 10	27 18	ns
t <sub>r</sub>	Turn-On Rise Time		Q2 Q1		11 14	20 25	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		Q2 Q1		36 21	58 34	ns
t <sub>f</sub>	Turn-Off Fall Time		Q2 Q1		18 7	29 14	ns
Q <sub>g</sub>	Total Gate Charge	Q2 V <sub>DS</sub> = 15 V, I <sub>D</sub> = 8.6 A, V <sub>GS</sub> = 5 V	Q2 Q1		18.5 8.5	26 12	nC

**Drain-Source Diode Characteristics and Maximum Ratings** 

Q1

Diani-30uice Didue Characteristics and Maximum Natings							
Is	Maximum Continuous Drain-Source Diode Forward Current	Q2		1.3	Α		
		Q1		1.3			
$V_{SD}$	Drain-Source Diode Forward $V_{GS} = 0 \text{ V}, I_S = 1.3 \text{ A}$ (Note 2)	Q2	0.72	1.2	V		
	Voltage $V_{cs} = 0 \text{ V. } I_s = 1.3 \text{ A} \text{ (Note 2)}$	Q1	0.74	1.2	İ		

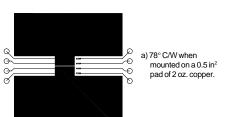
 $V_{DS} = 15 \text{ V}, I_{D} = 6.3 \text{ A}, V_{GS} = 5 \text{ V}$ 

#### Notes:

 $Q_{\text{gs}}$ 

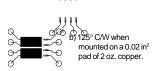
 $Q_{gd}$ 

 R<sub>BJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>BJC</sub> is guaranteed by design while R<sub>BCA</sub> is determined by the user's board design. Thermal rating based on independant single device opperation.



Gate-Source Charge

Gate-Drain Charge



Q2

Q1

Q2

Q1

7.3

2.4

6.2

3.1

nC

nC

c) 135° C/W when mounted on a minimum pad.

Scale 1: 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

## **Typical Characteristics: Q2**

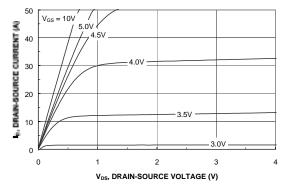


Figure 1. On-Region Characteristics.

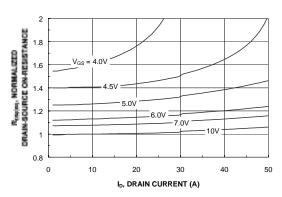


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

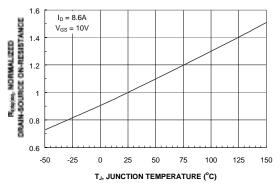


Figure 3. On-Resistance Variation with Temperature.

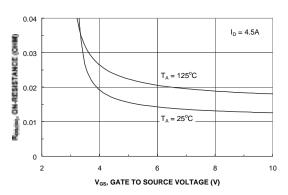


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

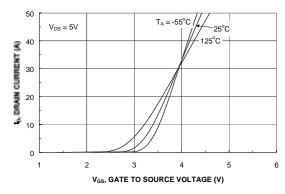


Figure 5. Transfer Characteristics.

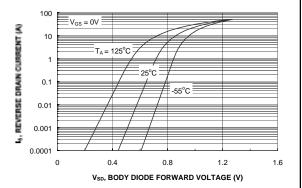


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# Typical Characteristics: Q2 (continued)

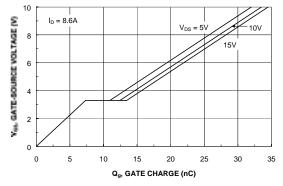


Figure 7. Gate-Charge Characteristics.

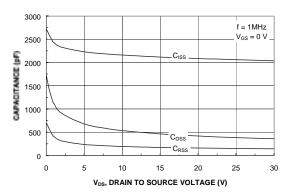


Figure 8. Capacitance Characteristics.

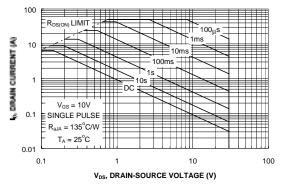


Figure 9. Maximum Safe Operating Area.

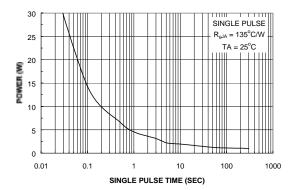


Figure 10. Single Pulse Maximum Power Dissipation.

## **Typical Characteristics: Q1**

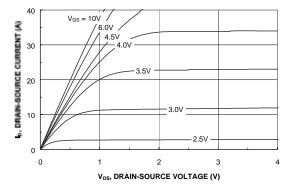


Figure 11. On-Region Characteristics.

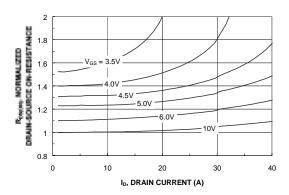


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

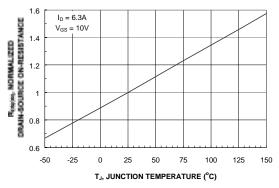


Figure 13. On-Resistance Variation with Temperature.

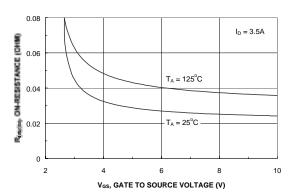


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

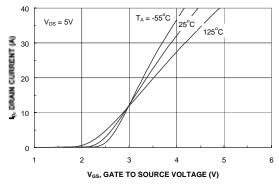


Figure 15. Transfer Characteristics.

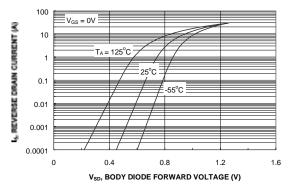


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

# Typical Characteristics: Q1 (continued)

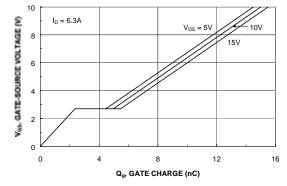


Figure 17. Gate-Charge Characteristics.

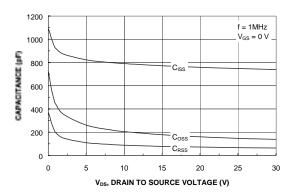


Figure 18. Capacitance Characteristics.

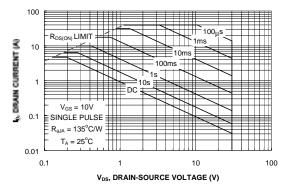


Figure 19. Maximum Safe Operating Area.

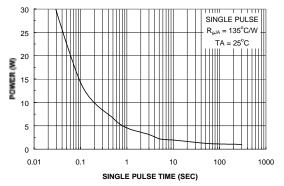


Figure 20. Single Pulse Maximum Power Dissipation.

# Typical Characteristics: Q1 & Q2 (continued)

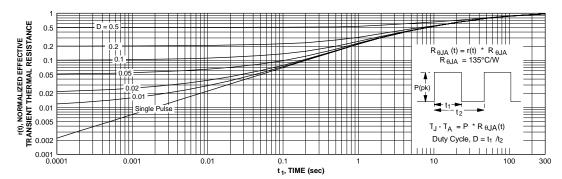


Figure 21. Transient Thermal Response Curve.

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