±15 kV ESD Protected, Dual RS-422 Transceiver

Data Sheet **ADM4168E**

FEATURES

- Dual RS-422 transceiver for
- ESD protection on bus input/output pins
  - ±15 kV HBM
  - ±8 kV IEC 61000-4-2, contact discharge
  - ±8 kV IEC 61000-4-2, air discharge
- Complies with TIA/EIA-422-B and ITU-T recommendation V.11
- Open circuit fail-safe
- Suitable for 5 V power supply applications
- Low supply current operation: 9 mA maximum
- Low driver output skew
- Receiver line input resistance: 30 kΩ typical
- Receiver common-mode range: −7 V to +7 V
- Power-up/power-down without glitches
- 16-lead TSSOP package
- Operating temperature range: −40°C to +85°C

APPLICATIONS

- RS-422 interfaces
- High data rate motor control
- Single-ended to differential signal conversion
- Point to point and multidrop transmission systems

FUNCTIONAL BLOCK DIAGRAM

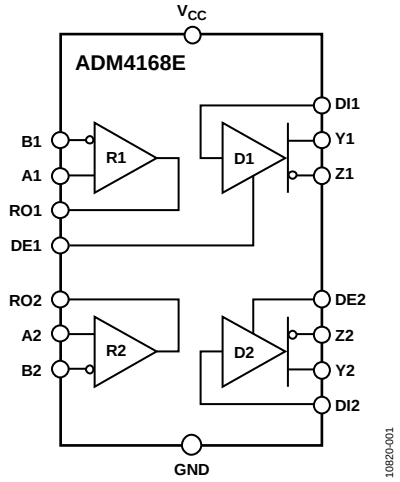

Figure 1.

GENERAL DESCRIPTION

The ADM4168E is a dual RS-422 transceiver suitable for high speed communication on point to point and multidrop transmission lines. The ADM4168E is designed for balanced transmission lines and complies with TIA/EIA-422-B.

The differential driver outputs and receiver inputs feature electrostatic discharge (ESD) circuitry that provides protection up to ±15 kV human body model (HBM) and ±8 kV IEC 61000-4-2 (contact and air discharge).

The ADM4168E operates from a single 5 V power supply. Excessive power dissipation caused by bus contention or output shorting is prevented by short-circuit protection circuitry. Short-circuit protection circuits limit the maximum output current to −150 mA during fault conditions.

The receivers of the ADM4168E contain a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM4168E is fully specified over the commercial and industrial temperature ranges and is available in a 16-lead TSSOP package.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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REVISION HISTORY

6/2019—Rev. A to Rev. B

Changes to Table 3 5
Changes to Thermal Resistance Section and Table 4 5
Changes to Figure 9 and Figure 10 8
Changes to Figure 13 9
Added Applications Information Section, Figure 17; Renumbered Sequentially, Figure 18, and Figure 19 11

9/2017—Rev. 0 to Rev. A

Changes to Features Section and General Description Section 1
Changes to Table 1 3
Added Maximum Data Rate Parameter, Table 2 4

9/2012—Revision 0: Initial Version

SPECIFICATIONS

4.5 V ≤ V_{CC} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = 5.0 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOW SUPPLY CURRENT						No load, drivers enabled
Total Package	I_{CC}		4	6	mA	Input voltage (V_I) = V_{CC} or GND
			5	9	mA	V_I = 2.4 V or 0.5 V[1]
DRIVER						
Differential Outputs (Y1, Z1, Y2, Z2 Pins)						
Input Clamp Voltage	V_{IK}			−1.5	V	I_I = −18 mA
Output Voltage High	V_{OH}	2.4	3.5		V	V_{IH} = 2 V, V_{IL} = 0.8 V, output high voltage (I_{OH}) = −20 mA
Output Voltage Low	V_{OL}		0.2	0.4	V	V_{IH} = 2 V, V_{IL} = 0.8 V, output low voltage (I_{OL}) = 20 mA
Differential Output Voltage						
No Load	$\|V_{OD1}\|$	2.0		6.0	V	I_O = 0 mA
Outputs Loaded[2]	$\|V_{OD2}\|$	2.0	3.7		V	Load resistance (R_L) = 100 Ω (see Figure 11)
Δ$\|V_{OD}\|$ for Complementary Output States	Δ$\|V_{OD}\|$			±0.4	V	R_L = 100 Ω (see Figure 11)
Common-Mode Output Voltage	V_{OC}			±3.0	V	R_L = 100 Ω (see Figure 11)
Δ$\|V_{OC}\|$ for Complementary Output States	Δ$\|V_{OC}\|$			±0.4	V	R_L = 100 Ω (see Figure 11)
Output Leakage Current	I_O			100	µA	DEx = 0 V, V_{CC} = 0 V or 5 V, output voltage (V_O) = 6 V
		−100			µA	DEx = 0 V, V_{CC} = 0 V or 5 V, V_O = −0.25 V
Output Current (Short Circuit)[3]	I_{OS}	−30		−150	mA	V_O = V_{CC} or GND
Input Capacitance	C_I		6		pF	
Logic Inputs (DIx, DEx Pins)						
Input Voltage High	V_{IH}	2.0			V	
Input Voltage Low	V_{IL}			0.8	V	
Input Current High	I_{IH}			1	µA	V_I = V_{CC} or V_{IH}
Input Current Low	I_{IL}			−1	µA	V_I = GND or V_{IL}
RECEIVER						
Differential Inputs (A1, B1, A2, B2 Pins)						
Differential Input Threshold Voltage[2]	V_{TH}	−200		+200	mV	
Input Voltage Hysteresis	V_{HYS}		60		mV	
Input Current	I_I			1.5	mA	V_I = 7 V, other input at 0 V
				−2.5	mA	V_I = −7 V, other input at 0 V
Line Input Resistance	R_{IN}	12	30		kΩ	V_{IC}[4] = −7 V to +7 V, other input at 0 V
Logic Outputs (RO1, RO2 Pins)						
Output Voltage High	V_{OH}	3.8	4.2		V	V_{ID}[5] = 200 mV, I_{OH} = −6 mA
Output Voltage Low	V_{OL}		0.1	0.3	V	V_{ID} = −200 mV, I_{OL} = 6 mA

[1] Measured per input with other inputs at V_{CC} or GND.
[2] For exact conditions, see TIA/EIA-422-B.
[3] No more than one output shorted at any time, with the duration of the short not to exceed 1 second.
[4] V_{IC} is the receiver input common mode voltage.
[5] V_{ID} is the receiver input differential voltage.

TIMING SPECIFICATIONS

4.5 V ≤ V_{CC} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = 5.0 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate	D_{RATE}	30			Mbps	R1, R2 = 50 Ω; R3 = 500 Ω; C1, C2, C3 = 40 pF
Propagation Delay	t_{DPLH}, t_{DPHL}		8	16	ns	S1 open (see Figure 12 and Figure 13)
Driver Output Skew	t_{SK}		1.5	4	ns	S1 open (see Figure 12 and Figure 13)
Rise Time/Fall Time	t_{DR}, t_{DF}		5	10	ns	S1 open (see Figure 12 and Figure 13)
Enable Time	t_{ZH}, t_{ZL}		10	19	ns	S1 closed (see Figure 13 and Figure 14)
Disable Time	t_{HZ}, t_{LZ}		7	16	ns	S1 closed (see Figure 13 and Figure 14)
RECEIVER[1]						
Propagation Delay	t_{RPLH}, t_{RPHL}	9	15	27	ns	Load capacitance (C_L) = 50 pF (see Figure 15 and Figure 16)
Transition Time	t_{TLH}, t_{THL}		4	9	ns	V_{IC} = 0 V, C_L = 50 pF (see Figure 15 and Figure 16)

[1] Measured per input with other inputs at V_{CC} or GND.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{CC}	−0.3 V to +7 V
Digital Input Voltage (DE1, DE2)	−0.3 V to +7 V
Driver Input Voltage (DI1, DI2)	−0.3 V to +7 V
Receiver Output Voltage (RO1, RO2)	−0.3 V to V_{CC} + 0.3 V
Driver Output Voltage (Y1, Z1, Y2, Z2)	−0.3 V to +7 V
Receiver Input Voltage (A1, B1, A2, B2)	−14 V to +14 V
Digital Input/Output (I/O) (DI1, DI2, DE1, DE2, RO1, RO2) Voltage Transient to GND	−2 V to +8 V for 10 ms
Driver Output (Y1, Z1, Y2, Z2) Voltage Transient to GND	−2 V to +8 V for 10 ms
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
ESD Protection on Ax, Bx, Yx, and Zx	
HBM	±15 kV
IEC 61000-4-2, Contact Discharge	±8 kV
IEC 61000-4-2, Air Discharge	±8 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
RU-16	113	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

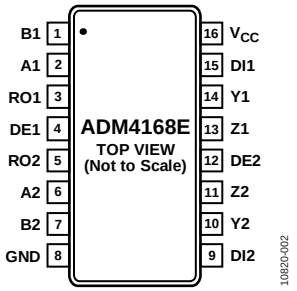


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	Inverting Receiver Input B, Transceiver 1.
2	A1	Noninverting Receiver Input A, Transceiver 1.
3	RO1	Receiver Output, Transceiver 1.
4	DE1	Driver Output Enable, Transceiver 1. A logic high enables the differential driver outputs, Y1 and Z1; a logic low places the differential driver outputs in a high impedance state.
5	RO2	Receiver Output, Transceiver 2.
6	A2	Noninverting Receiver Input A, Transceiver 2.
7	B2	Inverting Receiver Input B, Transceiver 2.
8	GND	Ground.
9	DI2	Driver Input, Transceiver 2. When the driver is enabled, a logic low on DI2 forces Y2 low and Z2 high, whereas a logic high on DI2 forces Y2 high and Z2 low.
10	Y2	Noninverting Driver Output Y, Transceiver 2.
11	Z2	Inverting Driver Output Z, Transceiver 2.
12	DE2	Driver Output Enable, Transceiver 2. A logic high enables the differential driver outputs, Y2 and Z2; a logic low places the differential driver outputs in a high impedance state.
13	Z1	Inverting Driver Output Z, Transceiver 1.
14	Y1	Noninverting Driver Output Y, Transceiver 1.
15	DI1	Driver Input, Transceiver 1. When the driver is enabled, a logic low on DI1 forces Y1 low and Z1 high, whereas a logic high on DI1 forces Y1 high and Z1 low.
16	V_{CC}	Power Supply (5 V ± 10%).

TYPICAL PERFORMANCE CHARACTERISTICS

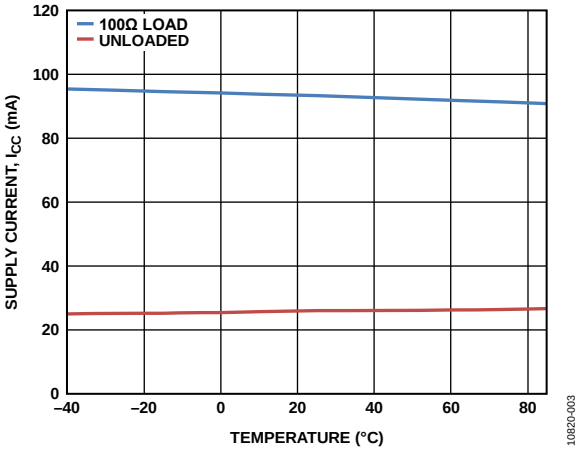


Figure 3. Supply Current vs. Temperature, Data Rate = 10 Mbps

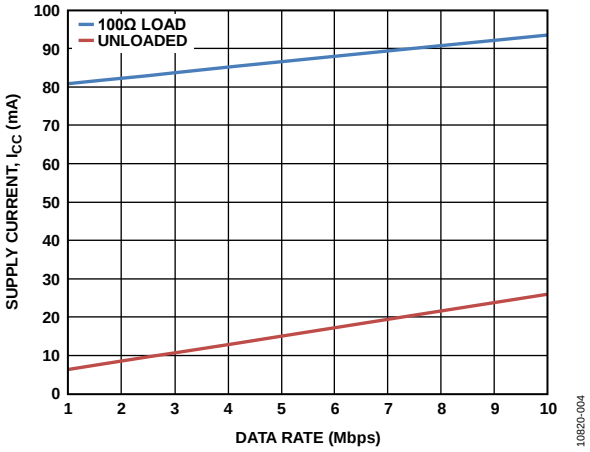


Figure 6. Supply Current vs. Data Rate

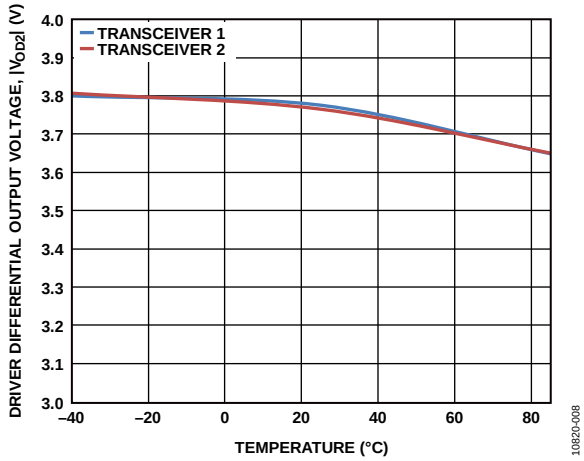


Figure 4. Driver Differential Output Voltage vs. Temperature

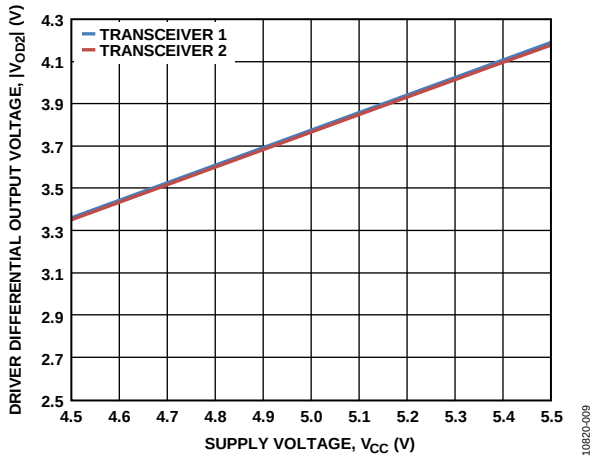


Figure 7. Driver Differential Output Voltage vs. Supply Voltage

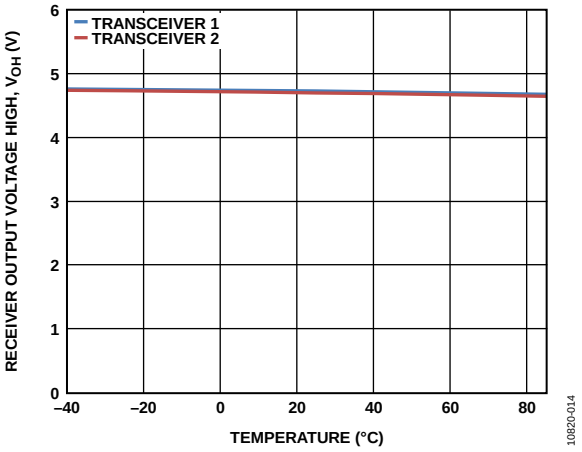


Figure 5. Receiver Output Voltage High vs. Temperature

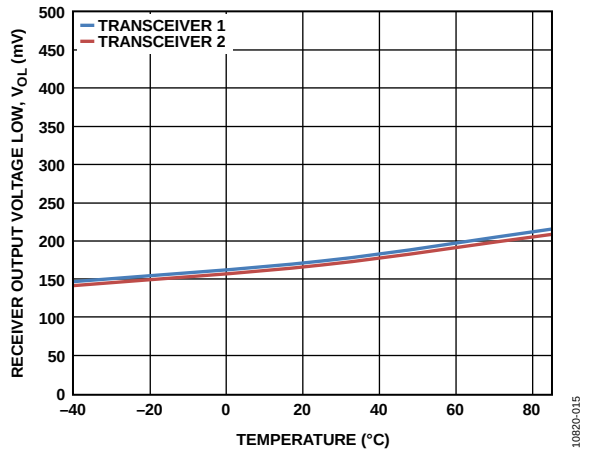


Figure 8. Receiver Output Voltage Low vs. Temperature

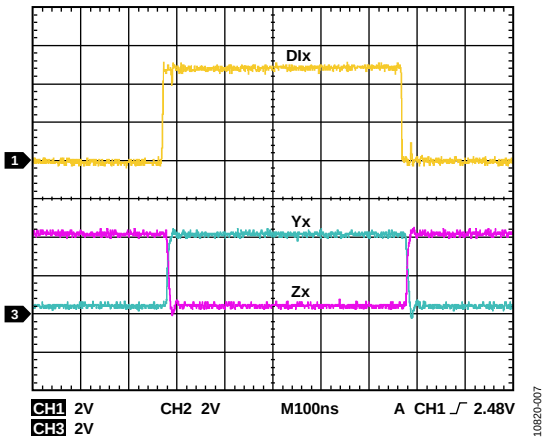


Figure 9. Driver Output

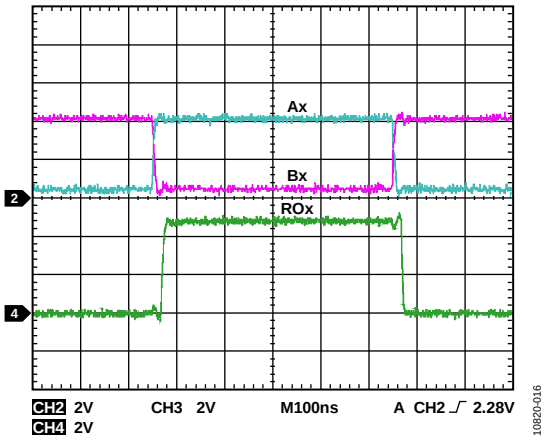


Figure 10. Receiver Output

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

DRIVER MEASUREMENTS

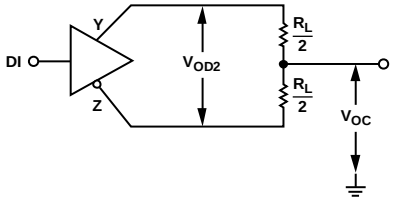
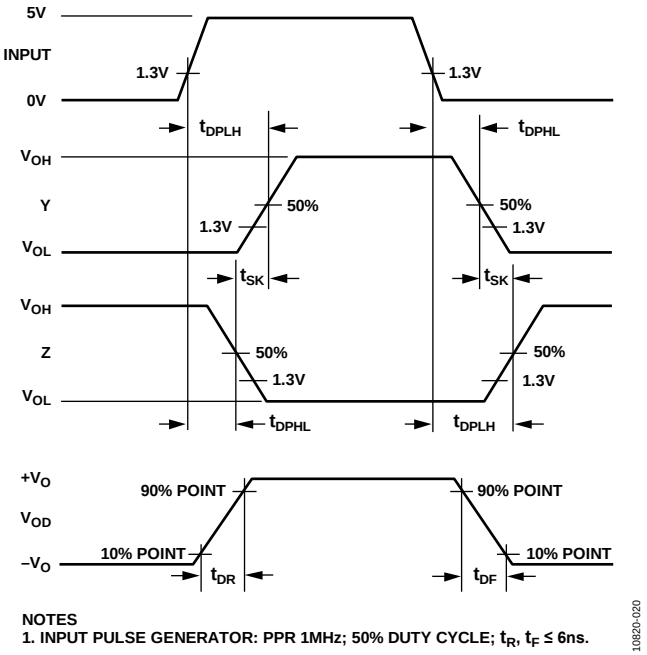


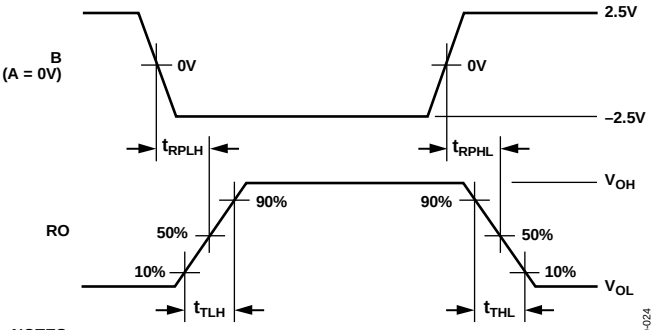
Figure 11. Driver Voltage Measurements



NOTES
1. INPUT PULSE GENERATOR: PPR 1MHz; 50% DUTY CYCLE; t_R, t_F ≤ 6ns.

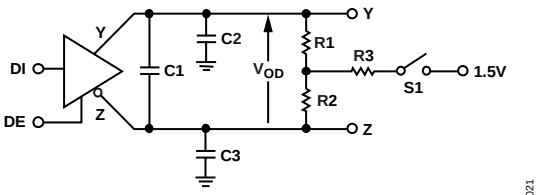
Figure 12. Driver Propagation Delay and Rise/Fall Timing

RECEIVER MEASUREMENTS



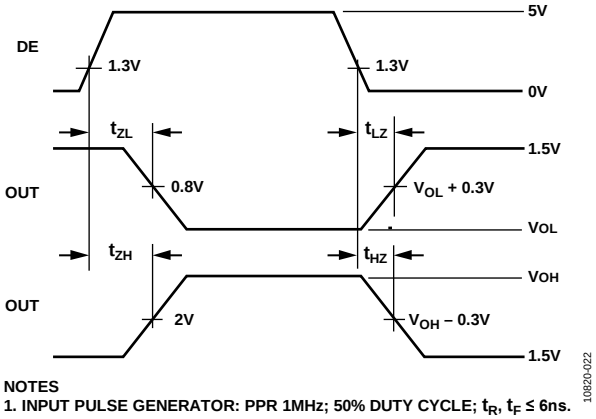
NOTES
1. INPUT PULSE GENERATOR: PPR 1MHz; 50% DUTY CYCLE; t_R, t_F ≤ 6ns.

Figure 15. Receiver Propagation Delay and Transition Timing



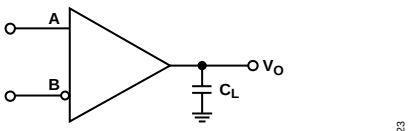
NOTES
1. C1, C2, C3 INCLUDE PROBE/INSTRUMENT CAPACITANCE.

Figure 13. Driver Timing Circuit



NOTES
1. INPUT PULSE GENERATOR: PPR 1MHz; 50% DUTY CYCLE; t_R, t_F ≤ 6ns.

Figure 14. Driver Enable/Disable Timing



NOTES
1. C_L INCLUDES PROBE/INSTRUMENT CAPACITANCE.

Figure 16. Receiver Timing Circuit

THEORY OF OPERATION

The ADM4168E is a dual RS-422 transceiver that operates from a single 5 V ± 10% power supply. The ADM4168E is intended for balanced data transmission and complies with TIA/EIA-422-B and ITU-T recommendation V.11. Each device contains two differential line drivers and two differential line receivers and is suitable for full duplex data transmission.

The receivers contain a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM4168E features a low propagation delay, ensuring maximum baud rate operation. The balanced driver ensures distortion free transmission.

Another important specification is a measure of the skew between the complementary outputs. Low skew enhances the noise immunity of the system and decreases the amount of electromagnetic interference (EMI).

TRUTH TABLES

Table 6. Abbreviations in Truth Tables

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant
Z	High impedance (off)

Table 7. Transmitting (Each Driver)

Inputs		Outputs	
DEx	**DIx**	**Zx**	**Yx**
H	H	L	H
H	L	H	L
L	X	Z	Z

Table 8. Receiving (Each Receiver)

Inputs	Output
Ax – Bx	**ROx**
≥ +0.2 V	H
≤ −0.2 V	L
−0.2 V < A − B < +0.2 V	I
Inputs open	H

APPLICATIONS INFORMATION

The ADM4168E dual RS-422 transceiver was tested in a two node network over 100 meters of Category 5e T568B shielded cable, with a 100 Ω termination resistor inserted at the receiving ADM4168E. Both of the ADM4168E devices are powered at 5 V V_{CC}. The transmitting ADM4168E sends data at 20 Mbps to the receiving ADM4168E. Figure 17 shows an example test setup.

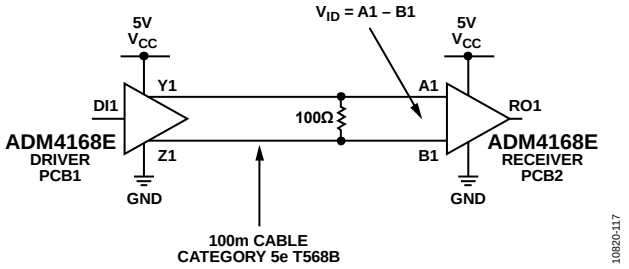


Figure 17. Test Setup for the ADM4168E Quality of Signal

Figure 18 and Figure 19 show quality of signal (eye pattern) oscilloscope plots for data transmission and receive quality using pseudo random binary sequence Base 7 (PRBS-7) and clock data patterns, respectively. Figure 18 and Figure 19 show the DI1 signal measured at the transmitting ADM4168E, the input differential voltage at the receiving ADM4168E (math A1-B1 signal), and the receiver output RO1 at the receiving ADM4168E.

Signal attenuation due to adding 100 meters of cabling does not lead to data errors at the RO1 output at the receiving node. The eye diagrams in Figure 18 and Figure 19 show some distortion due to cable effects; however, this does not lead to data errors on the RO1 output.

Figure 18 with PRBS-7 is representative of RS-422 data channels in a motor control encoder application. Figure 19 shows an RS-422 clock data, also commonly found in a motor control encoder interface.

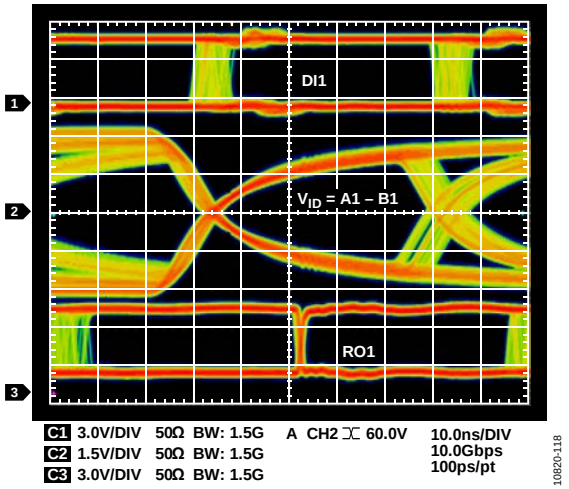


Figure 18. ADM4168E Quality of Signal Eye Diagram for PRBS-7

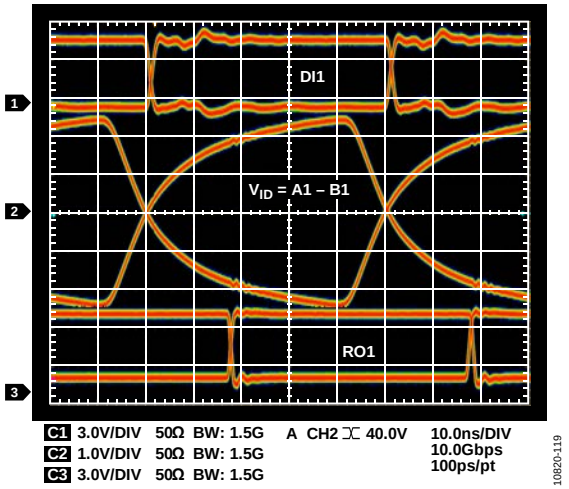


Figure 19. ADM4168E Quality of Signal Eye Diagram for Clock Data

OUTLINE DIMENSIONS

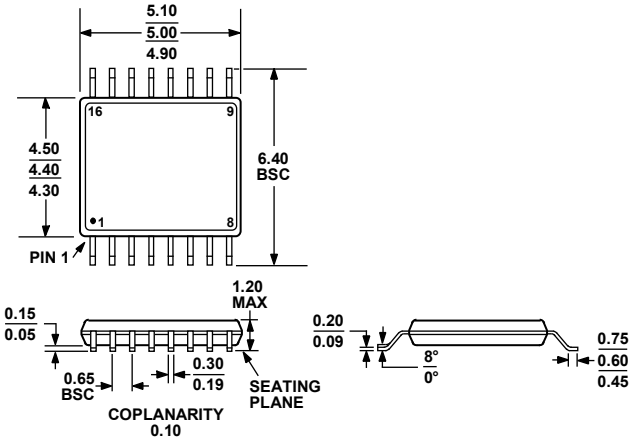


Figure 20. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM4168EBRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM4168EBRUZ-RL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
EVAL-ADM4168EEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D10820-0-6/19(B)