Eterna™ Board Specific Configuration Guide

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About This Guide

This document describes the use of the Eterna Board Specific Configuration application, FuseTable.exe, including the effects of the individual settings.

Audience

This document is intended for system developers, hardware designers, and software developers.

Related Documents

The following related documents are available:

Eterna Integration Guide

Eterna Board Serial Programmer Guide

Conventions and Terminology

This guide uses the following text conventions:

- `Computer type` indicates information that you enter, such as a URL.
- **Bold type** indicates buttons, fields, and menu commands.
- *Italic type* is used to introduce a new term.
- **Note:** Notes provide more detailed information about concepts.
- **Caution:** Cautions advise about actions that might result in loss of data.
- **Warning:** Warnings advise about actions that might cause physical harm to the hardware or your person.

Revision History

Revision	Date	Description
040-0109 rev 1	2/9/2012	Initial Release
040-0109 rev 2	4/20/2012	Cleaned up references
040-0109 rev 3	7/18/2012	Added RADIO_INHIBIT and SLEEPn fields
040-0109 rev 4	8/17/2012	Editorial changes
040-0109 rev 5	5/6/2012	Added documentation of BSP parameter support for 100 mote IP Manager products.
040-0109 rev 6	10/24/2012	Document formatting
040-0109 rev 7	9/24/2015	Addendum: Fuse Table and 20MHz crystal change

1 Getting Started

Installation

Note: *Microsoft Visual C++ 2008 SP1 Redistributable Package* must be installed on your computer prior to running the FuseTable utility. This package may be downloaded directly from Microsoft website.

Place the FuseTable.zip file into an empty directory of your choice (e.g. "\Program files\FuseTable") and extract the contents in place using Windows extract utility. When the extraction completes you should have several files, including FuseTable.exe. For convenience, you can place a shortcut to this executable onto your Desktop.

Invoke

Double click on FuseTable.exe.

Menu Options

Once invoked the top of the application window should appear as:

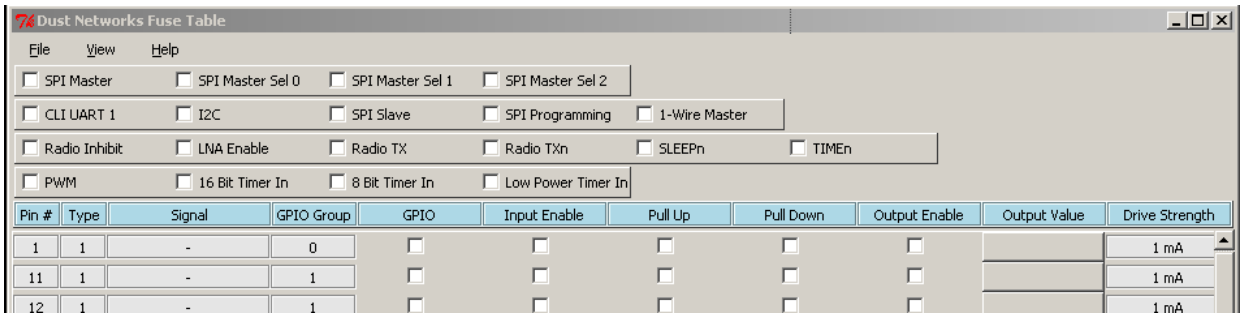


Figure 1 FuseTable.exe GUI after startup

The GUI is divided into two windows, the first window providing hardware configuration of IOs and the second window providing board support parameters. Move between the windows via `View -> Board Support Parameters` and `View -> IO Configuration`.

2 IO Configurations

Usage

The IO Configuration Window is divided into two segments. The upper segment shown in Figure 2, provides a method for configuring IO based upon the desired functions, such as SPI Master or I2C. When selecting the External Bus option this will also simultaneously disable CLI UART 0 and enable CLI UART 1 and is the only necessary configuration for External Bus support.

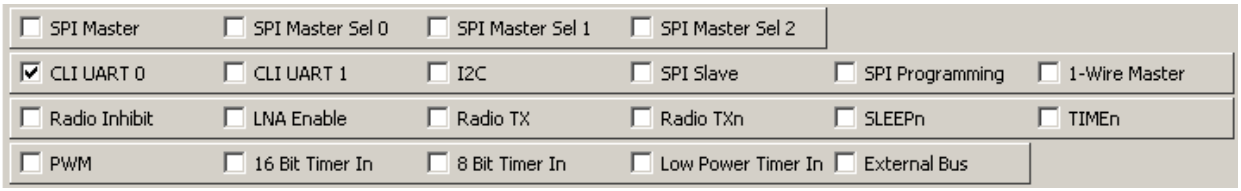


Figure 2 IO Configuration GUI Upper Segment

The lower segment shown in Figure 3, provides a method for configuring individual IO as GPIO and parameters, such as pull up/down, output enable and drive strength.

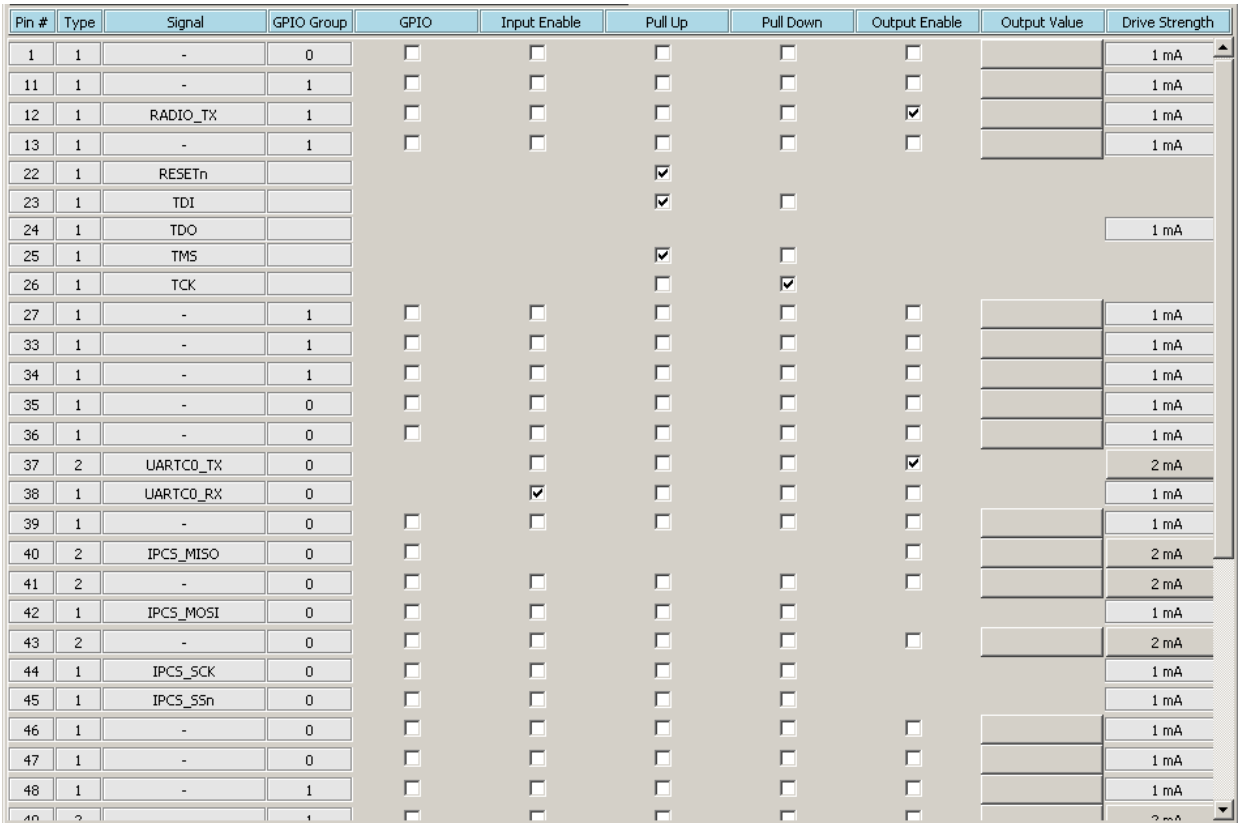


Figure 3 IO Configuration GUI Upper Segment

Pin Functions

Pin functions are selected by clicking on the check box. Selecting a Pin function results in the following:

1) Corresponding pin(s) in the IO table are labeled the “Signal” column by their function.

2) The “Input Enable”, “Pull Up”, “Pull Down” and “Output Enable” columns are populated to their default values

3) Corresponding pin(s) are locked to the selected pin function – they can not be reassigned to another function should the user select an option that would result in contention for the pin(s)

Pin functions correspond functions described in the Eterna product data sheet. See the product data sheet for signal functions and AC timing parameters.

Individual pins are assigned GPIO functionality by selecting the GPIO check boxes in the lower segment of the IO Configuration window.

IO Parameters

IO parameters are selected by clicking on the check box(es) or button(s) in the lower segment of the IO Configuration Window. Some IO parameters are fixed by the pin function selections made in the upper segment of the IO Configuration window. Per pin the settable IO parameters include:

Input Enable	IO’s input enable. Input leakage current will increase substantially when IO’s that are not actively driven whose input enable is set.
Pull Up	Enable the IO’s internal pull up resistor. The internal pull up and pull down resistors can not be simultaneously enabled.
Pull Down	Enable the IO’s internal pull down resistor. The internal pull up and pull down resistors can not be simultaneously enabled.
Output Enable	IO’s output enable.
Output Value	Output Value can only be set for IOs set at GPIO, other pin functions have defined values for their inactive state and are controlled via their controlling modules in the design.
Drive Strength	Only those IO’s with an active button shown in the Drive Strength column can be modified from their default value. It is strongly suggested that the minimum drive strength be selected unless there is an understood need for a higher drive strength.

Timing

IO Pin Functions and Parameters result in configuration of the IO when Eterna exits from power on reset.

3 Board Support Parameters

Usage

The Board Support Parameters Window can be viewed via `View -> Board Support Parameters` from the main menu and should appear similarly to Figure 4. The Board support parameters appear as list of check boxes and either drop down selection boxes or entry fields, one per line. To include a Board Support Parameter, BSP, select the check box labeled “Include”, “Force” or “Enable” and either make an entry in the entry field, by selecting the “Set” button, or select an item via the scroll down options. Regardless of the value in an entry field or selection box, a BSP will not be included in the resulting configuration file unless the checkbox is selected. Most of BSP parameters are not required for the majority of designs. Required fields will be highlighted in **bold**. Board Support Parameters provide switches to control software configuration of the device that are best served via flash configuration versus configuration over either the API or CLI interfaces.

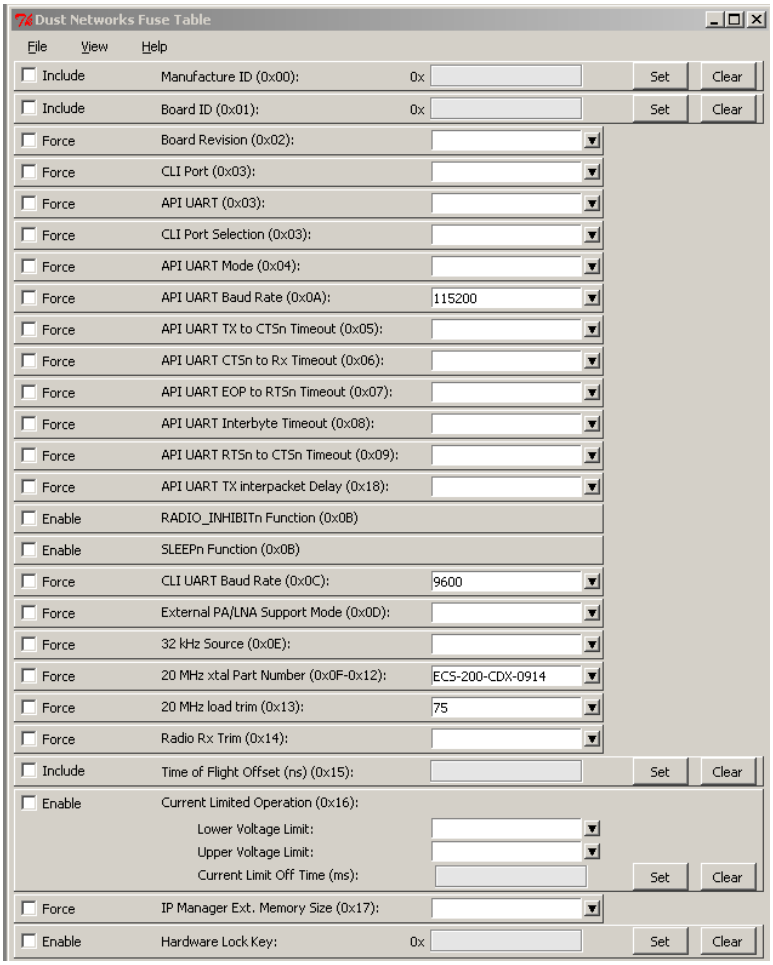


Figure 4 BSP Configuration Window

Parameters

The following parameters are listed in the order they appear on the display. Required Fields appear in bold.

Manufacture ID (0x00)	The Manufacturing ID is a 16-bit unique identifier for each manufacturer and allows the ability to provide targeted software based upon the combination of Manufacture ID, Board ID and Board Revision. Please contact your sales representative to obtain a Manufacturing ID for your organization if you do not currently have one.
Board ID (0x01)	The Board ID is a 16-bit unique identifier for each printed circuit board incorporating Eterna produced by a given manufacturer and allows the ability to provide targeted software based upon the combination of Manufacture ID, Board ID and Board Revision. Manufacturers should manage their own list of Board IDs.
Board Revision (0x02)	The Board Revision is a 8-bit unsigned integer for tracking the revision of each PCB design. The board revision allows the ability to provide targeted software based upon the combination of Manufacture ID, Board ID and Board Revision. Manufacturers should manage their own list of Board IDs.
CLI Port (0x03)	The CLI Port parameter allows for the disabling of the CLI Port. Use of this configuration is not recommended.
API UART (0x03)	The API UART parameter allows for the disabling of the API UART Port. Use of this configuration is not recommended.
CLI Port Selection (0x03)	The CLI Port parameter allows for switching the CLI Port Location. This is a test mode for Dust Networks internal use.
API UART Mode (0x04)	The API UART Mode determines the operating mode for the UART. This should be selected according to the modes defined in the Eterna datasheet.
API UART TX to CTSn Timeout (0x05)	This parameter corresponds to the $t_{TX\ to\ TX\_CTSn}$ timing parameter in the Eterna datasheet. Use of this configuration is not recommended. Absence of setting this field results in the default setting from the Eterna datasheet.
API UART CTSn to Rx Timeout (0x06)	This parameter corresponds to the $t_{CTSn\ to\ RX}$ timing parameter in the Eterna datasheet. Use of this configuration is not recommended. Absence of setting this field results in the default setting from the Eterna datasheet.
API UART EOP to RTSn Timeout (0x07)	This parameter corresponds to the $t_{EOP\ to\ TX\_CTSn}$ timing parameter in the Eterna datasheet. Use of this configuration is not recommended. Absence of setting this field results in the default setting from the Eterna datasheet.

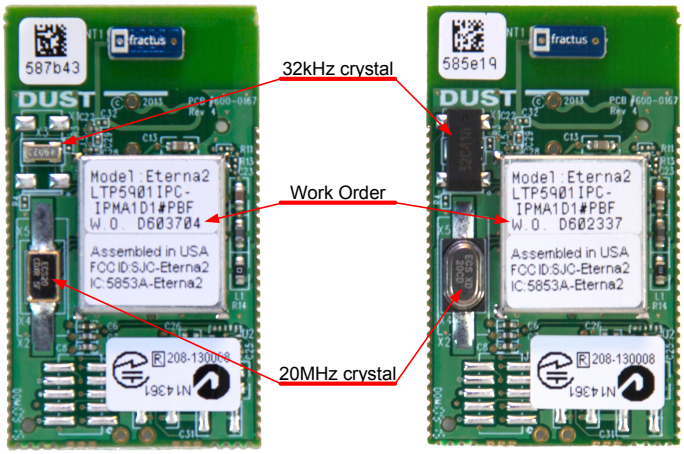
API UART Interbyte Timeout (0x08)	This parameter corresponds to the $t_{RX\ INTERBYTE}$ timing parameter in the Eterna datasheet. Use of this configuration is not recommended. Absence of setting this field results in the default setting from the Eterna datasheet.
API UART RTSn to CTSn Timeout (0x09)	This parameter corresponds to the $t_{RTSn\ to\ TX\_CTSn}$ timing parameter in the Eterna datasheet. Use of this configuration is not recommended. Absence of setting this field results in the default setting from the Eterna datasheet.
API UART Baud Rate (0x0A)	The baud rate for the API UART interface. Supported values are defined in the Eterna datasheet. Absence of setting this field results in the default setting from the Eterna datasheet.
RADIO_INHIBIT Function (0x0B)	Enable software to act upon the assertion of the RADIO_INHIBIT input. If the radio inhibit function is not used then this function should not be enabled.
SLEEPn Function (0x0B)	Enable software to act upon the assertion of the SLEEPn input. If the radio inhibit function is not used then this function should not be enabled.
CLI UART Baud Rate (0x0C)	The baud rate for the CLI UART interface. Supported values are defined in the Eterna datasheet. Absence of setting this field results in the default setting from the Eterna datasheet.
External PA/LNA Support Mode (0x0D)	Mode settings for supporting external RF PA and LNA hardware. Supported values are defined in the Eterna datasheet.
32 kHz Source (0x0E)	Selects the 32kHz source. Absence of setting this field results in a setting for the use of a 32 kHz xtal.
20 MHz xtal Part Number (0x0F-0x12)	Select the crystal part number included in the BOM See 040-0102 Eterna Hardware Integration Guide for the list of supported 20 MHz crystals.
20 MHz load trim (0x13)	The programmable load on the 20 MHz xtal. This value needs to be trimmed for each new design where a design changes the PCB layout or the crystal. Trimming is essential to center the radio channels. See 040-0102 Eterna Hardware Integration Guide for procedures to trim the crystal in a new design.
Radio Rx Trim (0x14)	Test mode trimming for the radio receive operation. Use of this configuration is not recommended.
Time of Flight Offset (ns) (0x15)	A 16 bit signed offset to be applied to all time of flight measurements. Use of this configuration is not recommended.
Current Limited Operation (0x16)	Enable for current limited operation. Current limited operation, will result in the device going into a low power state after completing its current atomic operation, following the voltage falling below the “Lower Voltage Limit”. The device will remain in a low power state for a duration in ms set by “Current Limit Off Time”. After waiting the device will check to see that the voltage is above “Upper Voltage Limit” prior to returning to an active state. If not the device will again return to a low power state for another “Current Limit Off Time” ms.

Lower Voltage Limit (0x16)	The lower voltage trip point that results in Eterna entering a low power state and waiting for “Current Limit Off Time” ms prior to attempting to resume operation.
Upper Voltage Limit (0x16)	The upper voltage trip point that Eterna checks when returning from a low power state. If the trip point is not met the device will return to a low power state for another “Current Limit Time Off” ms.
Current Limit Off Time (ms) (0x16)	The interval Eterna will remain in a low power state in ms prior to checking to see if the supply is above the “Upper Voltage Limit”.
IP Manager Ext. Memory Size (0x17)	**This field is only required for the LTC5800-IPRA, LTC5800-IPRB, LTP5901-IPRA, LTP5901-IPRB, LTP5901-IPRC, LTP5902-IPRA, LTP5902-IPRB and LTP5902-IPRC products and should not be enabled for other products.** Set this field to the appropriate external memory size and –IPRA / -IPRB product dash option.
Hardware Lock Key	Setting and enabling a Hardware Lock Key, results in Eterna’s memory being inaccessible and is advised for network security. It is envisioned that this setting would be enabled just prior to moving to production. See *040-0110 Eterna Board Serial Programmer Guide* for details on unlocking devices.

Addendum

Crystal changes on Printed Circuit Assembly (PCA) and Demo Circuits

Starting with Work Order ("WO") number D603679, PCA products and Demo Circuits containing the LTC5800 feature different crystals. The following image illustrates the differences on an LTP5901 PCA product.



New (WO# > D603679) Former (WO# < D603679)

Board Specific Parameters ("Fuse Table") associated with the version of 20MHz crystal

If a PCA Product (LTP59xx) or a Demo Circuit (DCxxxx) is reprogrammed after it leaves the factory, attention should be given to Board Specific Parameters.

Linear Technology provides binary images of the Board Specific Parameters called "Fuse Tables" for each PCA Product and Demo Circuit. Fuse Table files are named after the product and an internal part number of the form 680-xxxx-yyyy, where xxxx is a sequential number specific to the PCA or Demo Circuit and yyyy is a version number.

PCA products and Demo Circuits[1] based on LTP5901 and LTP5902 with WO greater than D603679 shall include Board Specific Parameters with version -0003 or newer.

LTP5900 products with WO greater than D603679 shall include Board Specific Parameters with version -0005 or newer.

Other Demo Circuits such as the DC9000, DC9001, DC9003 and DC9007 are all built prior to WO D603679 and may be programmed with any of the respective mote or manager recommended Board Specific Parameters.

[1] Demo Circuits based on LTP5901 or LTP5902 include DC9018, DC9020, DC9021, DC2126 and DC2274 series

Board Specific Parameters ("Fuse Table") for PCA with WO# D603679 or newer (greater)

PCA Products or Demo Circuits for WO number equal or greater than D603679 shall be programmed with the Fuse Tables shown below (or newer).

Current Products	Fuse Table
LTP5900IPC-WHMA	FT-LTP5900-WHMA-M13-9600-115K-680-0204-0005REV1.bin
LTP5901IPC-IPMA [2]	FT-LTP5901-IPMA-M4-115K-680-0237-0003REV1.bin FT-LTP5901-IPRA-M4-115K-680-0238-0003REV1.bin FT-LTP5901-IPRB-MEM-128K-M4-115K-680-0301-0003REV1.bin
LTP5901IPC-WHMA	FT-LTP5901-WHMA-M4-115K-680-0236-0003REV1.bin
LTP5902IPC-IPMA [2]	FT-LTP5902-IPMA-M4-115K-680-0241-0003REV1.bin FT-LTP5902-IPRA-M4-115K-680-0242-0003REV1.bin FT-LTP5902-IPRB-MEM-128K-M4-115K-680-0302-0003REV1.bin
LTP5902IPC-WHMA	FT-LTP5902-WHMA-M4-115K-680-0240-0003REV1.bin

Legacy Products [3]	Fuse Table (if WO is D603679 or greater)
LTP5900IPC-WHMA***	FT-LTP5900-WHMA-M13-9600-115K-680-0204-0005REV1.bin
LTP5901IPC-IPMA***	FT-LTP5901-IPMA-M4-115K-680-0237-0003REV1.bin
LTP5901IPC-IPRA***	FT-LTP5901-IPRA-M4-115K-680-0238-0003REV1.bin
LTP5901IPC-IPRB***	FT-LTP5901-IPRB-MEM-128K-M4-115K-680-0301-0003REV1.bin
LTP5901IPC-IPRC***	FT-LTP5901-IPRC-MEM-128K-M4-115K-680-0305-0003REV1.bin
LTP5901IPC-WHMA***	FT-LTP5901-WHMA-M4-115K-680-0236-0003REV1.bin
LTP5902IPC-IPMA***	FT-LTP5902-IPMA-M4-115K-680-0241-0003REV1.bin
LTP5902IPC-IPRA***	FT-LTP5902-IPRA-M4-115K-680-0242-0003REV1.bin
LTP5902IPC-IPRB***	FT-LTP5902-IPRB-MEM-128K-M4-115K-680-0302-0003REV1.bin
LTP5902IPC-IPRC***	FT-LTP5902-IPRC-MEM-128K-M4-115K-680-0306-0003REV1.bin
LTP5902IPC-WHMA***	FT-LTP5902-WHMA-M4-115K-680-0240-0003REV1.bin

[2] LTP5901IPC-IPMA and LTP5902IPC-IPMA products may be programmed as a mote, 32-mote manager (which does not require external memory) or 100-mote manager (which requires external memory). The programmed software image shall include the Main Executable corresponding to the mote or manager function and the Fuse Table specified in this table. The Fuse Tables are respectively named after -IPMA, -IPRA and -IPRB, for mote, manager and manager with memory.

[3] LTP5900, LTP5901 and LTP5902 based products were originally shipped pre-programmed at the factory; these product versions are still available but referred to as Legacy Products. In this column, "***" represents a three digit alphanumeric field signifying the pre-programmed software revision (e.g. "LTP5901IPC-IPMA**1D1**"). If a Legacy Product is re-programmed and its WO number is greater than D603679, the Fuse Table specified in this table or newer is required.

Demo Circuits	Fuse Table (if WO is D603679 or greater)
DC2126A	FT-LTP5901-IPMA-M4-115K-680-0237-0003REV1.bin
DC2274A-A	FT-DC2274A-MEM-128K-M4-115K-680-0383-0003REV1.bin
DC9018A-B	FT-DC9018A-MOTE-M4-115K-680-0379-0003REV1.bin
DC9018A-C	FT-DC9018A-MOTE-M4-115K-680-0379-0003REV1.bin
DC9018B-B	FT-DC9018B-MOTE-M4-115K-680-0380-0003REV1.bin
DC9018B-C	FT-DC9018B-MOTE-M4-115K-680-0380-0003REV1.bin
DC9020A	FT-DC9020A-MANAGER-MEM-128K-M4-115K-680-0381-0003REV1.bin
DC9020B	FT-DC9020B-MANAGER-MEM-128K-M4-115K-680-0382-0003REV1.bin

Board Specific Parameters ("Fuse Table") for PCA with WO# older than D603679

The following details the latest compatible Fuse Table for older PCA Products or Demo Circuits with WO number smaller than D603679.

Legacy Products [3]	Fuse Table (if WO is smaller than D603679)
LTP5900IPC-WHMA***	FT-LTP5900-WHMA-M13-9600-115K-680-0204-0004REV1.bin
LTP5901IPC-IPMA***	FT-LTP5901-IPMA-M4-115K-680-0237-0002REV1.bin
LTP5901IPC-IPRA***	FT-LTP5901-IPRA-M4-115K-680-0238-0002REV1.bin
LTP5901IPC-IPRB***	FT-LTP5901-IPRB-MEM-128K-M4-115K-680-0301-0002REV1.bin
LTP5901IPC-IPRC***	FT-LTP5901-IPRC-MEM-128K-M4-115K-680-0305-0002REV1.bin
LTP5901IPC-WHMA***	FT-LTP5901-WHMA-M4-115K-680-0236-0002REV1.bin
LTP5902IPC-IPMA***	FT-LTP5902-IPMA-M4-115K-680-0241-0002REV1.bin
LTP5902IPC-IPRA***	FT-LTP5902-IPRA-M4-115K-680-0242-0002REV1.bin
LTP5902IPC-IPRB***	FT-LTP5902-IPRB-MEM-128K-M4-115K-680-0302-0002REV1.bin
LTP5902IPC-IPRC***	FT-LTP5902-IPRC-MEM-128K-M4-115K-680-0306-0002REV1.bin
LTP5902IPC-WHMA***	FT-LTP5902-WHMA-M4-115K-680-0240-0002REV1.bin

Older Demo Circuits	Fuse Table (if WO is smaller than D603679)
DC2126A	FT-LTP5901-IPMA-M4-115K-680-0237-0002REV1.bin
DC2274A-A	FT-DC2274A-MEM-128K-M4-115K-680-0383-0002REV1.bin
DC9001A	FT-DC9003A-M4-115K-680-0222-0004REV1.bin
DC9001B	FT-DC9011A-M4-115K-MEM256k-680-0258-0003REV1.bin
DC9003A-B	FT-DC9003A-M4-115K-680-0222-0004REV1.bin
DC9003A-C	FT-DC9003A-M4-115K-680-0222-0004REV1.bin
DC9018A-B	FT-DC9018A-MOTE-M4-115K-680-0379-0002REV1.bin
DC9018A-C	FT-DC9018A-MOTE-M4-115K-680-0379-0002REV1.bin
DC9018B-B	FT-DC9018B-MOTE-M4-115K-680-0380-0002REV1.bin
DC9018B-C	FT-DC9018B-MOTE-M4-115K-680-0380-0002REV1.bin
DC9020A	FT-DC9020A-MANAGER-MEM-128K-M4-115K-680-0381-0002REV1.bin
DC9020B	FT-DC9020B-MANAGER-MEM-128K-M4-115K-680-0382-0002REV1.bin

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Document Status	Product Status	Definition
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