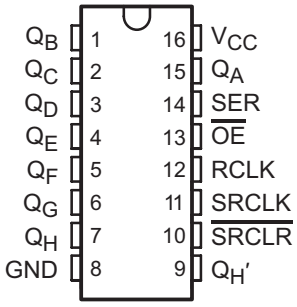
8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

Check for Samples: SN74HC595-EP

FEATURES

- **8-Bit Serial-In, Parallel-Out Shift**
- **Wide Operating Voltage Range of 2 V to 6 V**
- **High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads**
- **Low Power Consumption: 80-μA (Max) I_{CC}**
- **t_{pd} = 13 ns (Typ)**
- **±6-mA Output Drive at 5 V**
- **Low Input Current: 1 μA (Max)**
- **Shift Register Has Direct Clear**

PW PACKAGE
(TOP VIEW)



SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges available - contact factory

DESCRIPTION

The SN74HC595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

ORDERING INFORMATION(1)

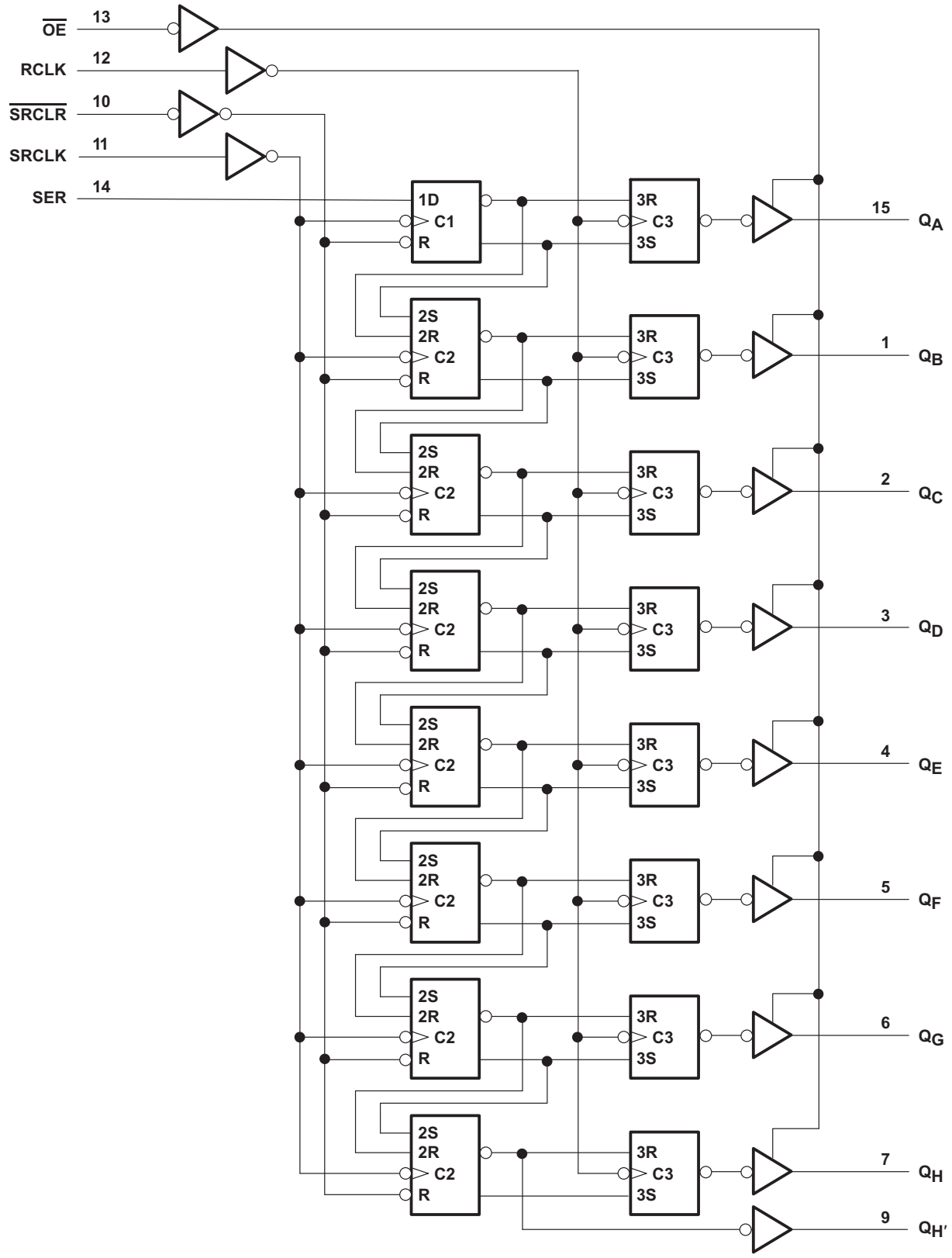
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	TSSOP – PW	Reel of 2000	SN74HC595MPWREP	HC595EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

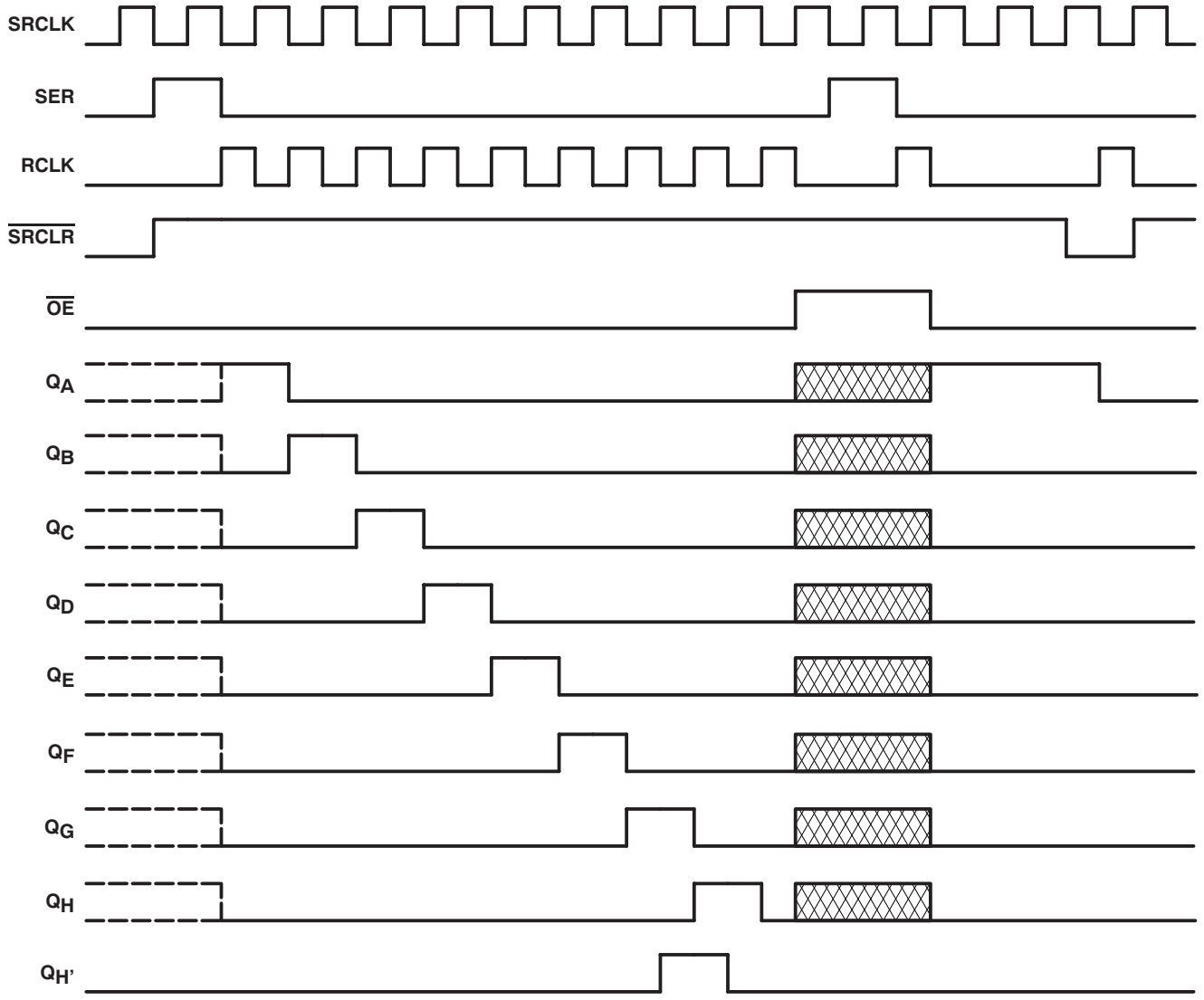
Table 1. FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A–Q_H are disabled.
X	X	X	X	L	Outputs Q_A–Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

LOGIC DIAGRAM (POSITIVE LOGIC)



TIMING DIAGRAM



NOTE: ▨ implies that the output is in 3-State mode.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range		−0.5 V to 7 V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$	±20 mA
I_{OK}	Output clamp current (2)	$V_O < 0$ or $V_O > V_{CC}$	±20 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	±35 mA
	Continuous current through VCC or GND		±70 mA
θ_{JA}	Package thermal impedance(3)		108°C/W
T_{stg}	Storage temperature range		−65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time(2)	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–55		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			T_A = –55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = −20 μA	2 V	1.9	1.998		1.9		V
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
		$Q_{H'}$, I_{OH} = −4 mA	4.5 V	3.98	4.3		3.7		
		Q_A–Q_H, I_{OH} = −6 mA		3.98	4.3		3.7		
		$Q_{H'}$, I_{OH} = −5.2 mA	6 V	5.48	5.8		5.2		
		Q_A–Q_H, I_{OH} = −7.8 mA		5.48	5.8		5.2		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1	V
			4.5 V		0.001	0.1		0.1	
			6 V		0.001	0.1		0.1	
		$Q_{H'}$, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4	
		Q_A–Q_H, I_{OL} = 6 mA			0.17	0.26		0.4	
		$Q_{H'}$, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4	
		Q_A–Q_H, I_{OL} = 7.8 mA			0.15	0.26		0.4	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, Q_A–Q_H		6 V		±0.01	±0.5		±10	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			8		160	μA
C_i			2 V to 6 V		3	10		10	pF

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		T_A = –55°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2	MHz
			4.5 V		31		21	
			6 V		36		25	
t_w	Pulse duration	SRCLK or RCLK high or low	2 V	80		120		ns
			4.5 V	16		24		
			6 V	14		20		
		$\overline{SRCLR}$ low	2 V	80		120		
			4.5 V	16		24		
			6 V	14		20		
t_{su}	Setup time	SER before SRCLK↑	2 V	100		150		ns
			4.5 V	20		30		
			6 V	17		25		
		SRCLK↑ before RCLK↑ (1)	2 V	75		113		
			4.5 V	15		23		
			6 V	13		19		
		$\overline{SRCLR}$ low before RCLK↑	2 V	50		75		
			4.5 V	10		15		
			6 V	9		13		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2 V	50		75		
			4.5 V	10		15		
			6 V	9		13		
t_h	Hold time, SER after SRCLK↑		2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			2 V	6	26		4.2		MHz
			4.5 V	31	38		21		
			6 V	36	42		25		
t_{pd}	SRCLK	$Q_{H'}$	2 V		50	160		240	ns
			4.5 V		17	32		48	
			6 V		14	27		41	
	RCLK	Q_A–Q_H	2 V		50	150		225	
			4.5 V		17	30		45	
			6 V		14	26		38	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	2 V		51	175		261	ns
			4.5 V		18	35		52	
			6 V		15	30		44	
t_{en}	$\overline{OE}$	Q_A–Q_H	2 V		40	150		255	ns
			4.5 V		15	30		45	
			6 V		13	26		38	
t_{dis}	$\overline{OE}$	Q_A–Q_H	2 V		42	200		300	ns
			4.5 V		23	40		60	
			6 V		20	34		51	
t_t		Q_A–Q_H	2 V		28	60		90	ns
			4.5 V		8	12		18	
			6 V		6	10		15	
		$Q_{H'}$	2 V		28	75		110	
			4.5 V		8	15		22	
			6 V		6	13		19	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted)

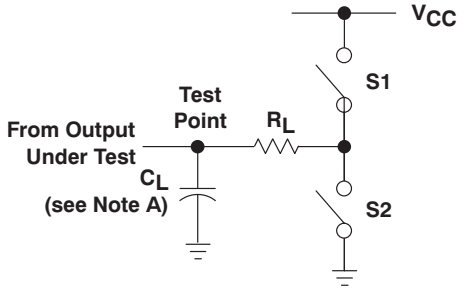
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	RCLK	Q_A–Q_H	2 V		60	200		300	ns
			4.5 V		22	40		60	
			6 V		19	34		51	
t_{en}	$\overline{OE}$	Q_A–Q_H	2 V		70	200		298	ns
			4.5 V		23	40		60	
			6 V		19	34		51	
t_t		Q_A–Q_H	2 V		45	210		315	ns
			4.5 V		17	42		63	
			6 V		13	36		53	

OPERATING CHARACTERISTICS

T_A = 25°C

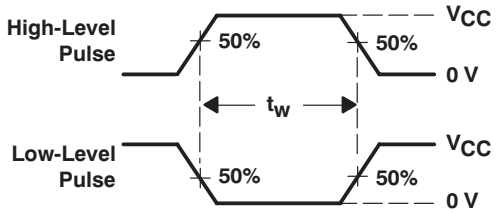
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	400	pF

PARAMETER MEASUREMENT INFORMATION

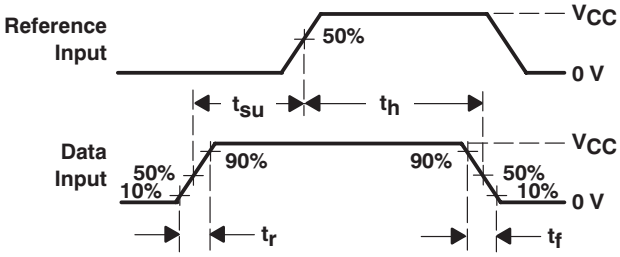


LOAD CIRCUIT

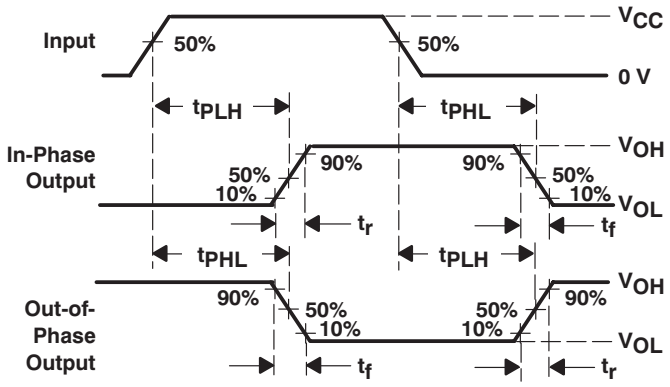
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t			50 pF or 150 pF	Open	Open



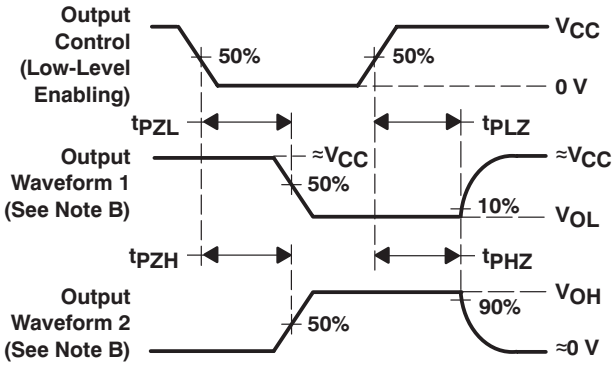
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC595MPWREP	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74HC595-EP :

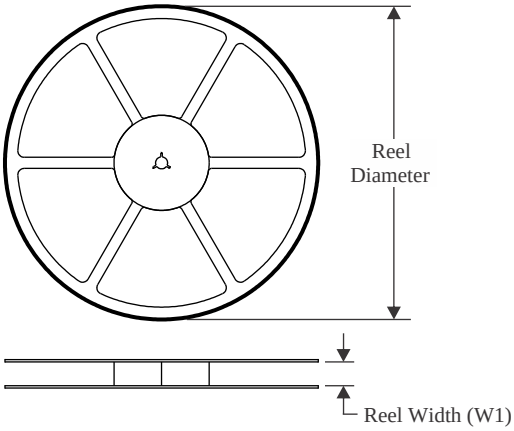
- Catalog: SN74HC595
- Automotive: SN74HC595-Q1
- Military: SN54HC595

NOTE: Qualified Version Definitions:

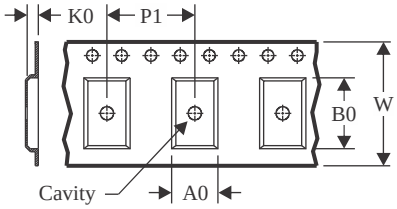
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

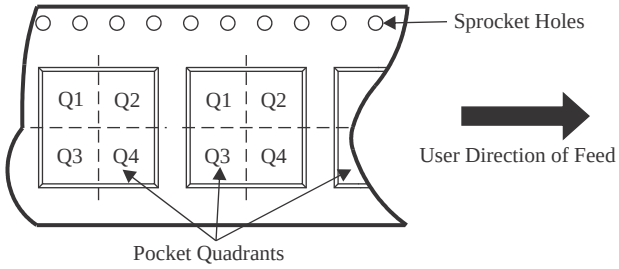


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

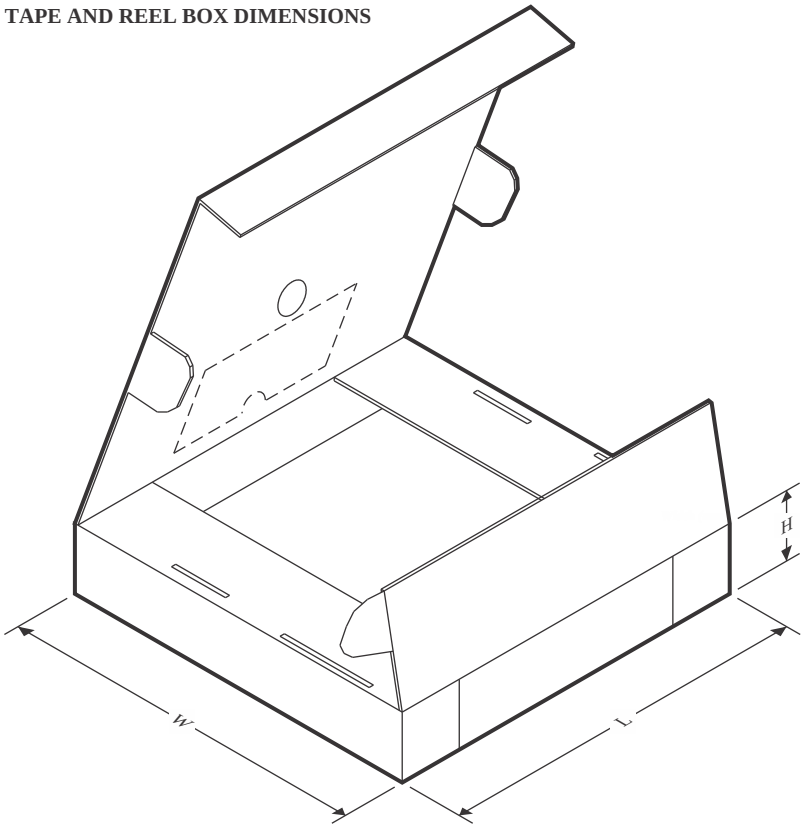
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC595MPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

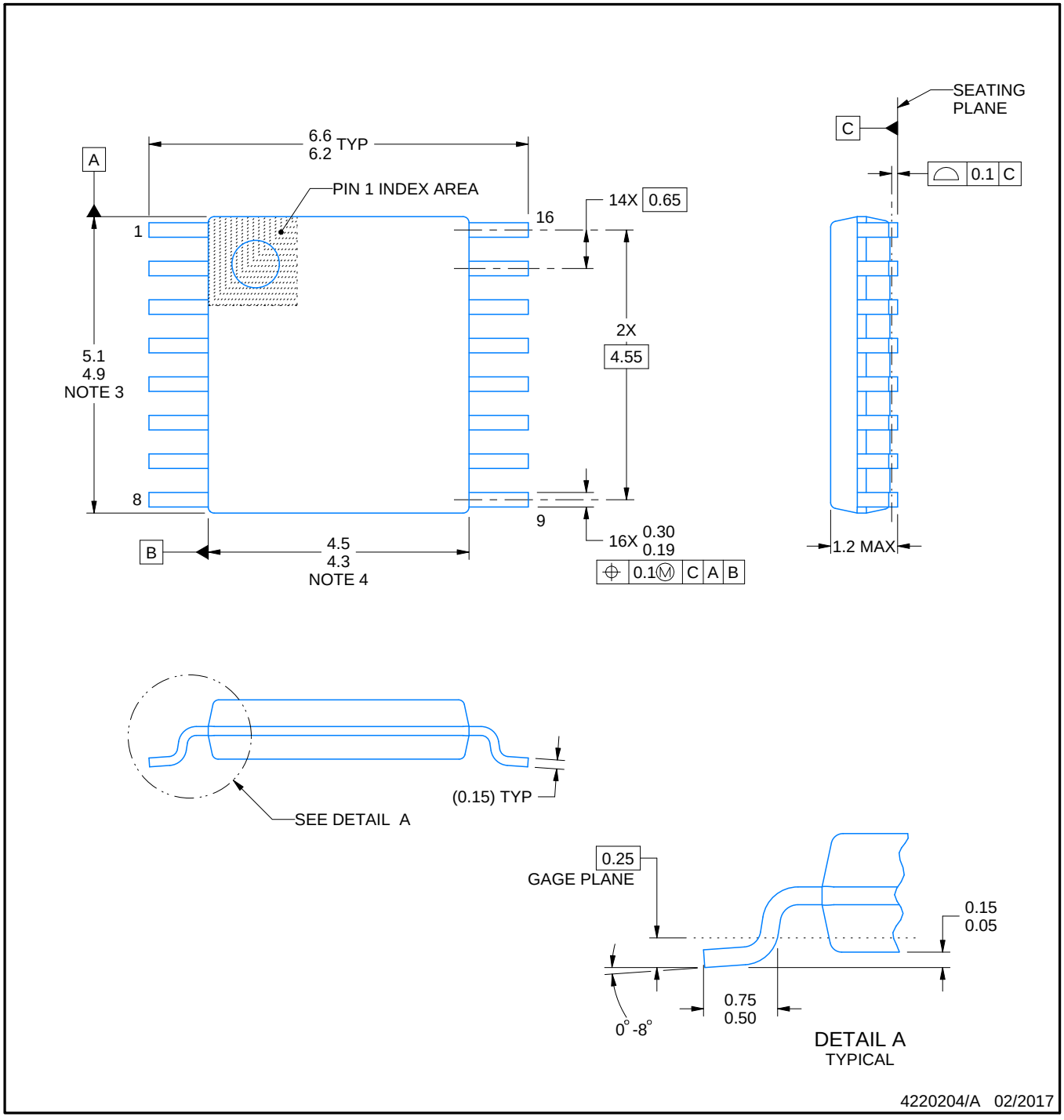
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC595MPWREP	TSSOP	PW	16	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0016A

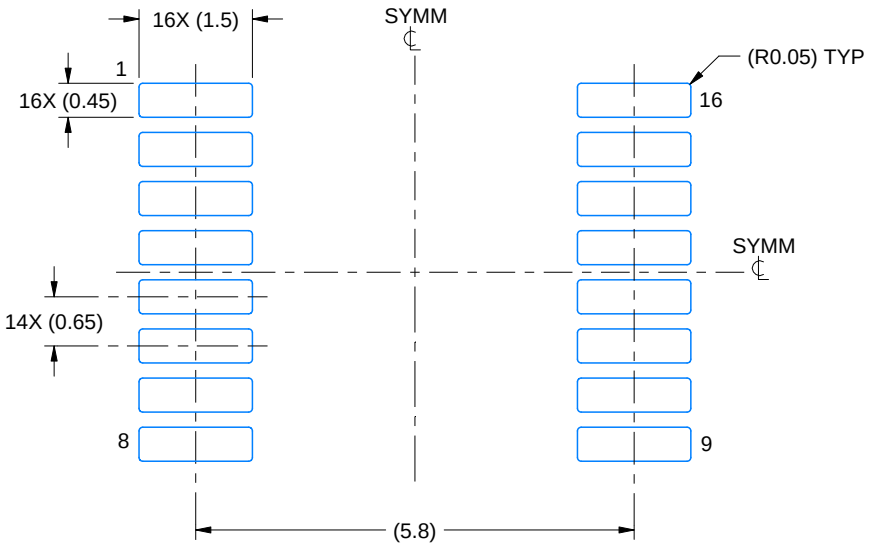
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

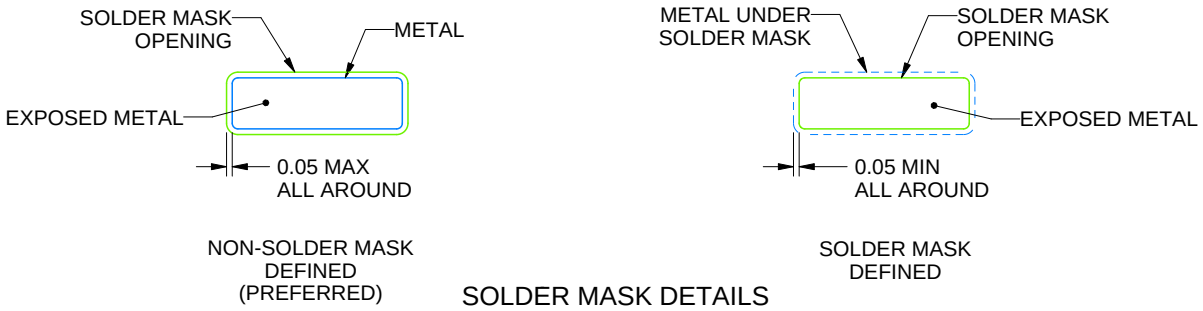


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

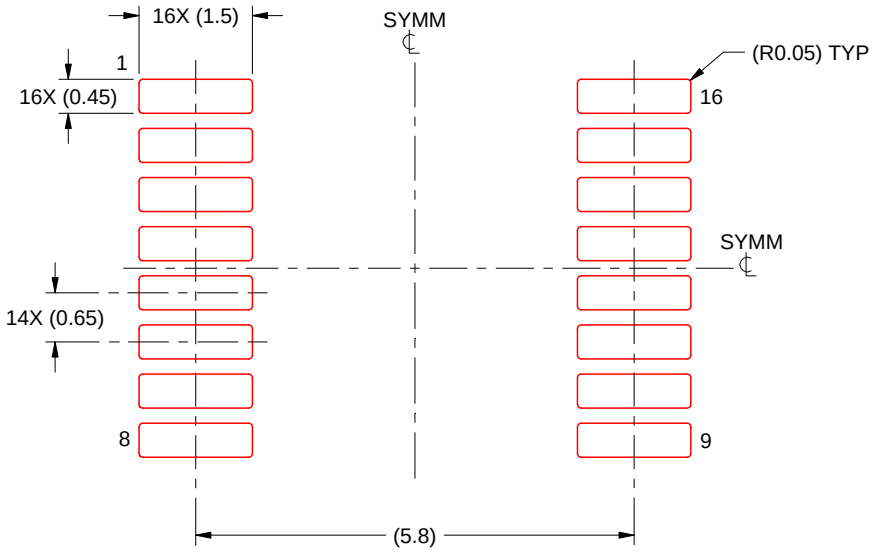


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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