IR3826 OptiMOS™ IPOL

23 A single-voltage synchronous Buck regulator

Features

- Single 5 V to 17 V application or Wide Input Voltage Range from 1.0 V to 17 V with external Vcc
- Precision Reference Voltage (0.6 V ± 0.6%) for Output Voltage Range: 0.6 V to 0.86×Vin
- Enhanced Line/Load Regulation with Feed-Forward
- Programmable Switching Frequency up to 1.5 MHz
- Monotonic Start-Up with Internal Digital Soft-Start & Enhanced Pre-Bias Start-Up
- Thermally Compensated Internal Over-Current Protection with Three Selectable Settings
- Enable input with Voltage Monitoring Capability & Programmable Power Good Output
- Thermal Shut Down
- Operating temp: -40 °C < Tj < 125 °C
- Small Size: 6 mm x 5 mm PQFN
- Lead-free, Halogen-free and RoHS2 Compliant

Potential applications

Server Applications

- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The IR3826 is an easy-to-use, fully integrated and highly efficient dc-dc regulator.
The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make the IR3826 a small footprint solution, providing high-efficiency power delivery.
The IR3826 is a versatile regulator, operating with wide input and output voltage range, offering programmable switching frequency from 300 kHz to 1.5 MHz, and providing three selectable over current limits.
It also features important protection functions, such as pre-bias start-up, thermally compensated current limit, over voltage protection and thermal shutdown to give required system level security in the event of fault conditions.

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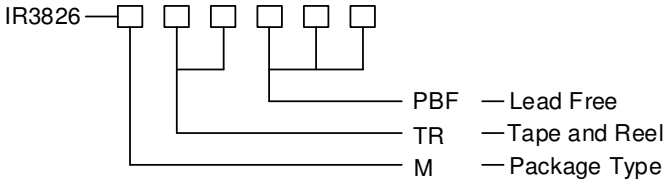
1 Ordering information

Table 1 Ordering Information

Base Part Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
IR3826	QFN 6 mm x 5 mm	Tape and Reel	4000	IR3826MTRPBF



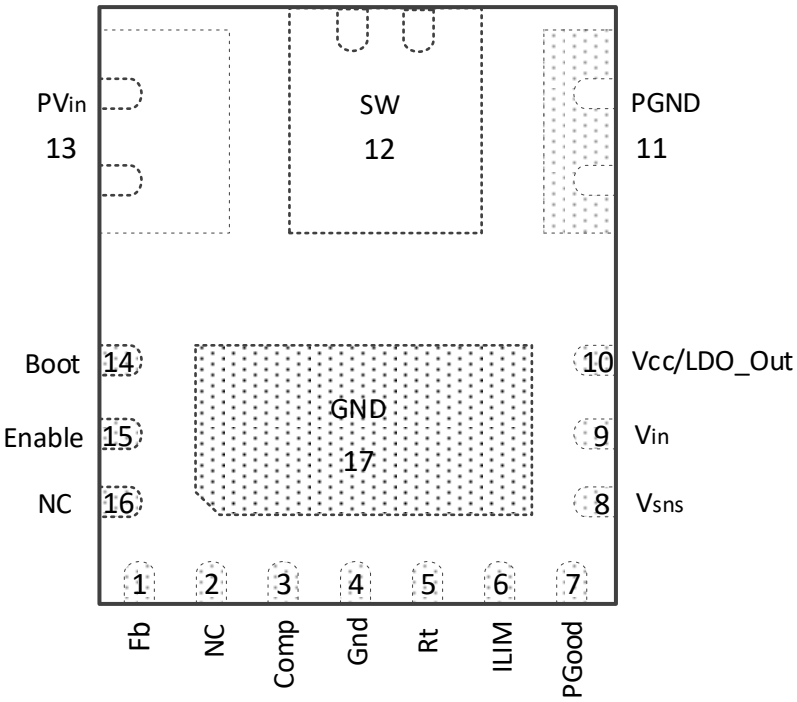


Figure 1 Package Top View

2 Functional block diagram

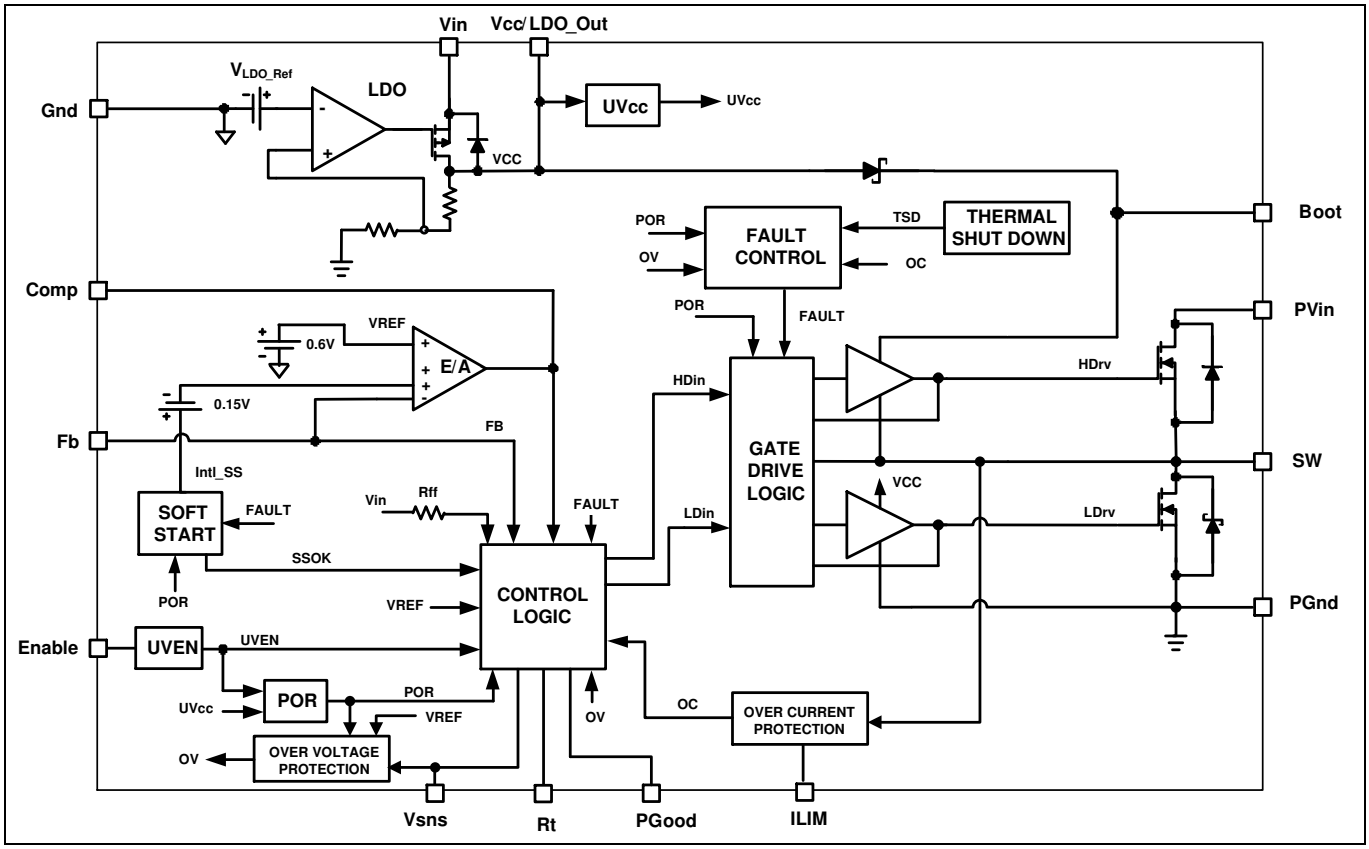


Figure 2 Block diagram

3 Typical application diagram

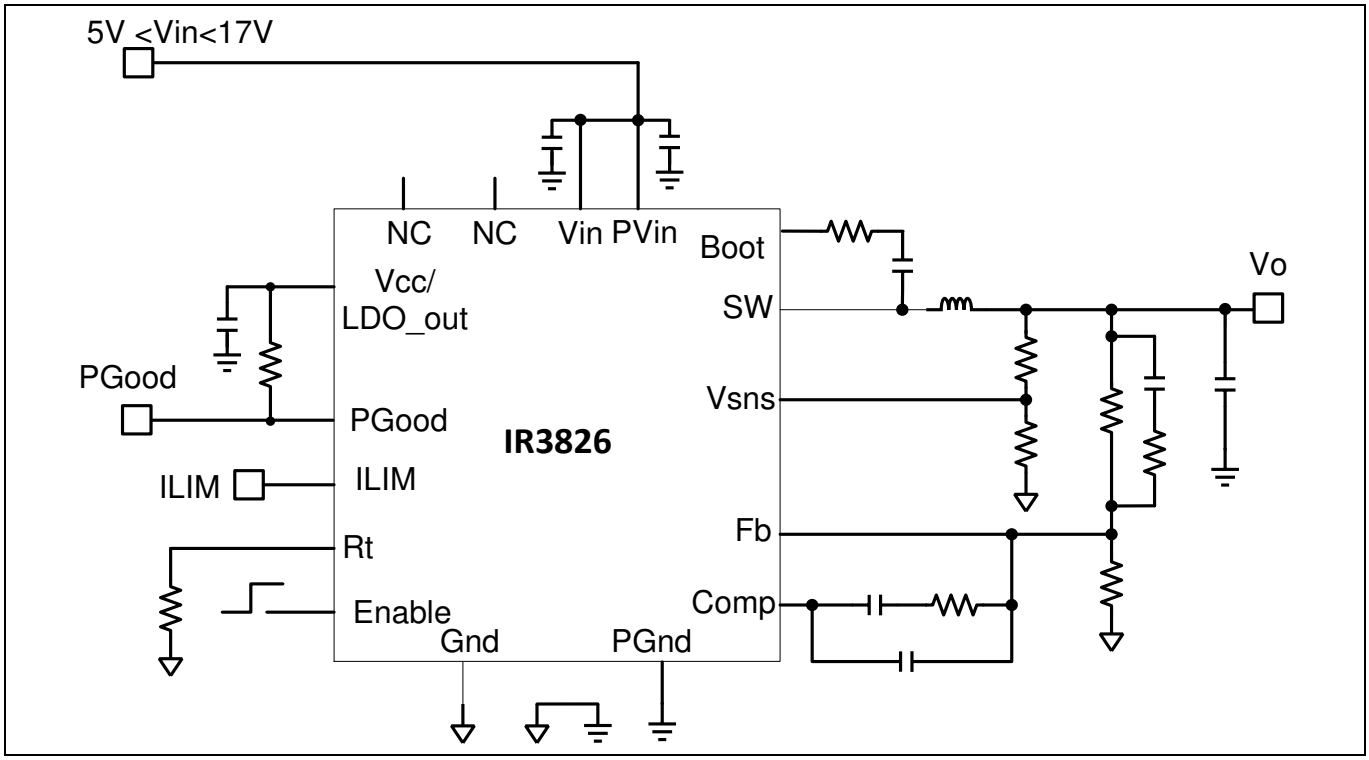


Figure 3 IR3826 basic application circuit

4 Pin descriptions

Table 2 Pin descriptions

Pin#	Pin name	Pin description
1	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	NC	Not Connected
3	Comp	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to Fb to provide loop compensation.
4	Gnd	Signal ground for internal reference and control circuitry.
5	Rt	Set switching frequency. Use an external resistor from this pin to Gnd to set the free-running switching frequency.
6	ILIM	Current Limit set point. This pin allows the trip point to be set to one of three possible settings by floating this pin, connecting it to Vcc or connecting it to PGnd.
7	PGood	Power Good status pin. Connect a pull up resistor from this open drain output to a voltage lower than or equal to the Vcc supply.
8	Vsns	Sense pin for over-voltage protection and PGood.
9	Vin	Input voltage for Internal LDO. A 1.0 µF capacitor should be connected between this pin and PGnd. If an external supply is connected to Vcc/LDO_out pin, this pin should be shorted to Vcc/LDO_out pin.
10	Vcc/LDO_Out	Input Bias for external Vcc Voltage/ output of internal LDO. Place a 2.2 µF capacitor from this pin to PGnd.
11	PGnd	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
12	SW	Switch node. This pin is connected to the output inductor.
13	PVin	Input voltage for power stage.
14	Boot	Supply voltage for the high side driver, a 100 nF capacitor should be connected between this pin and SW pin.
15	Enable	Enable pin to turn the device on and off. Connecting this pin to PVin pin through a resistor divider implements the input voltage UVLO function.
16	NC	Not Connected
17	Gnd	Signal ground for internal reference and control circuitry.

5 Absolute maximum ratings

Table 3 Absolute maximum ratings

PVin, Vin	-0.3 V to 25 V
Vcc/LDO_Out	-0.3 V to 8 V (Note 1)
Boot	-0.3 V to 33 V
SW	-0.3 V to 25 V (dc), -5 V to 25 V (ac, 20 ns)
Boot to SW	-0.3 V to VCC + 0.3 V (Note 2)
ILIM, PGood	-0.3 V to VCC + 0.3 V (Note 2)
Other Input/Output Pins	-0.3 V to +3.9 V
PGnd to Gnd	-0.3 V to +0.3 V
Thermal information	
Junction to Ambient Thermal Resistance θ_{JA}	17 °C/W (Note 3)
Junction to PCB Thermal Resistance $\theta_{J\text{-}PCB}$	3.5 °C/W (Note 4)
Junction to Case Top Thermal Resistance θ_{JCtop}	15 °C/W
Storage Temperature Range	-55 °C to 150 °C
Junction Temperature Range	-40 °C to 150 °C (Note 1)

Note:

[1] Vcc must not exceed 7.5 V for Junction Temperature between -10 °C and -40 °C
[2] Must not exceed 8 V
[3] Thermal resistance (θ_{JA}) is measured with components mounted on a standard IRDC3826 demo board in free air.
[4] Thermal resistance ($\theta_{J\text{-}PCB}$) is based on the board temperature near the PVin pin.

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

6 Electrical specifications

Table 4 Recommended operating conditions for reliable operation with margin

Input Voltage Range, PVin (Note 4)	1 V to 17 V
Input Voltage Range, Vin (Note 5)	5 V to 17 V
Supply Voltage Range, Vcc (Note 6)	4.5 V to 6.5 V
Supply Voltage Range, Boot to SW	4.5 V to 6.5 V
Output Voltage Range	0.6 V to 0.86 x PVin
Output Current Range	0 to 23 A
Switching Frequency (Note 5, Note 6)	300 kHz to 1500 kHz (8V ≤ Vin ≤ 17V)
	700 kHz to 1500 kHz (4.5V ≤ Vin < 8V)
Operating Junction Temperature	-40 °C to 125 °C

Note: *[4] Maximum absolute SW node voltage should not exceed 25 V. A common practice is to have 20% margin on the maximum SW node voltage in the design. For applications requiring PVin equal to or above 14 V, a small resistor in series with the Boot pin should be used to ensure the maximum SW node spike voltage does not exceed 20 V. Alternatively, a snubber can be used at the SW node to reduce the SW node spike.*

Note: *[5] For internally biased single rail operation. When Vin drops below 6 V, the internal LDO may enter dropout mode, resulting in lower LDO voltage and lower Over Current limits. Please note that in dropout mode, the LDO voltage must be above the Vcc UVLO threshold voltage to ensure a proper operation.*

Note: *[6] Vcc/LDO_out can be connected to an external regulated supply. If so, the Vin input should be connected to Vcc/LDO_out pin to bypass the internal LDO.*

7 Electrical characteristics

Note: Unless otherwise specified, the specifications apply over, 6 V ≤ Vin = PVin ≤ 17 V, in 0 °C < T_J < 125 °C. Typical values are specified at Ta = 25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Power Losses	P_{LOSS}	Vin = 12 V, V_O = 1.2 V, I_O = 23 A, Fs = 600 kHz, L = 215 nH, Natural Convection, Vcc = Internal LDO, Note 7		3.47		W
Top Switch	$R_{ds(on)\_Top}$	VBoot – Vsw= 5.3 V, I_O = 23 A, Tj =25 °C		3.8		mΩ
Bottom Switch	$R_{ds(on)\_Bot}$	Vcc = 5.3 V, I_O = 23 A, Tj =25 °C		2.25		mΩ
Bootstrap Diode Forward Voltage		I(Boot) = 15 mA, Tj = 25 °C	200	420	500	mV
		I(Boot) = 15 mA, 0 °C < Tj < 125 °C	200	420	600	mV
SW Leakage Current	I_{SW}	SW = 0 V, Enable = 0 V			1	µA
		SW = 0 V, Enable = high, No Switching				
Dead Band Time	T_{db}	Note 7		20		ns
Supply Current	Vin					
Vin Supply Current (standby)	$I_{in(Standby)}$	EN = Low, No Switching		100	150	µA
Vin Supply Current (dynamic)	$I_{in(Dyn)}$	EN = High, Fs = 600 kHz, Vin=Pvin=17 V		15	25	mA
VCC LDO Output	Vcc					
Output Voltage	Vcc	Vin(min) = 6 V, Icc = 0-50 mA, Cload = 2.2 µF	5.0	5.3	5.6	V
VCC Dropout	Vcc_drop	Vin = 5 V, Icc=30 mA, Cload=2.2 µF			0.88	V
Short Circuit Current	I_{short}		-	60	-	mA
Oscillator	R_T					
Rt Voltage	Vrt			1.0		V
Frequency Range	Fs (Note 9)	Rt = 80.6 kΩ	270	300	330	kHz
		Rt = 39.2 kΩ	540	600	660	kHz
		Rt = 15.0 kΩ	1350	1500	1650	kHz
Ramp Amplitude	Vramp Vin slew rate max = 1V/µs	Vin = 6 V, Note 7		0.90		Vp-p
		Vin = 12 V, Note 7		1.80		Vp-p
		Vin = 17 V, Note 7		2.55		Vp-p

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		Vcc=Vin=5 V, Note 7		0.75		
Ramp Offset	Ramp(os)	Note 7		0.16		V
Min Pulse Width	Tmin(ctrl)	Note 7			60	ns
Max Duty Cycle	Dmax	Fs = 300 kHz, Pvin = Vin = 12 V	86			%
Fixed Off Time	Toff	Note 7		200	250	ns
Error Amplifier	Comp					
Input Bias Current	Ifb(E/A)		-1		+1	µA
Sink Current	Isink(E/A)		0.4	0.85	1.2	mA
Source Current	Isource(E/A)		4	7.5	11	mA
Slew Rate	SR	Note 7	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 7	20	30	40	MHz
DC Gain	Gain	Note 7	100	110	120	dB
Maximum output Voltage	Vmax(E/A)		1.7	2.0	2.3	V
Minimum output Voltage	Vmin(E/A)				100	mV
Reference Voltage	Vref					
Feedback Voltage	Vfb			0.6		V
Accuracy		25 °C < Tj < 85 °C	-0.6		+0.6	%
		-40 °C < Tj < 125 °C, Note 8	-1.2		+1.2	
Soft Start						
Soft Start Ramp Rate	Ramp S-Start		0.16	0.2	0.24	mV/µs
Power Good	Pgood					
Pgood Turn on Threshold	VPG(on)	Vsns Rising	85	90	95	% Vref
Pgood Lower Turn off Threshold	VPG(lower)	Vsns Falling	80	85	90	% Vref
Pgood Turn on Delay	VPG(on)_Dly	Vsns Rising, see VPG(on)		2.5		ms
Pgood Upper Turn off Threshold	VPG(Upper)	Vsns Rising	115	120	125	% Vref
Pgood Comparator Delay	VPG(comp)_Dly	Vsns < VPG(lower) or Vsns > VPG(upper)	1	2	3.5	µs
Pgood Voltage Low	PG(voltage)	Ipgood = -5 mA			0.5	V
Under-Voltage Lockout						
Vcc-Start Threshold	VCC_UVLO_Start	Vcc Rising Trip Level	3.9	4.1	4.3	V
Vcc-Stop Threshold	VCC_UVLO_Stop	Vcc Falling Trip Level	3.6	3.8	4.0	
Enable-Start-Threshold	Enable_UVLO_Start	Supply ramping up	1.14	1.2	1.26	V
Enable-Stop-Threshold	Enable_UVLO_Stop	Supply ramping down	0.95	1	1.05	
Enable Leakage Current	Ien	Enable = 3.3 V			1	µA
Over-Voltage Protection	Vsns					

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OVP Trip Threshold	OVP_Vth	Vsns Rising	115	120	125	% Vref
OVP Comparator Delay	OVP_Tdly		1	2	3.5	µs
Over-Curent Protection						
Current Limit	ILIMIT	ILIM=VCC, VCC = 5.3 V, Tj=25 °C	22.60	29	33.6	A
		ILIM=floating, VCC = 5.3 V, Tj=25 °C	20.09	25.7	29.8	
		ILIM=PGnd, VCC =5.3 V, Tj=25°C	16.65	21.4	24.8	
Hiccup blanking time	Tblk_Hiccup			20.48		ms
Over-Temperature Protection						
Thermal Shutdown Threshold	Ttsd	Note 7		145		°C
Hysteresis	Ttsd_hys	Note 7		20		

Note: *[7] Guaranteed by design and not tested in production*

Note: *[8] Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.*

Note: *[9] For 4.5 V ≤ Vin < 8 V, Fs must be within 700 kHz and 1500 kHz. For 8 V ≤ Vin ≤ 17 V, 300 kHz to 1500 kHz, can be used.*

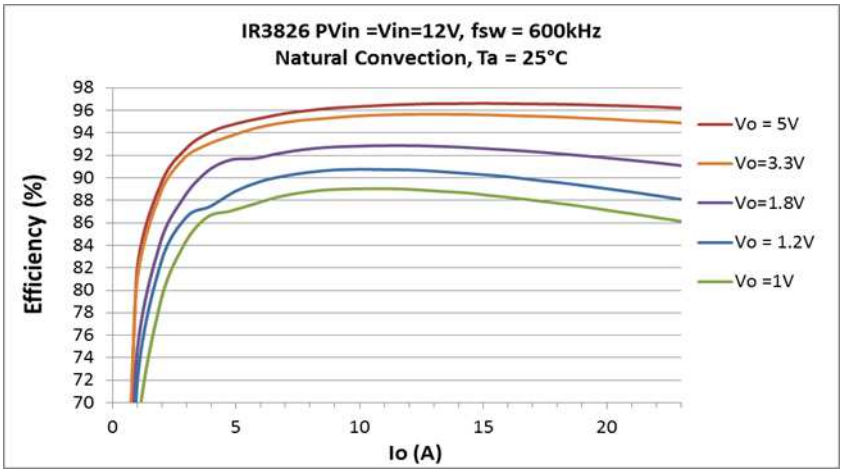
8 Typical efficiency and power loss curves

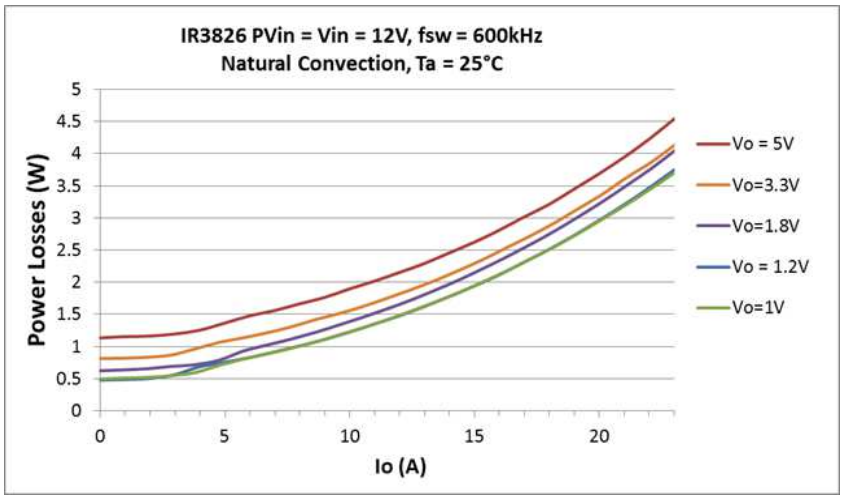
8.1 $PV_{in} = V_{in} = 12$ V, $F_s = 600$ kHz

$PV_{in} = V_{in} = 12$ V, Vcc = Internal LDO, $I_o = 0$ A-23 A, $F_s = 600$ kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3826, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 5 Inductors for $PV_{in}=V_{in}=12$ V, $F_s = 600$ kHz

Vout (V)	Lout (uH)	P/N	DCR (mΩ)	Size (mm)
1.0	0.15	HCB178380D-151 (Delta)	0.15	10.8 x 8 x 8
1.2	0.215	HCB1075N-211 (Delta)	0.29	10.1 x 7.8 x 7.3
1.8	0.215	HCB1075N-211 (Delta)	0.29	10.1 x 7.8 x 7.3
3.3	0.47	744309047 (Wurth)	0.165	14 x 13 x 9
5	0.47	744309047 (Wurth)	0.165	14 x 13 x 9



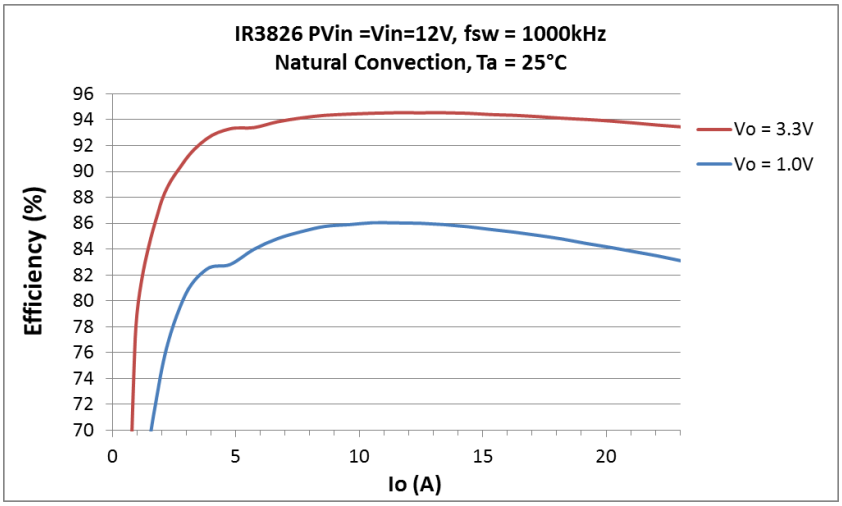


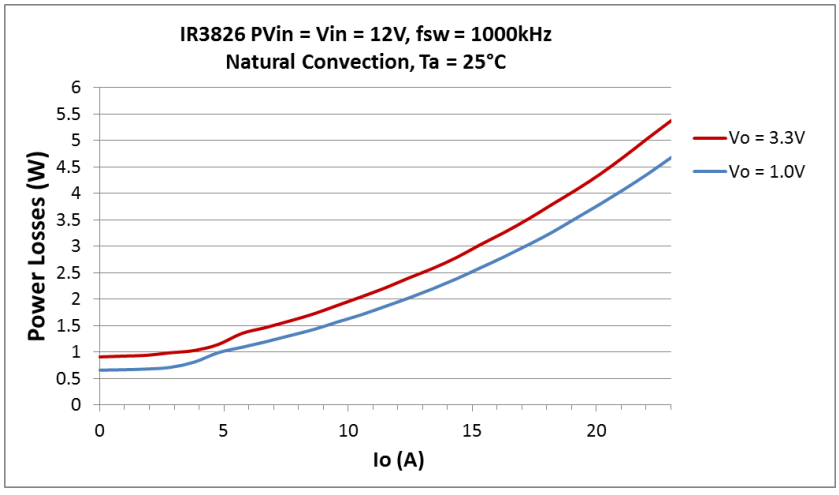
8.2 $PV_{in} = V_{in} = 12$ V, $F_s = 1000$ kHz

$PV_{in} = V_{in} = 12$ V, Vcc = Internal LDO, Io = 0 A-23 A, Fs = 1000 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3826, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 6 Inductors for $PV_{in}=V_{in}=12$ V, $F_s = 1000$ kHz

Vout (V)	Lout (uH)	P/N	DCR (mΩ)	Size (mm)
1.0	0.1	HCBR946740D-101 (Delta)	0.31	9.4 x 6.7 x 4.1
3.3	0.215	HCB1075N-211 (Delta)	0.29	10.1 x 7.8 x 7.3



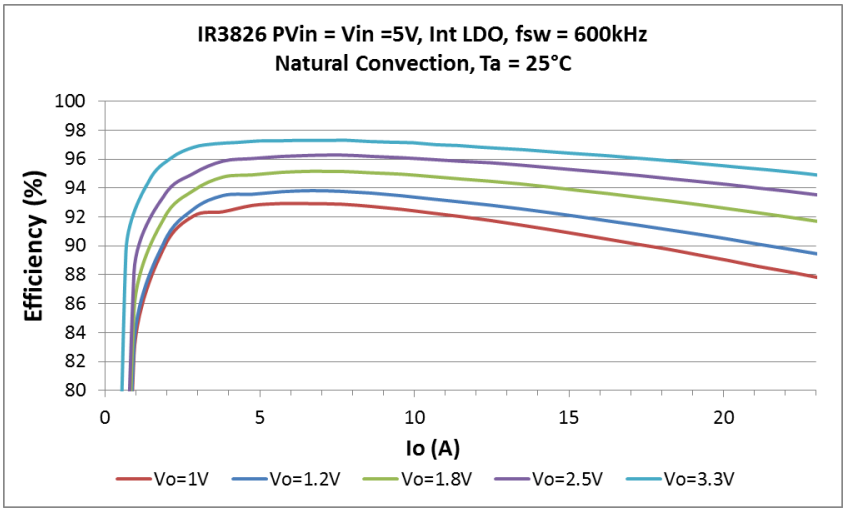


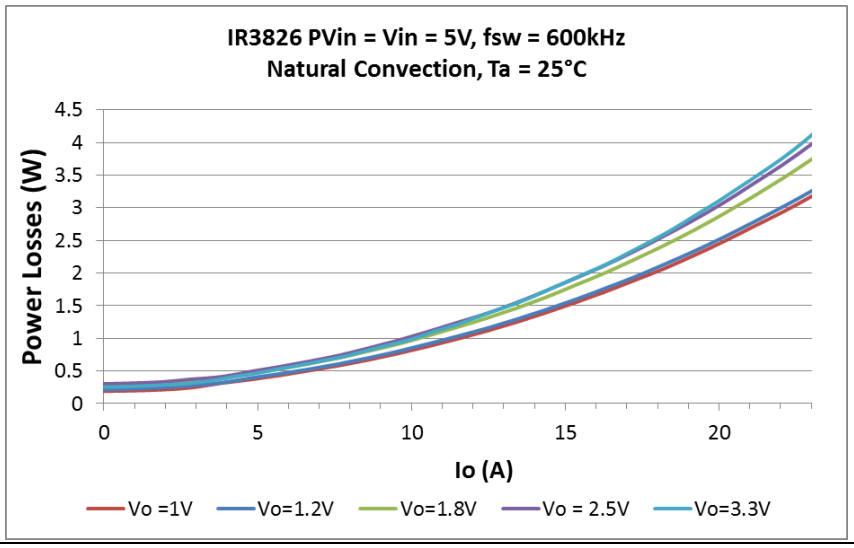
8.3 $PV_{in} = V_{in} = Vcc = 5\ V, F_s = 600\ kHz$

$PV_{in} = V_{in} = Vcc = 5.0$ V, $I_o = 0$ A – 23 A, $F_s = 600$ kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3826, the inductor losses, the losses of the input and output capacitors and and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 7 Inductors for $PV_{in}=V_{in}=Vcc=5$ V, $F_s = 600$ kHz

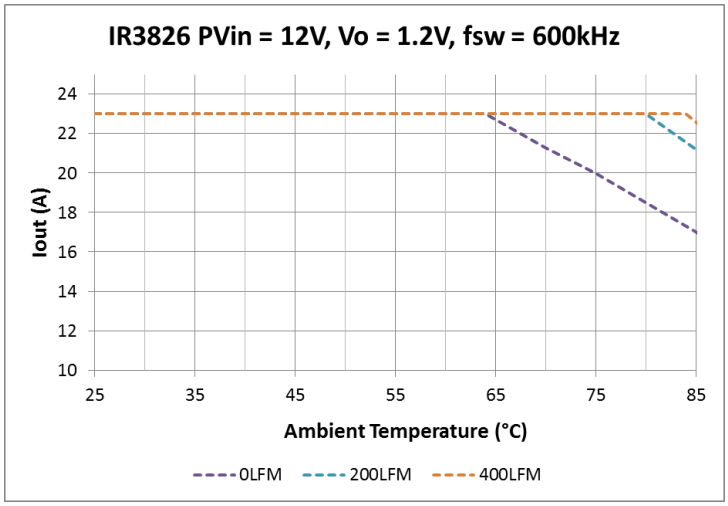
Vout (V)	Lout (uH)	P/N	DCR (mΩ)	Size (mm)
1.0	0.18	HCB118080D-181 (Delta)	0.19	11 x 8 x8
1.2	0.18	HCB118080D-181 (Delta)	0.19	11 x 8 x8
1.8	0.215	HCB1075N-211 (Delta)	0.29	10.1 x 7.8 x 7.3
2.5	0.215	HCB1075N-211 (Delta)	0.29	10.1 x 7.8 x 7.3
3.3	0.215	HCB1075N-211 (Delta)	0.29	10.1 x 7.8 x 7.3

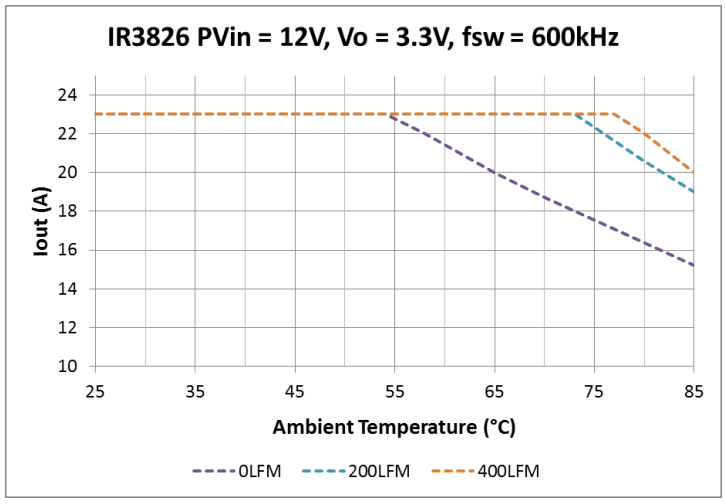




9 Thermal Derating curves

Measurement is done on Evaluation board of IRDC3826. PCB is a 6-layer board with 1.5 oz Copper for top and bottom layer and 2 oz Copper for the inner layers, FR4 material, size 3.0”x3.0”.





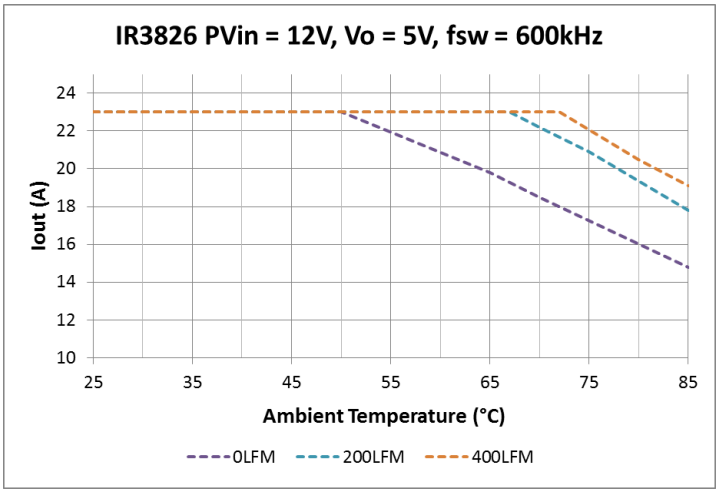


Figure 4 Thermal derating curves, PV_{in} = 12 V, V_{out}=1.2 V/3.3 V/5 V, Vcc = Internal LDO, F_s = 600 kHz

10 $R_{DS(ON)}$ of MOSFET Over Temperature

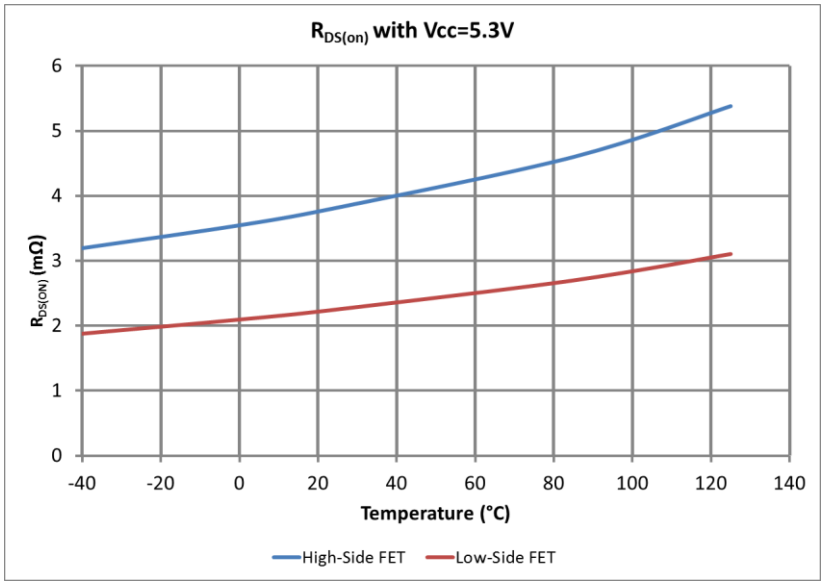


Figure 5 $R_{DS(on)}$ of MOSFETs over Temperature

11 Typical operating characteristics (-40 °C to +125 °C)

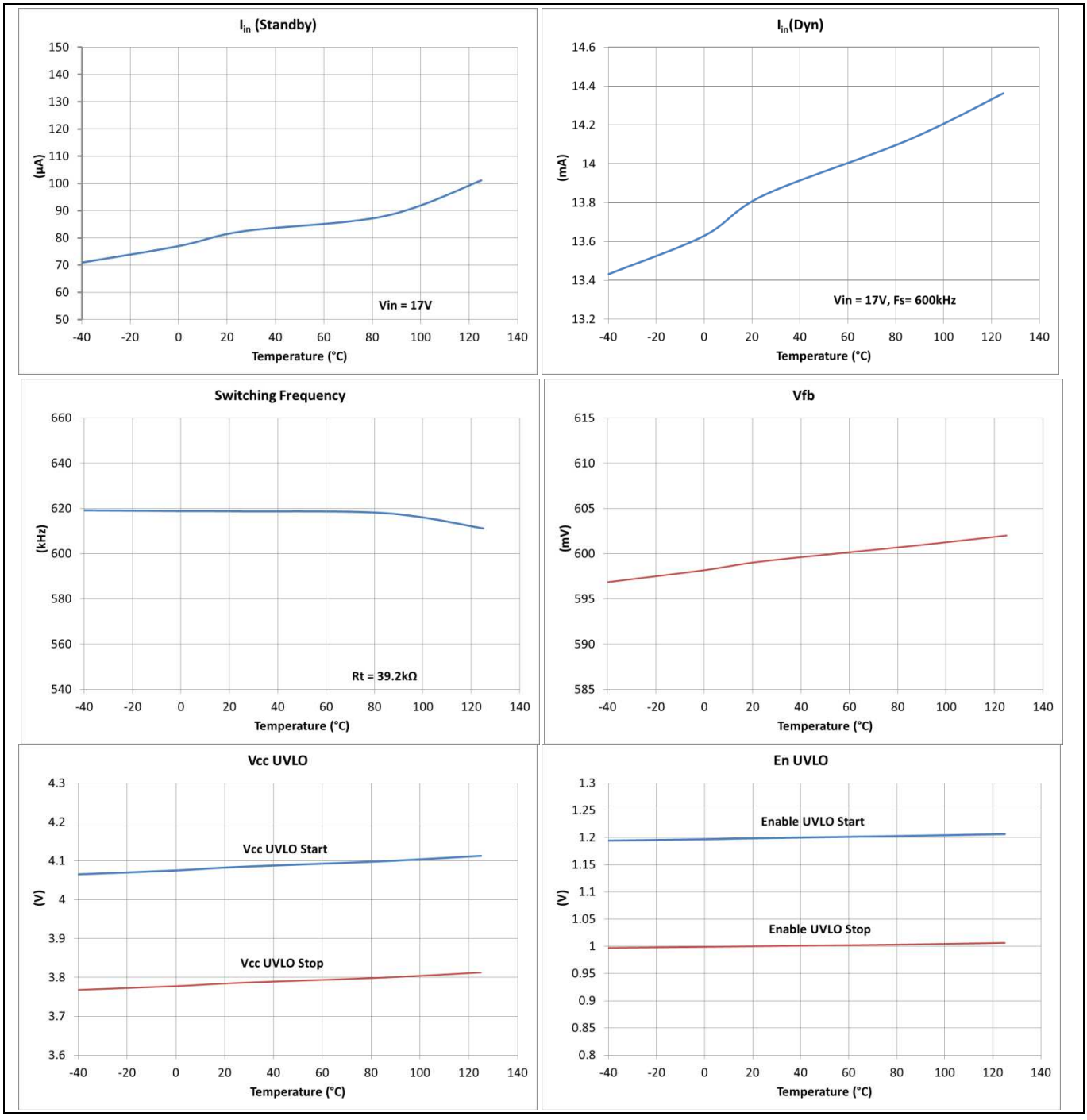


Figure 6 Typical operating characteristics (set 1 of 2)

Typical operating characteristics (-40 C to +125 C)

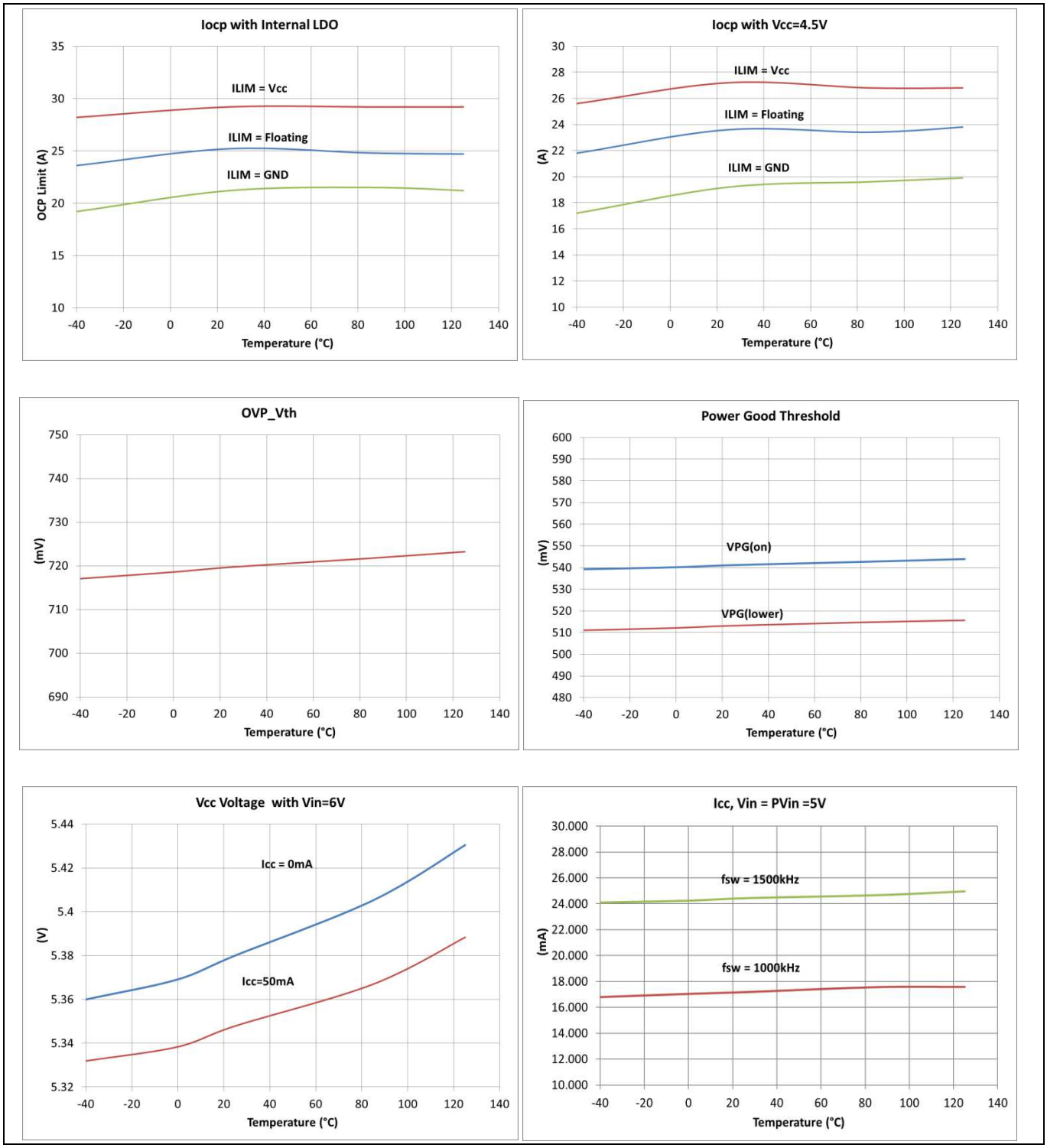


Figure 7 Typical operating characteristics (set 2 of 2)

12 Theory of operation

12.1 Description

The IR3826 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 300 kHz to 1.5 MHz. This provides the capability of optimizing the design in terms of size and performance. IR3826 provides precisely regulated output voltage programmed via two external resistors from 0.6 V to 0.86*Vin.

The IR3826 operates with an internal bias supply (LDO) which is connected to the Vcc/LDO_out pin. This allows operation with single supply. The IC can also be operated with an external supply from 4.5 V to 6.5 V, allowing an extended operating input voltage (PVin) range from 1.0 V to 17 V. When using the internal LDO supply, the Vin pin should be connected to Pvin pin. If an external supply is used, it should be connected to the Vcc/LDO_Out pin and the Vin pin should be shorted to Vcc/LDO_Out pin as well.

The device utilizes the on-resistance of the low side MOSFET (sync FET) for over current protection. This method enhances the converter's efficiency and reduces cost by eliminating the need for an external current sense resistor. The IR3826 includes two low $R_{DS(on)}$ MOSFETs using Infineon's OptiMOS™ technology. These are specifically designed for high efficiency applications.

12.2 Voltage Loop Compensation design

The IR3826 uses PWM voltage mode control. The output voltage of the POL, sensed by a resistor divider, is fed into an internal Error Amplifier (E/A). The output of the E/A is then compared to an internal ramp voltage to determine the pulse width of the gate signal for the control FET. The amplitude of the ramp voltage is proportional to Vin so that the bandwidth of the voltage loop remains almost constant for different input voltages. This feature is called input voltage Feedforward. It allows the feedback loop design independent of the input voltage. Please refer to the feedforward section for more information.

A RC network has to be connected between the FB pin and the COMP pin to form a feedback compensator. The goal of the compensator design is to achieve a high control bandwidth with a phase margin of 45° or above. The high control bandwidth is beneficial for the loop dynamic response, which helps to reduce the number of output capacitors, the PCB size and the cost. A phase margin of 45° or higher is desired to ensure system stability. The proprietary PWM modulator in the IR3826 significantly reduces PWM jitter, allowing the control bandwidth in the range of 1/10th to 1/5th of the switching frequency.

Two types of compensators are commonly used: Type II (PI) and Type III (PID), as shown in Figure 8. The selection of the compensation type is dependent on the ESR of the output capacitors. Electrolytic capacitors have relatively higher ESR. If the ESR pole is located at a frequency lower than the cross-over frequency, FC, the ESR pole will help to boost the phase margin. Thus, a type II compensator can be used. For the output capacitors with lower ESR such as ceramic capacitors, type III compensation is often desired.

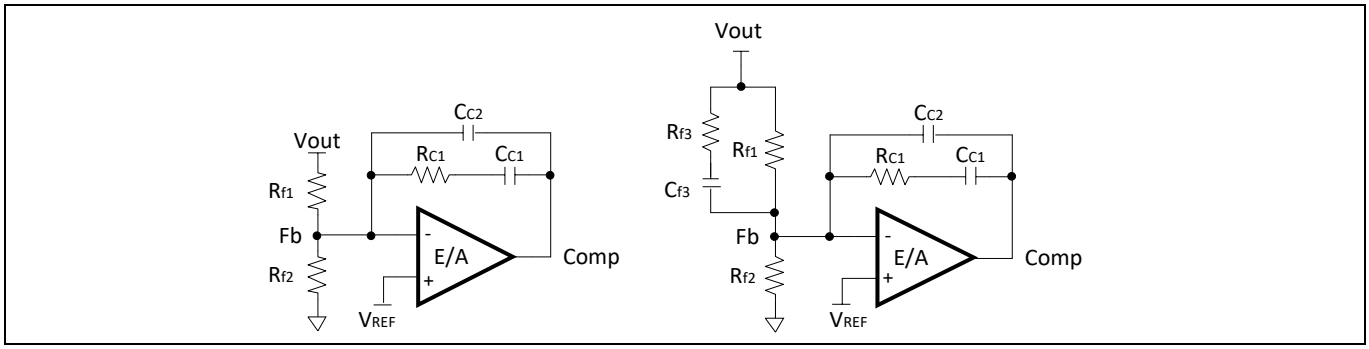


Figure 8 Loop Compensator: (Left) Type II, (Right) Type III

Table 8 lists the compensation selection for different types of output capacitors.

Design guidelines for voltage loop compensation can be found in application note AN-1162, "Compensation Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier". The Sup*IR*Buck design tool is also available at www.infineon.com providing a reference design based on the user's design requirements.

Table 8 Recommended Compensation Type

Compensator	Location of cross-over frequency	Type of output capacitors
Type II (PI)	$F_{LC}<F_{ESR}<F_0<F_S/2$	Electrolytic, POS-CAP, SP-CAP
Type III-A (PID)	$F_{LC}<F_0<F_{ESR}<F_S/2$	POS-CAP, SP-CAP
Type III-B (PID)	$F_{LC}<F_0<F_S/2<F_{ESR}$	Ceramic

F_{LC} is the resonant frequency of the output LC filter. It is often referred to as double pole.

$$F_{LC} = \frac{1}{2 \times \pi \sqrt{L_o \times C_o}}$$

F_{ESR} is the ESR zero of the output capacitor.

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_o}$$

F_0 is the cross-over frequency of the closed voltage loop and F_S is the switching frequency.

12.3 Under-Voltage Lockout and POR

The under-voltage lockout circuit monitors the voltage of Vcc/LDO_Out pin and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drops below the set thresholds. Normal operation resumes once Vcc/LDO_Out and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when these two signals reach the valid logic level (see system block diagram). When the POR is asserted, the soft start sequence starts (see soft start section).

12.4 Enable

The Enable adds another level of flexibility for startup. The Enable has a precise threshold, which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3826 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2 V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3826 does not turn on until the bus voltage reaches the desired level (Figure 9). Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold will the IR3826 be enabled. Therefore, in addition to being a logic input pin to enable the IR3826, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage (Pvin). This is desirable, particularly for high output voltage applications.

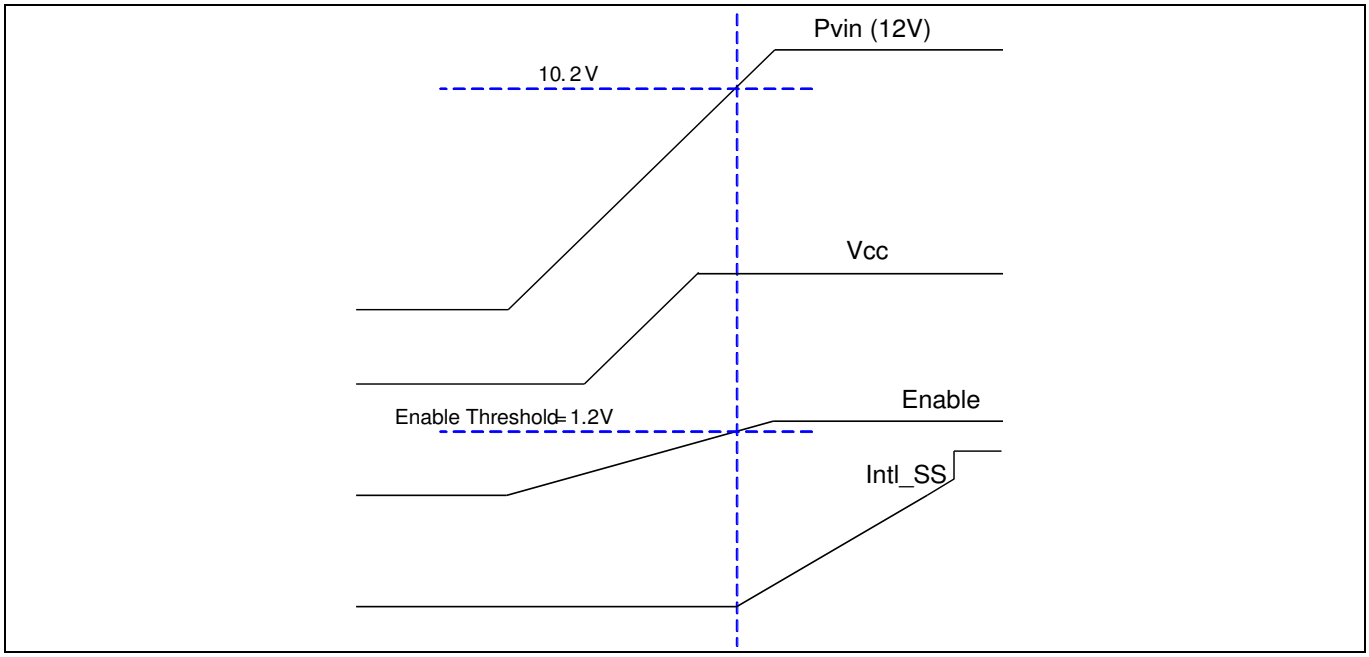


Figure 9 Normal start-up with En signal generated by a resistor divider from PVin.

Figure 9 illustrates the start-up sequence with a resistor divider used at EN pin from Pvin to turn on the device at 10.2 V. Figure 10 shows the recommended start-up sequence for the normal operation of IR3826, when Enable is used as a logic input.

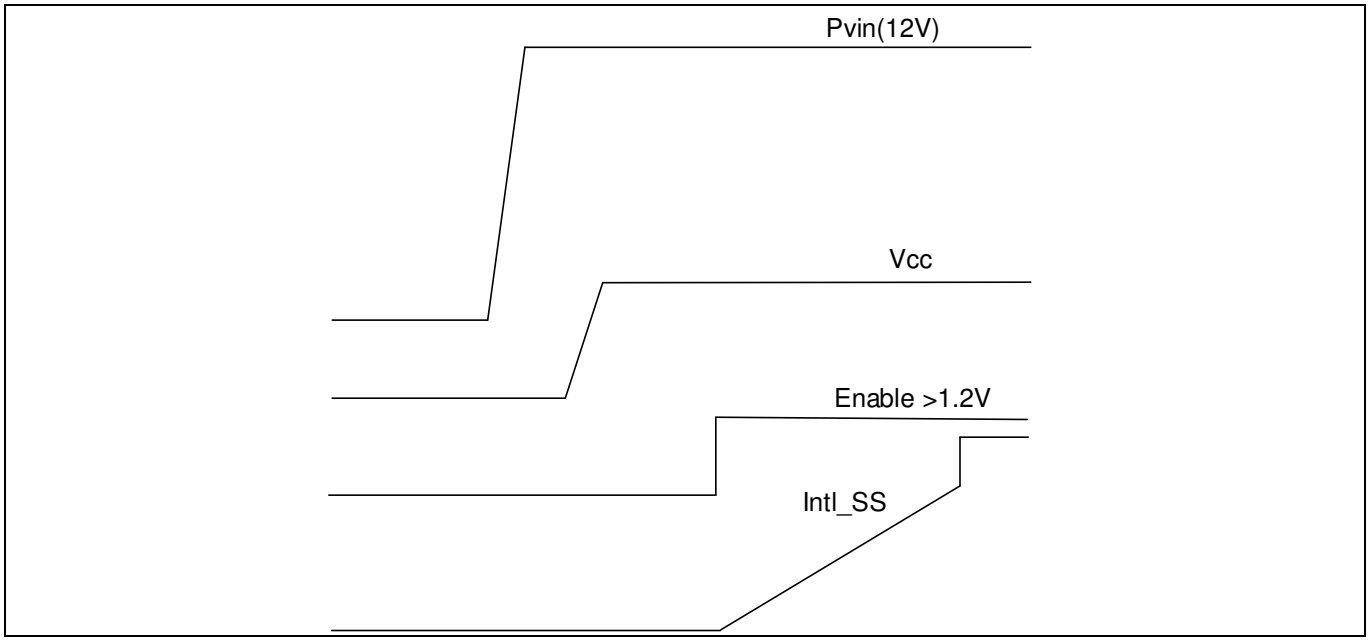


Figure 10 Normal start-up with a logic input for Enable signal

It is recommended to connect a 1 kΩ resistor in series with the Enable pin to limit the current flowing into the Enable pin. In addition, the Enable pin should not be left floating. A pull-down resistor in the range of several kilohms can be connected between the Enable Pin and Gnd. Note that this might create a resistor divider. Care must be taken to ensure the voltage at the En pin is sufficient to exceed the threshold.

12.5 Pre-Bias startup

The IR3826 is able to start up into pre-charged output, without oscillations or other disturbance of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET (sync FET) off until the first gate signal for the control MOSFET (ctrl FET) is generated. Figure 11 shows a typical pre-bias condition at start up.

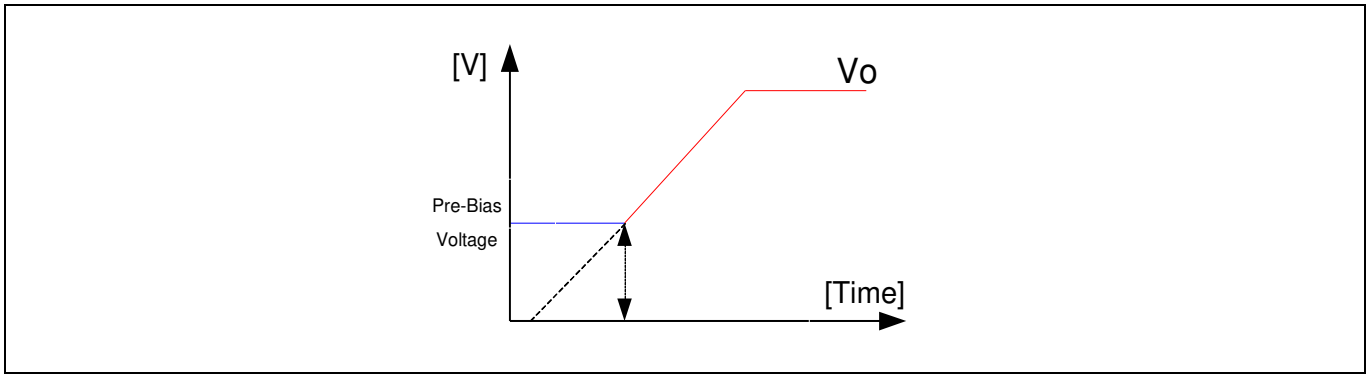


Figure 11 Pre-Bias startup

The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5% until it reaches the steady state value. There are 16 pulses in each step. This value is internally programmed. Figure 12 shows the series of 16x8 startup pulses.

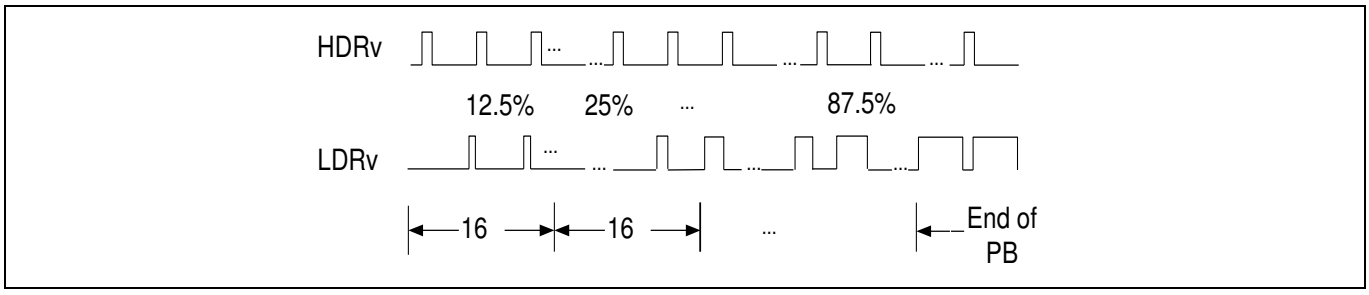


Figure 12 Pre-bias startup pulses

12.6 Soft-start

The IR3826 has an internal digital soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc voltages rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal soft-start (Intl_SS) signal linearly rises at the rate of 0.2 mV/µs from 0 V to 1.5 V, and then is pulled up to 3.0V. Figure 13 shows the waveforms during the soft-start. As shown in Figure 13, Vout starts to ramp up after the internal softstart signal rises above 0.15V, which results in an effective enable delay of (t2-t1). From t2 to t3, Vout ramps up with a fixed soft-start time equal to:

$$T_{start} = \frac{0.75\,\text{V} - 0.15\,\text{V}}{0.2\,\text{mV}/\mu\text{s}} = 3.0\,\text{ms}$$

During soft-start, Over-Current Protection (OCP) and Over-Voltage Protection (OVP) are enabled to protect the device for any short circuit or over voltage condition.

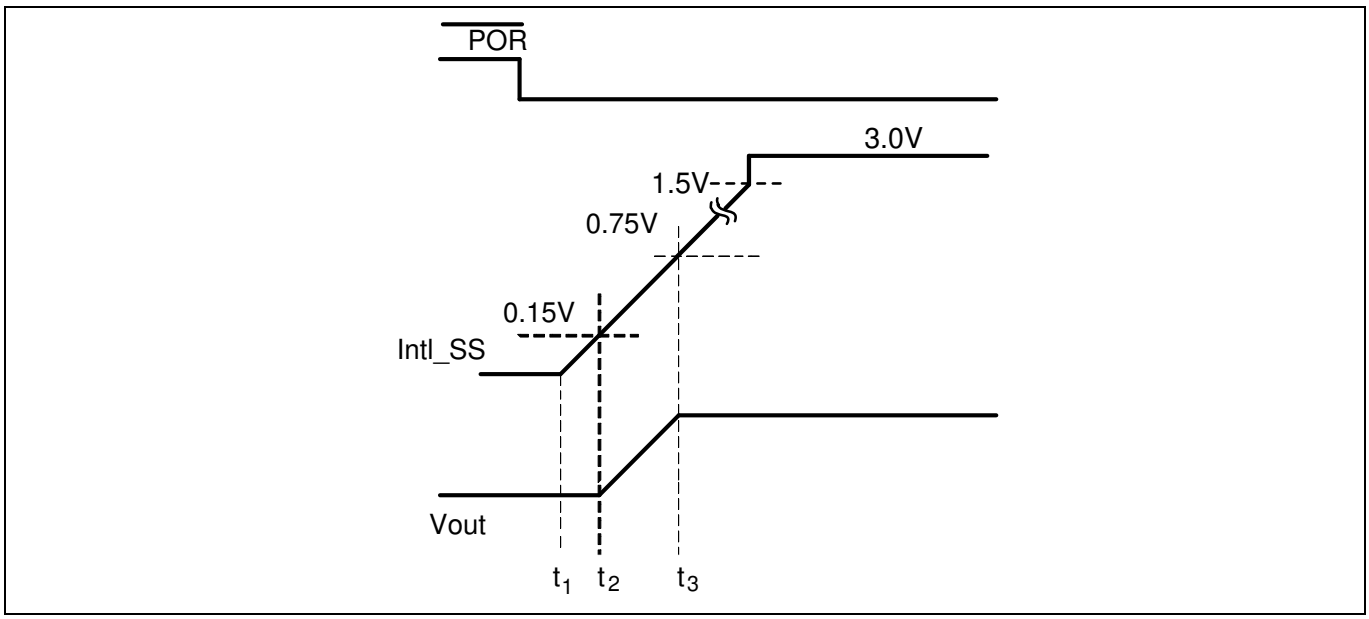


Figure 13 Theoretical waveforms during soft-start

12.7 Operating frequency

The switching frequency can be programmed between 300 kHz and 1500 kHz by connecting an external resistor from Rt pin to Gnd. Table 9 lists the Rt with each corresponding switching frequency.

Table 9 Switching Frequency (Fs) vs. External Resistor (Rt)

Rt (kΩ)	Freq (kHz)
80.6	300
60.4	400
48.7	500
39.2	600
34	700
29.4	800
26.1	900
23.2	1000
21	1100
19.1	1200
17.4	1300
16.2	1400
15	1500

12.8 Shutdown

The IR3826 can be shut down by pulling the Enable pin below its 1.0 V threshold. This will put both the high side and the low side FETs off.

12.9 Over Current Protection

Over Current Protection (OCP) is performed by sensing current through the $R_{DS(on)}$ of the synchronous MOSFET. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and minimizes the effect of any layout related noise issues. The Over Current (OC) limit can be set to one of three possible settings by floating the ILIM pin, by pulling up the ILIM pin to VCC, or by pulling down the ILIM pin to PGnd. The current limit is internally compensated according to the IC temperature, resulting in the over-current trip threshold remaining almost constant.

Note that the over current limit is affected by the Vcc voltage. In general, a lower Vcc voltage increases the $R_{DS(on)}$ of the Synchronous MOSFET and hence results in a lower OCP limit. Please refer to the typical performance curves of the OCP current limit with different Vcc voltages.

To prevent false tripping induced by noise and transients, the current near the valley of the inductor current is sensed by the Over Current Protection circuit. More precisely, the inductor current is sampled for about 40 ns on the downward inductor current slope approximately 12.5% of the switching period before the inductor current valley. When the current exceeds the OCP limit, an over current condition is detected.

When an Over Current event is detected, the Pgood signal is pulled low and the device enters hiccup mode. Hiccup mode is performed by latching an internal OC signal, which keeps both control FET and synchronous FET off for 20.48 ms (typical) blanking time. The OC signal clears after the completion of blanking time and the device attempts to recover to the nominal output voltage with a soft-start, as shown in Figure 14. The device will repeat hiccup mode and attempt to recover until the overload or short circuit condition is removed.

Since the current sensing point is near the valley of the inductor current, the actual DC output current limit point will be greater than the valley point by approximately one half of the peak to peak inductor ripple current. The DC current limit point can be calculated by the following equation. It should be pointed out that the OCP limits specified in the Electrical Table refer to the over current limit valley point.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta I}{2}$$

I_{OCP} = DC current limit hiccup point

I_{LIMIT} = Over Current limit (valley of inductor current)

ΔI = Inductor ripple current

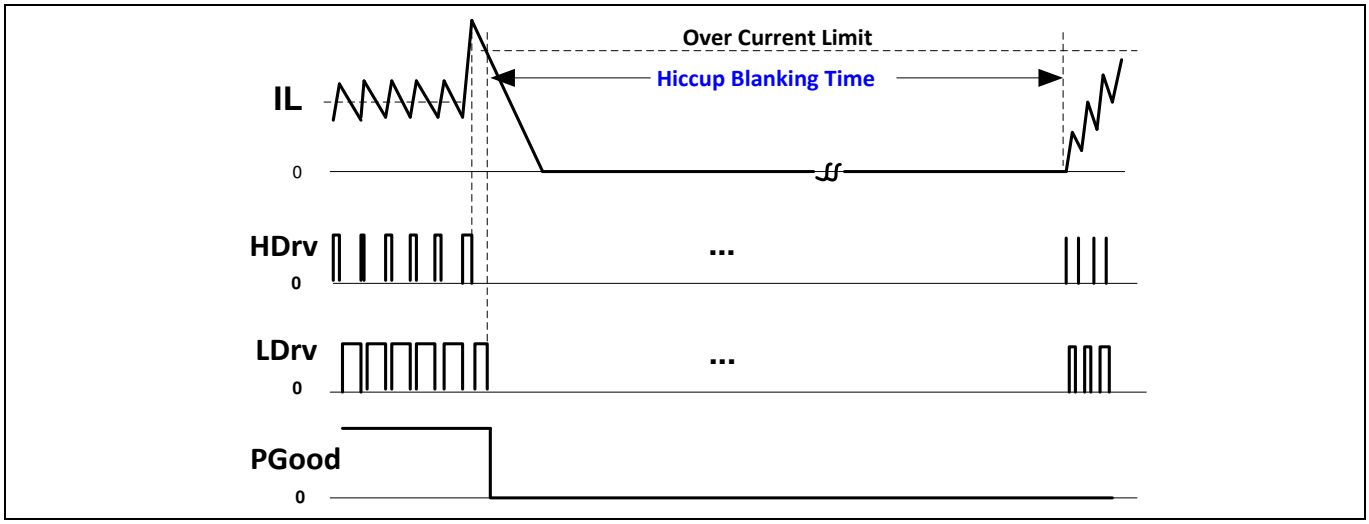


Figure 14 Timing diagram for current limit hiccup

12.10 Thermal shutdown

Temperature of the IC is measured internal to the IR3826. The trip threshold is typically set to 145 °C. When this threshold is exceeded, thermal shutdown turns off both MOSFETs and resets the internal soft start.

Automatic restart is initiated when the sensed temperature drops back into the operating range. There is a 20 °C hysteresis in the thermal shutdown threshold.

12.11 Feed-forward

Feed-forward is an important feature, because it can keep the converter stable and preserve its load transient performance when Vin varies in a large range. In the IR3826, the feedforward function is enabled when the Vin pin is connected to the Pvin pin. In this case, the internal low dropout (LDO) regulator is used. The PWM ramp amplitude (Vramp) is proportionally changed with the Vin to maintain Vin/Vramp almost constant throughout the Vin variation range (as shown in Figure 15). Thus, the control loop bandwidth and phase margin can be maintained constant. Feed-forward function can also minimize impact on output voltage if fast Vin transients occur. The maximum Vin slew rate is within 1 V/µs.

On IR3826, Vin signal signal is used for feedforward. If an external bias voltage is used as Vcc, the Vin pin should be connected to Vcc/LDO_out, therefore Vin signal does not follow Pvin anymore. This disables the feedforward function. Loop compensation parameters must be adjusted.

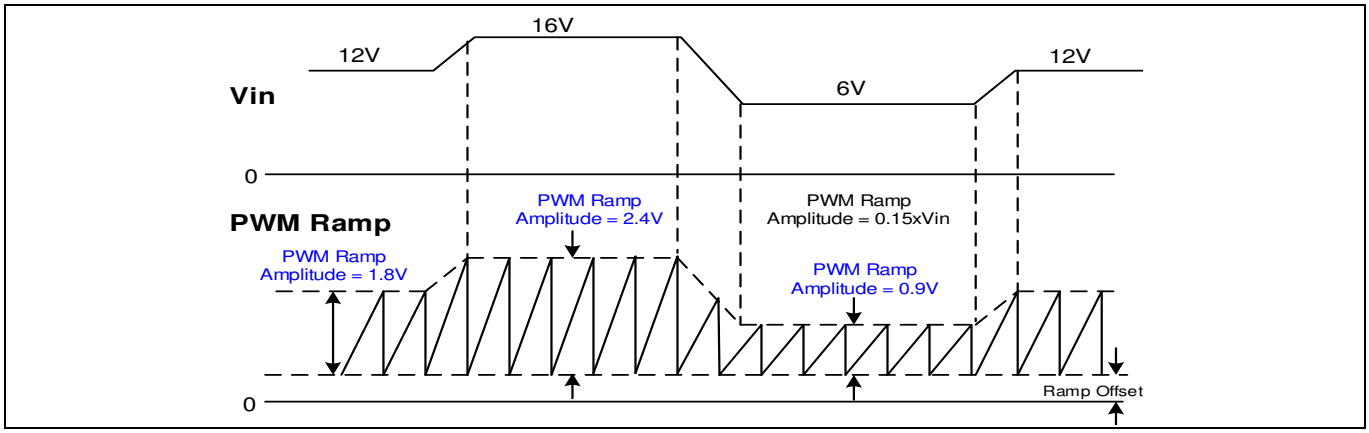


Figure 15 Timing diagram for feed-forward (F.F.) function

12.12 Low Dropout Regulator (LDO)

The IR3826 has an integrated low dropout (LDO) regulator which can provide gate drive voltage for both drivers.

For internally biased single rail operation, the Vin pin should be connected to Pvin, as shown in Figure 16. If an external bias voltage is used, the Vin pin should be connected to Vcc/LDO_Out, as shown in Figure 17. When the Vin voltage is below 6 V, the internal LDO may enter the dropout mode. The dropout voltage increases with the switching frequency.

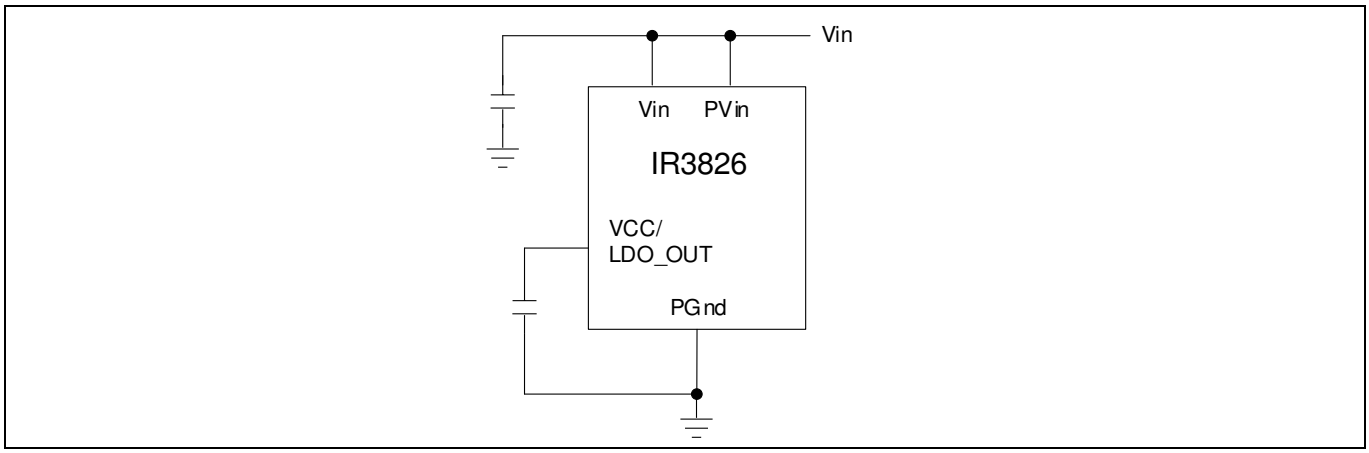


Figure 16 Internally biased single rail operation

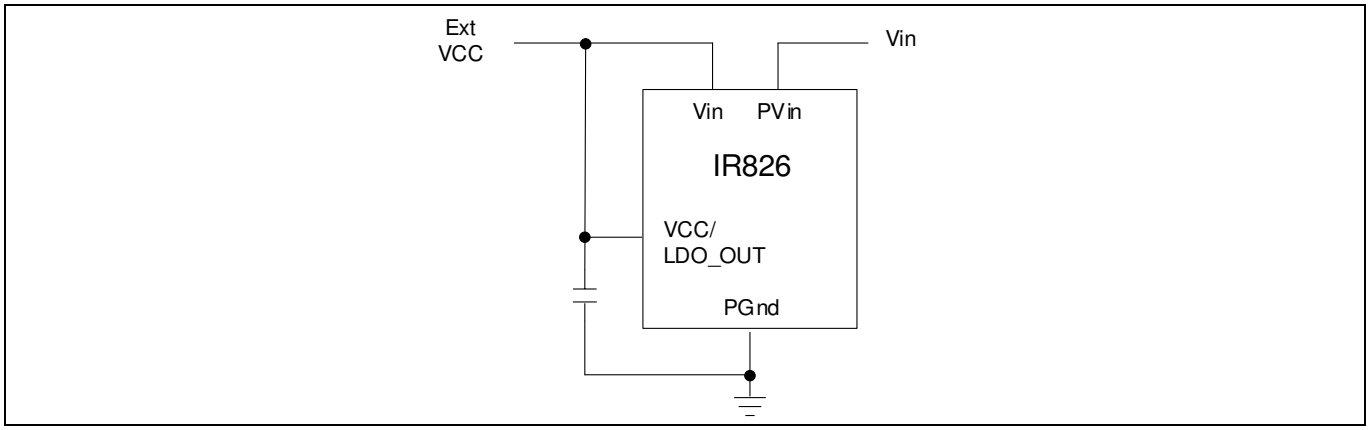


Figure 17 Use external bias voltage

12.13 Power Good Output

The IR3826 continually monitors the output voltage via the sense pin (Vsns). The Vsns voltage is an input to the window comparator with upper and lower turn-off threshold of 120% and 85% of the reference voltage, respectively. The Pgood signal is high whenever the Vsns voltage is within the Pgood comparator window thresholds. A high state indicates that output is in regulation.

Figure 18 shows the timing diagram of the Pgood signal. The Vsns signal is also used by OVP comparator for detecting output over voltage conditions. The Pgood is an open drain output, and pull-up resistor is needed to

limit the current flowing into the Pgood pin to be less than 5mA when the output voltage is not in regulation. A typical value used is 49.9 kΩ.

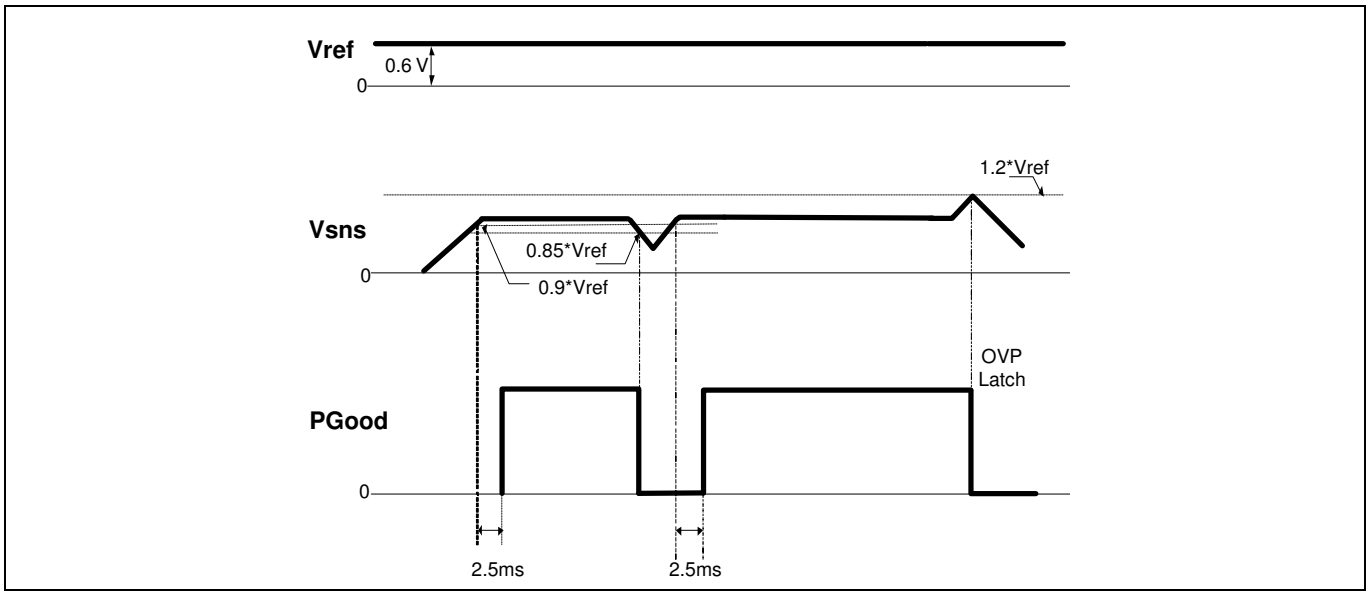


Figure 18 The relationship between Vsns and Pgood

12.14 Over-Voltage Protection (OVP)

OVP is achieved by comparing Vsns voltage to an OVP threshold voltage, 1.2×Vref. When Vsns exceeds the OVP threshold, an over voltage trip signal asserts after 2 µs (typical) delay. The control FET is latched off immediately and Pgood flags low. The sync FET remains on to discharge the output capacitor. When the Vsns voltage drops below the threshold, the sync FET turns off to prevent the complete depletion of the output capacitor. The control FET remains latched off until either Vcc or Enable signal is cycled.

The OVP comparator becomes active when the enable signal exceeds the start threshold. Vsns voltage is set by the voltage divider connected to the output and it can be programmed externally. Figure 19 shows the timing diagram for OVP in non-tracking mode.

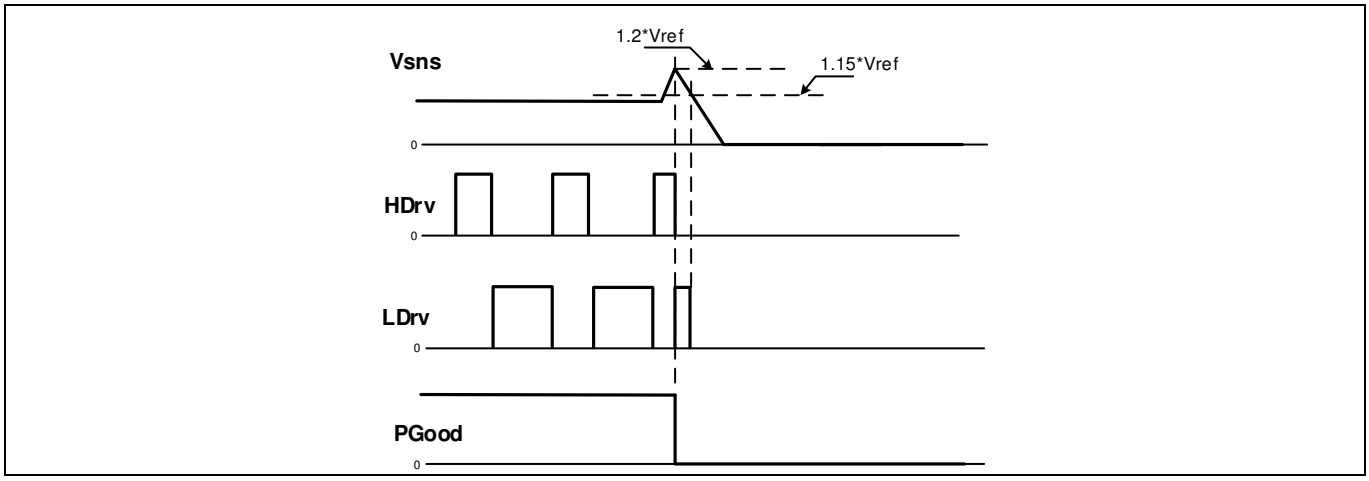


Figure 19 Timing diagram for OVP

12.15 Minimum On-Time Considerations

The minimum ON time is the shortest amount of time for the control FET to be reliably turned on. This is a very critical parameter for low duty cycle and high frequency applications. Conventional approaches limit the pulse width to prevent noise, jitter and pulse skipping. This results in lower closed loop bandwidth.

Infineon has developed a proprietary scheme to improve and enhance minimum pulse width which utilizes the benefits of voltage mode control with higher switching frequency, wider conversion ratio and higher closed loop bandwidth. This results in reduction of output capacitance requirements. System designers must ensure operation with a pulse width that is higher than this minimum on-time. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{V_{in} \times F_s}$$

In any application that uses IR3826, the following condition must be satisfied:

$$t_{on(\min)} \leq t_{on}$$

$$t_{on(\min)} \leq \frac{V_{out}}{V_{in} \times F_s}$$

$$V_{in} \times F_s \leq \frac{V_{out}}{t_{on(\min)}}$$

The minimum output voltage is limited by the reference voltage and hence Vout(min) = 0.6 V. Therefore, for Vout(min) = 0.6 V,

$$V_{in} \times F_s \leq \frac{V_{out}}{t_{on(\min)}} = \frac{0.6\,V}{60\,ns} = 10V/\mu s$$

At the maximum recommended input voltage of 17 V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 588 kHz. Conversely, for operation at the maximum recommended operating frequency (1.5 MHz) and minimum output voltage (0.6 V), the input voltage (Pvin) should not exceed 6.6 V, or pulse skipping will occur.

12.16 Maximum Duty Ratio

The IR3826 is designed to have a maximum duty ratio of 0.86 for most applications. In addition, there are two other factors that limit the maximum duty ratio. One is the minimum off-time, which is more dominant at high switching frequency. The other factor is the maximum output voltage of the error amplifier. Due to the built-in input voltage feedforward, the ramp voltage of the internal PWM modulator increases with Vin. However, the output of the error amplifier is clamped at the maximum voltage as specified in the electrical table, which can result in a max duty ratio smaller than 0.86 at high Vin. Figure 20 shows a plot of the maximum duty ratio vs. the switching frequency with built in input voltage feedforward.

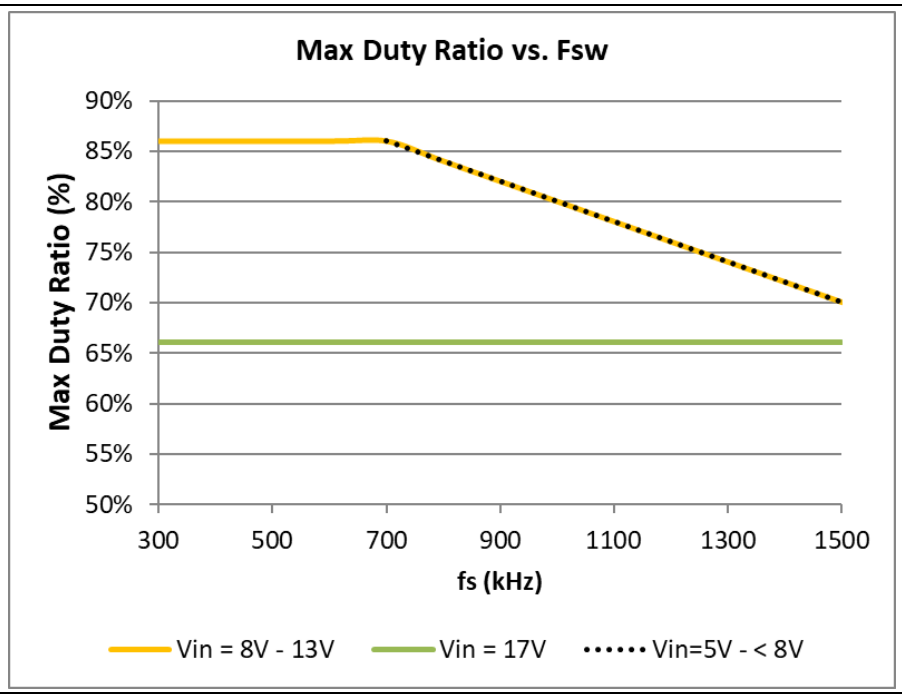


Figure 20 Maximum duty cycle vs. switching frequency with Vin feedforward

13 Design example

The following example is a typical application for the IR3826. The application circuit is shown in Figure 25.

PVin = Vin = 12 V (±10%)

Vo = 1.2 V

Io = 23 A

Peak-to-Peak Ripple Voltage = 1% of Vo

ΔVo = ± 4% of Vo (for 30% Load Transient)

Fs = 600 kHz

13.1 Enabling the IR3826

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage as shown in Figure 21.

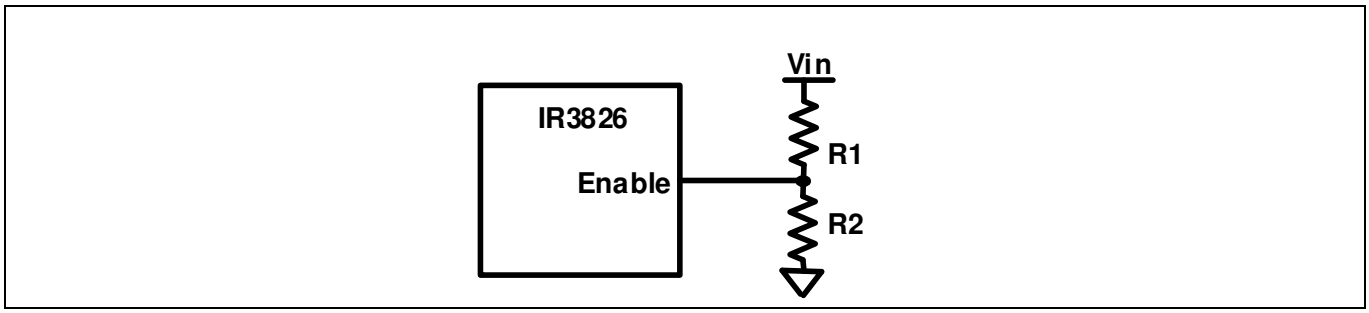


Figure 21 Using Enable pin for UVLO implementation for a typical Enable threshold of V_{EN} = 1.2 V

$$V_{in(\min)} \times \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2\text{V}$$

$$R_2 = R_1 \times \frac{V_{EN}}{V_{in(\min)} - V_{EN}}$$

For $V_{in\,(min)}$=9.2 V, R1=49.9 kΩ and R2=7.5 kΩ ohm is a good choice.

13.2 Programming the Frequency

For Fs = 600 kHz, select Rt = 39.2 kΩ, using Table 9.

13.3 Output Voltage Programming

Output voltage is programmed by the reference voltage and an external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.6 V. The divider ratio is set to provide 0.6 V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{ref} \times (1 + \frac{R_{F1}}{R_{F2}})$$

The external resistor divider is connected to the output as shown in Figure 22.

$$R_{F2} = R_{F1} \times \left(\frac{V_{ref}}{V_o - V_{ref}} \right)$$

Select R_{F1}=4.22 kΩ,

$$R_{F2} = 4.22 \times \left(\frac{0.6}{1.2 - 0.6} \right) = 4.22\ k\Omega$$

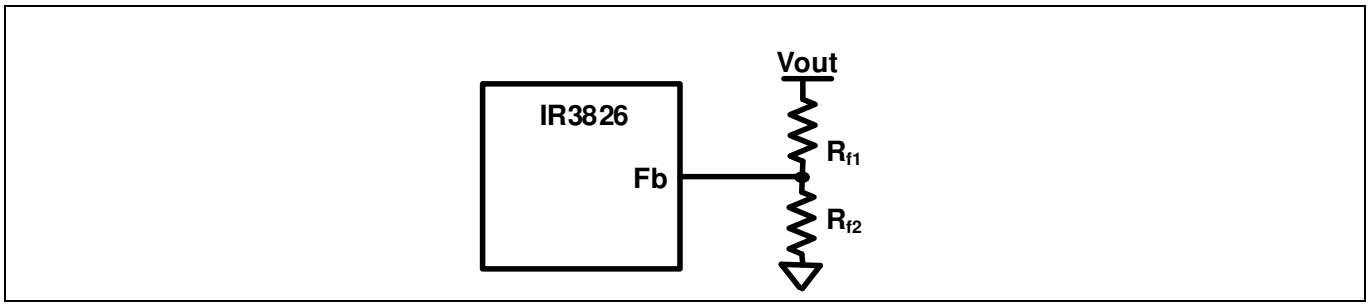


Figure 22 Typical application of the IR3826 for programming the output voltage

13.4 Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4 V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C1). The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards Vcc through the internal bootstrap diode (Figure 23), which has a forward voltage drop V_D. The voltage Vc across the bootstrap capacitor C1 is approximately given as:

$$V_C = V_{CC} - V_D$$

When the control FET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage Vin. However, if the value of C1 is appropriately chosen, the voltage Vc across C1 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{BOOT} = V_{in} + V_{CC} - V_D$$

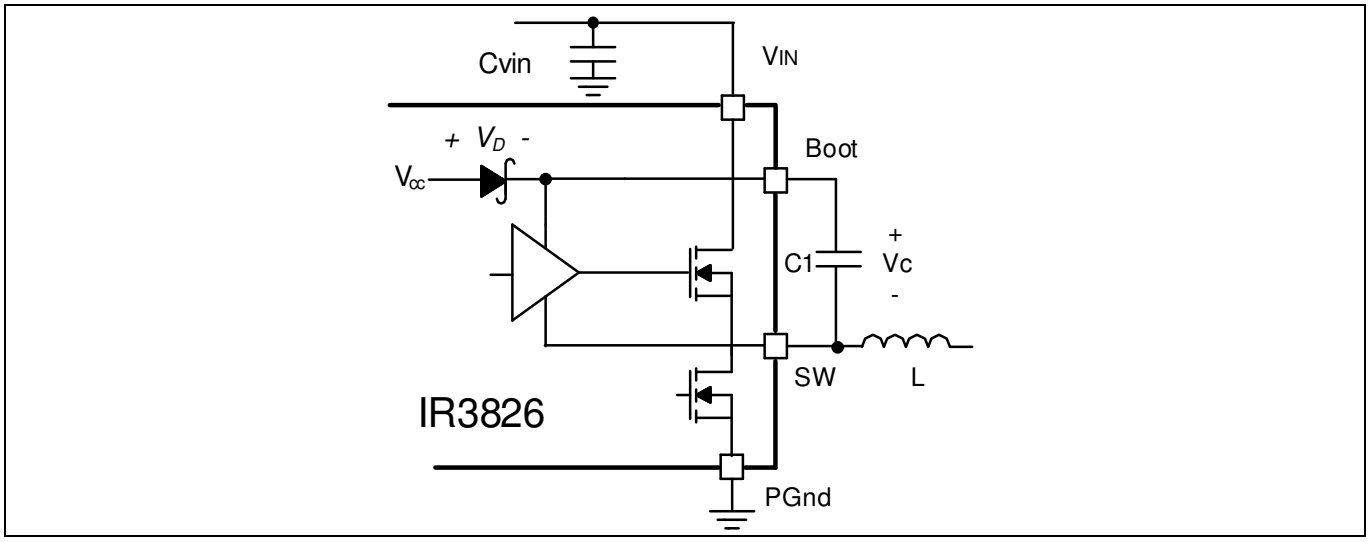


Figure 23 Bootstrap circuit to generate Vc voltage. A value 0.1 µF is suitable for most applications

13.5 Input Capacitor Selection

The ripple current generated during the on time of the control FET should be provided by the input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1-D)}$$

$$D = \frac{V_o}{V_{in}}$$

Where:

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current. Io is the output current.

For Io=23 A and D = 0.1, the I_{RMS} = 6.9 A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have eight 22 µF, 25V ceramic capacitors in 0805 package. In addition to these, although not mandatory, a single 330 µF, 25V electrolytic capacitor may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

13.6 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in smaller size and faster response to a load transient, but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (ΔiL). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$V_{in\max} - V_o = L \times \frac{\Delta i_L}{\Delta t}$$

$$\Delta t = \frac{D}{F_s}$$

$$L = (V_{in\max} - V_o) \times \frac{V_o}{V_{in} \times \Delta i_L \times F_s}$$

Where:

Vin = Maximum input voltage

Vo = Output Voltage

Δi = Inductor Peak-to-Peak Ripple Current

Fs = Switching Frequency

Δt = On time for Control FET

D = Duty Cycle

If Δi ≈ 35%*Io, then the output inductor is calculated to be 0.224 µH. Select L=0.21 µH for this application.

13.7 Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors' type and values. The criterion is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L \times ESR$$

$$\Delta V_{o(ESL)} = (\frac{V_{in} - V_o}{L}) \times ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 \times C_o \times F_s}$$

Where:

ΔV_0 = Output Voltage Ripple

ΔI_L = Inductor Ripple Current

Since the output capacitor has a major role in the overall performance of the converter and determines the transient response characteristics, selection of the capacitor is critical. The IR3826 can perform well with all types of capacitors. As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. In this case, ten 47 µF/6.3V/0805 ceramic capacitors are used. The ESR of this type of capacitor is around 3 mΩ each. The

de-rated capacitance value with 1.2 V dc bias and 10 mV ac voltage is around 32 µF each. It is also recommended to use a 0.1 µF ceramic capacitor at the output for high frequency filtering.

13.8 Feedback Compensation

For this design, the resonant frequency of the output LC filter, F_{LC}, is

$$F_{LC} = \frac{1}{2\times\pi\sqrt{L_o\times C_o}}$$
$$= \frac{1}{2\times\pi\sqrt{0.215\times10^{-6}\times10\times33\times10^{-6}}}$$
$$= 19\text{kHz}$$

The equivalent ESR zero of the output capacitors, F_{ESR}, is.

$$F_{ESR} = \frac{1}{2\pi\times ESR\times C_o}$$
$$= \frac{1}{2\pi\times0.3\times10^{-3}\times33\times10^{-6}}$$
$$= 1.24\ \text{MHz}$$

Designing crossover frequency around 1/7th of switching frequency gives F_0=80 kHz.

According to Table 8, Type III B compensation is selected for $F_{LC}<F_0<F_S/2<F_{ESR}$. Type III compensator is shown below for easy reference.

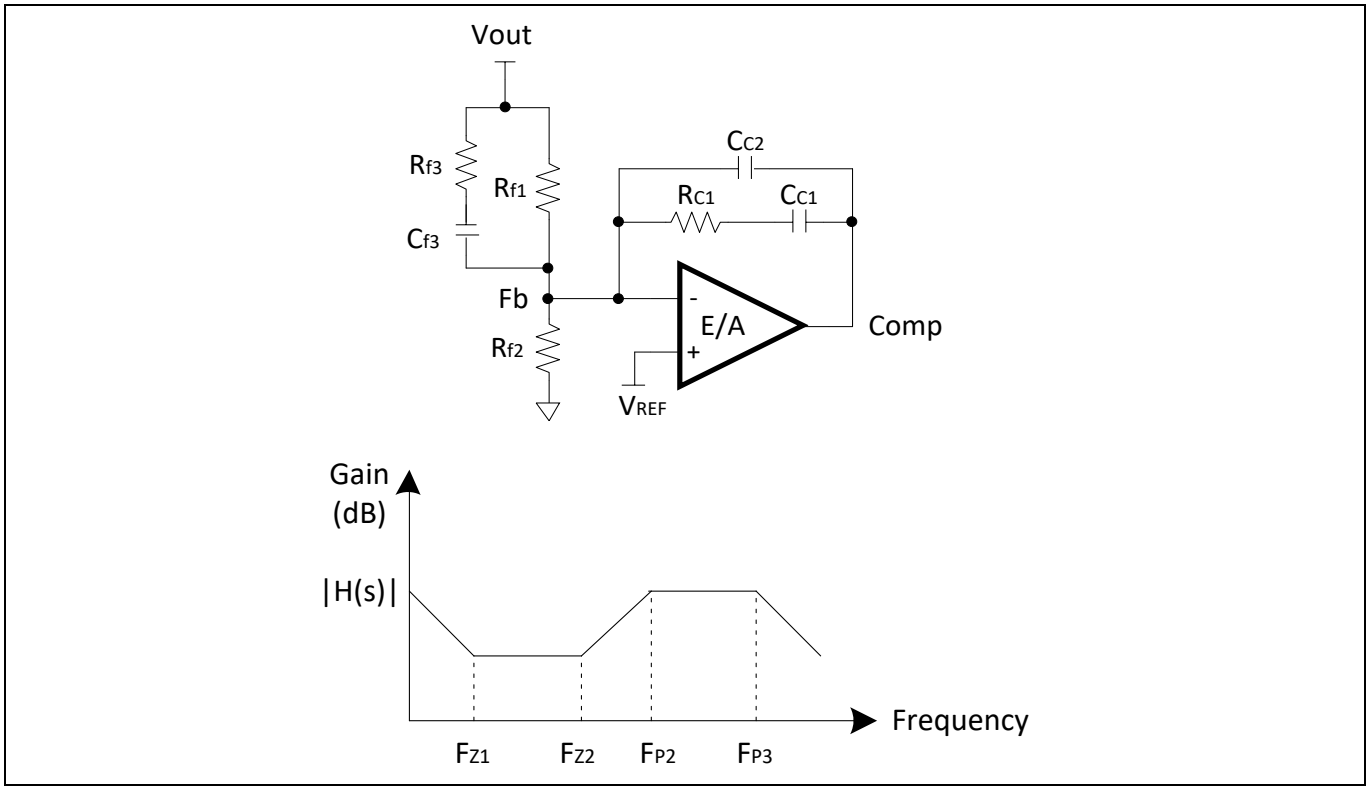


Figure 24 Type III compensation and its asymptotic gain plot

As can be seen from Figure 24, Type III compensator contains two zeros and three poles. They can be calculated as follows.

The zeros are:

$$F_{Z1} = \frac{1}{2\pi \times R_{C1} \times C_{C1}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{F3} \times (R_{F3} + R_{F1})}$$

The poles are:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_{F3} \times C_{F3}}$$

$$F_{P3} = \frac{1}{2\pi \times R_{C1} \times C_{C2}}$$

To achieve sufficient phase boost near the cross-over frequency, it is desired to place one zero and one pole as follows:

$$F_{Z2} = F_0 \sqrt{\frac{1-\sin\theta}{1+\sin\theta}} = 80 \times 10^3 \sqrt{\frac{1-\sin 75}{1+\sin 75}} = 10.53\text{kHz}$$

$$F_{P2} = F_0 \sqrt{\frac{1+\sin\theta}{1-\sin\theta}} = 80 \times 10^3 \sqrt{\frac{1+\sin 75}{1-\sin 75}} = 607\text{kHz}$$

To compensate the phase lag of the pole at the origin and to provide extra phase boost, the other zero could be placed at one half of the calculated zero above, i.e. F_{Z1} = 5.27 kHz. The third pole is usually placed at one half of the switching frequency to damp the switching noise. i.e. F_{p3} = 300 kHz.

Please note that the actual zero and pole locations can be fine tuned based on the calculated values. The selected compensation parameters are: R_{F1}=4.22 kΩ, R_{F2}=4.22 kΩ, R_{F3}=100 Ω, C_{F3}=2200 pF, R_{C1}=2.61 kΩ, C_{C1}=8.2nF, C_{C2}=160 pF. Finally, select the Vsns resistor divider to the same ratio of R_{F1}/R_{F2} to ensure the proper OVP and Pgood operations.

13.9 Application Diagram

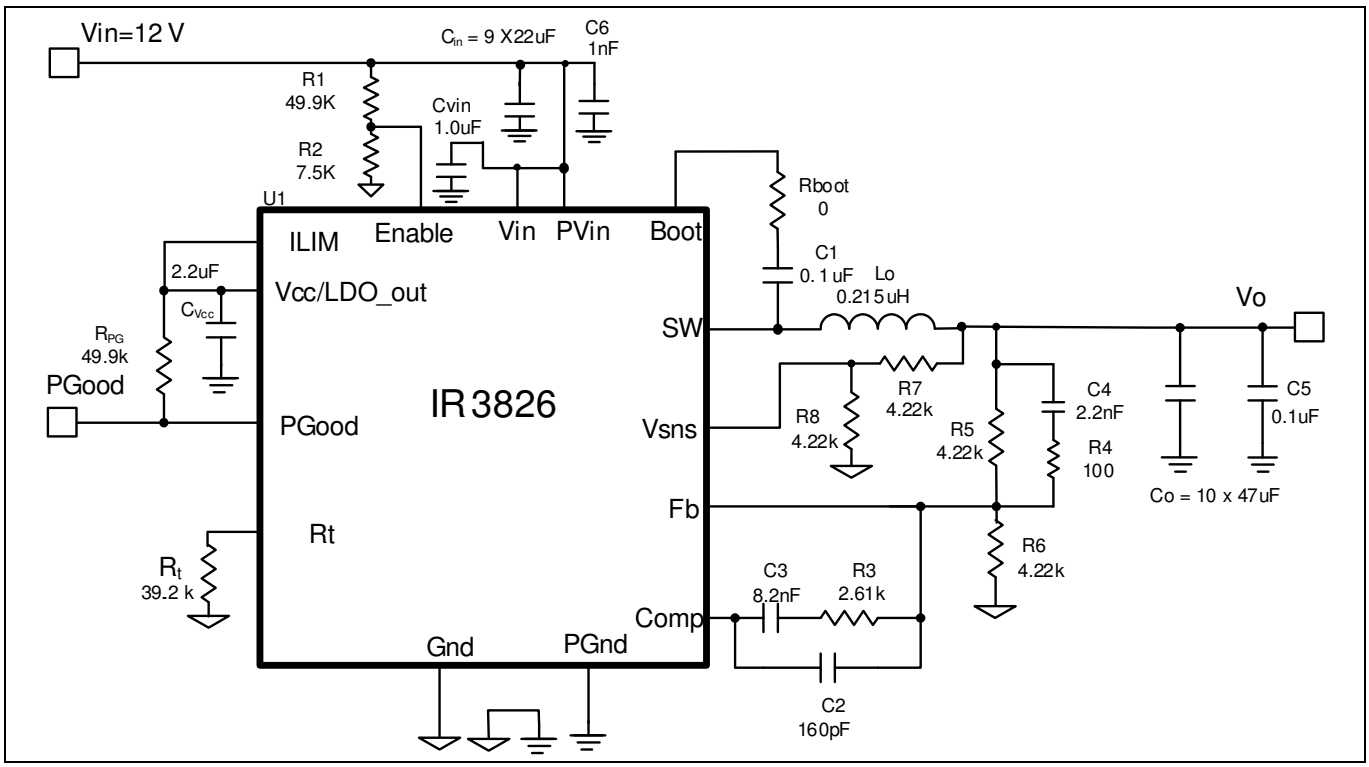


Figure 25 Application circuit for a 12 V to 1.2 V, 23 A point of load converter

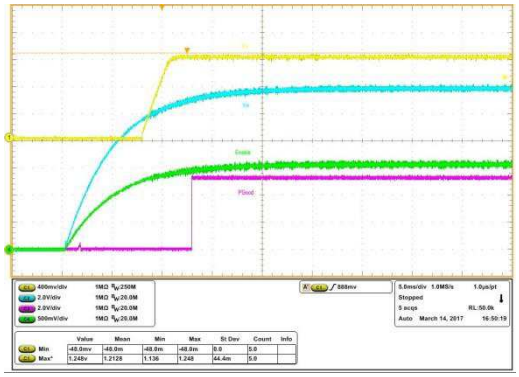
13.10 Suggested Bill of Materials for the Application Circuit

Part Reference	Qty	Value	Description	Manufacturer	Part Number
Cin	1	330 µF	SMD Electrolytic F size 25 V 20%	Panasonic	EEV-FK1E331P
	9	22 µF	CAP CER 22 µF 25 V 20% X5R 0805	Murata	GRM21BR61E226ME44L
C6	1	1 nF	CAP CER 1000 pF 16 V 10% X7R 0603	Murata	GRM188R71C102KA01D
C1 C5	2	0.1 µF	0402, 25 V, X7R, 10%	Murata	GRM155R71E104KE14J
C4	1	2200 pF	CAP CER 2200 pF 50 V 10% X7R 0402	Murata	GRM155R71H222KA01D
C2	1	160 pF	CAP CER 160 pF 50 V 5% NP0 0402	Murata	GRM1555C1H161JA01D
Co	10	47 µF	0805, 6.3 V, X5R, 20%	TDK	C2012X5R0J476M125AC
CVcc	1	2.2 µF	0603, 16 V, X5R, 10%	Murata	GRM188R61C225KE15D
C3	1	8.2 nF	CAP CER 8200 pF 25 V 10% X7R 0402	Murata	GRM155R71E822KA01D
Cvin	1	1.0 µF	0402, 25 V, X5R, 10%	Murata	GRM155R61E105KA12D
Lo	1	0.215uH	SMD 10.4 x 8.0 x 7.5 mm,0.29 mΩ	Delta	HCB1075N-211
R3	1	2.61k	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF2611X
R5 R6 R7 R8	4	4.22K	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF4221X
R4	1	100	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF1000X

Rt	1	39.2 kΩ	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF3922X
Rboot	1	0 Ohm	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2GE0R00X
R1 Rpg	2	49.9 kΩ	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF4992X
R2	1	7.5 kΩ	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF7501X
U1	1	IR3826	PQFN 6 mm x 5 mm	Infineon	IR3826MPBF

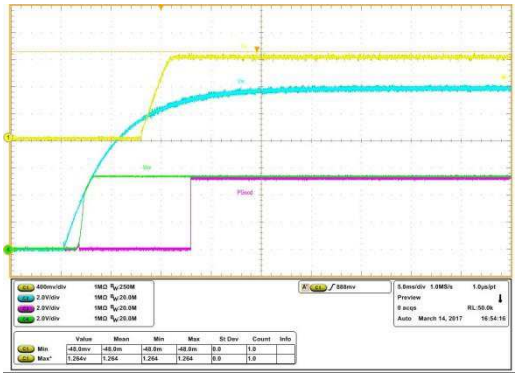
14 Typical Operating Waveforms

Vin=12.0 V, Vout=1.2 V, Iout=0-23 A, room temperature, Natural Convection



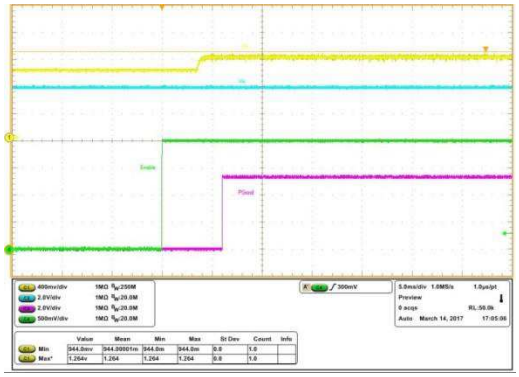
Start up at 23 A Load

Ch1:V_{out}, Ch2:PV_{in}, Ch3: P_{Good}, Ch4:Enable



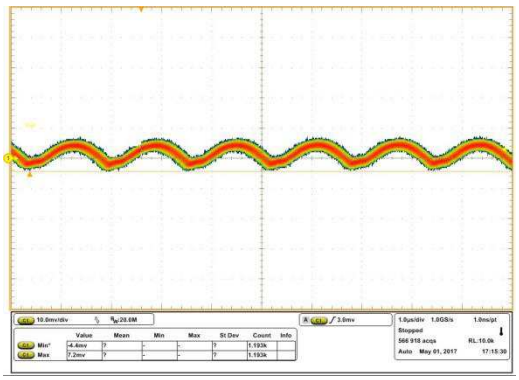
Start up at 23 A Load

Ch1:V_{out}, Ch2:PV_{in}, Ch3:P_{Good}, Ch4: V_{cc}



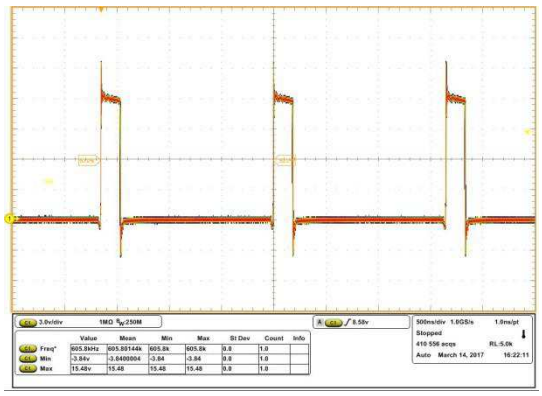
Start up with pre bias, 0 A Load

Ch1: V_{out}, Ch_2:PV_{in}, Ch_3:P_{Good},Ch_4:Enable



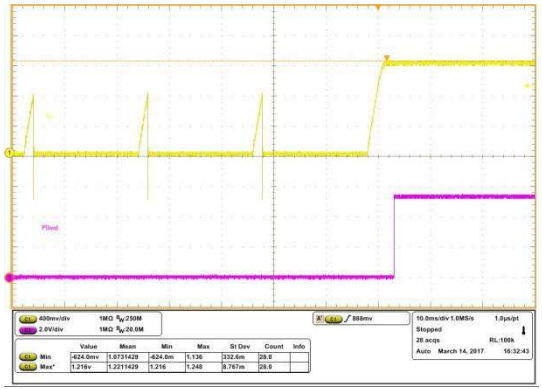
Output voltage ripple, 23 A load

Ch1: Vout, peak-to-peak $V_{o\text{-}ripple}$ = 11.6mV



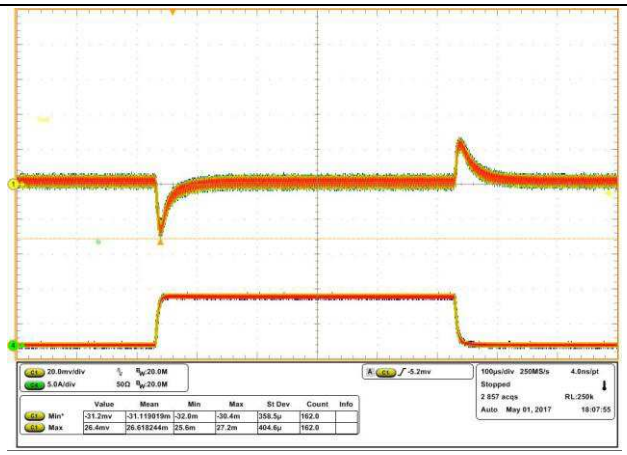
Inductor node at 23 A load

Ch1:Switch Node

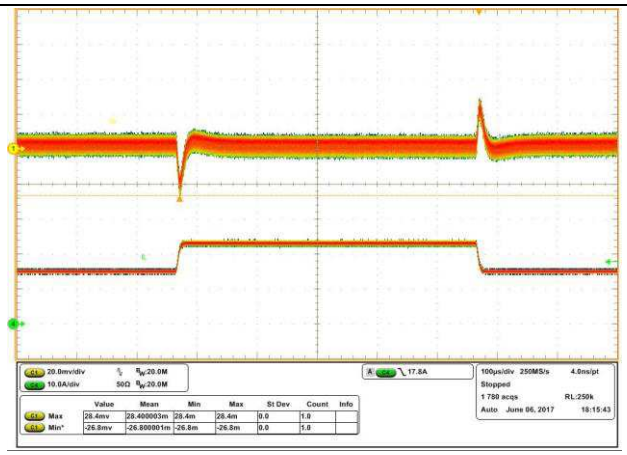


Short circuit (hiccup) recovery

Ch1:V_{out} , Ch_3:P_{Good}



Transient response with Io= 0 A – 7 A and slew rate of 2.5 A/µs, Overshoot = 26.4mV, Undershoot = -31.2mV
Ch1:Vout Ch4:Iout



Transient response with Io= 15 A – 23 A and slew rate of 2.5 A/µs, Overshoot = 28.4mV, Undershoot = -26.8mV
Ch1:Vout Ch4:Iout

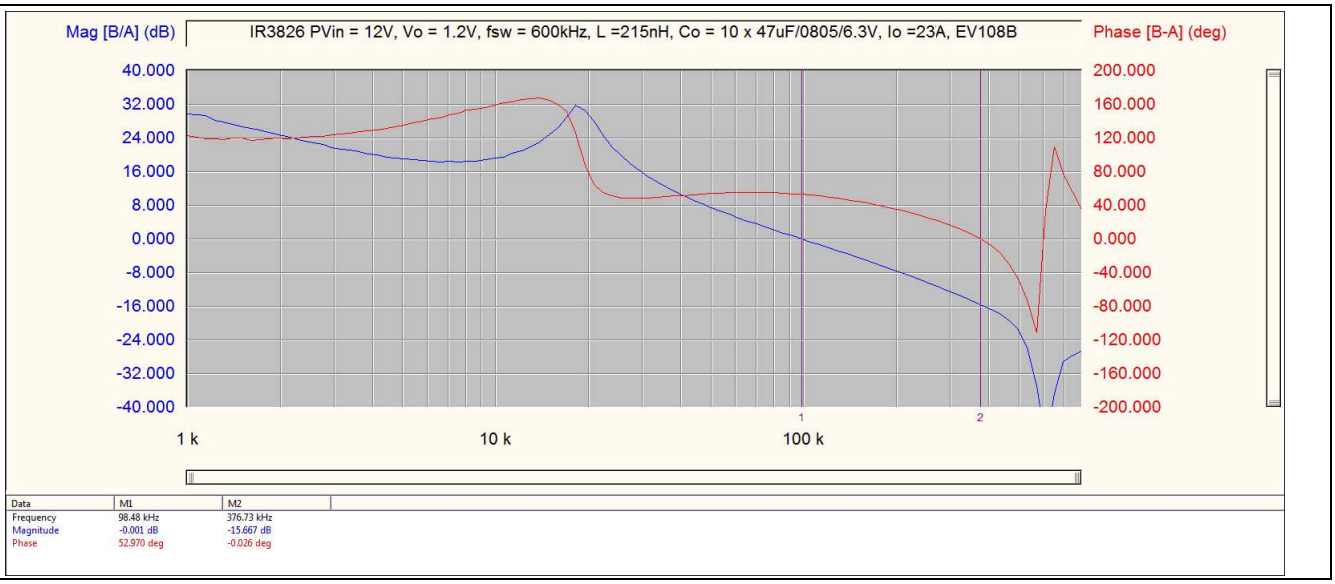


Figure 26 Bode plot of IR3826 at 23 A load shows a bandwidth of 98 kHz, phase margin of 53° and gain margin of -15 dB

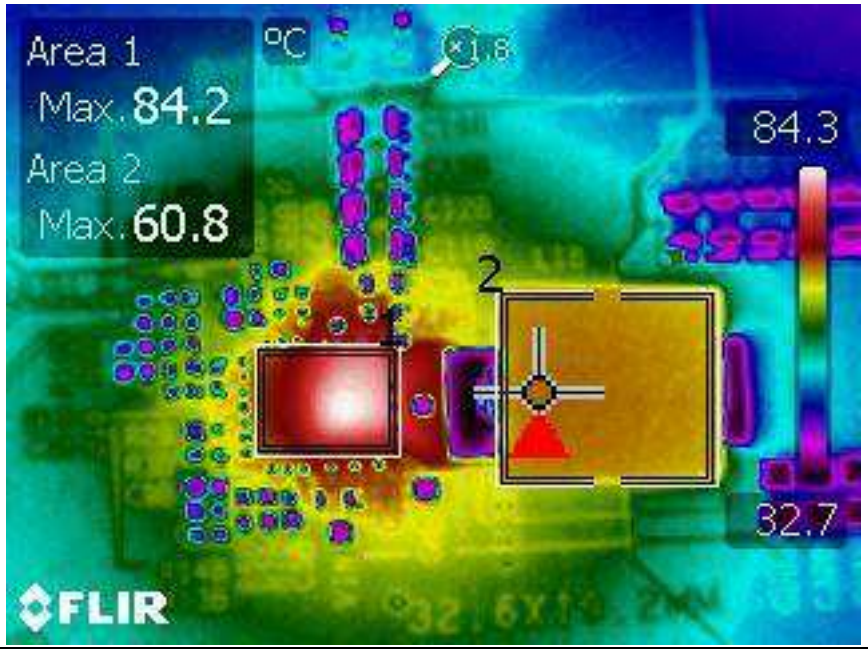


Figure 27 **Thermal image of the IR3826 demo board at 23 A load, room temperature, natural convection. Max Temperature of IR3826 = 84.2 °C, L=61°C.**

15 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make the connections for the power components on the top layer with wide, copper filled areas or shapes. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The inductor, output capacitors and the IR3826 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PVin pin of IR3826. The feedback part of the system should be kept away from the inductor and other noise sources. The critical bypass components such as capacitors for Vin and Vcc should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB, use at least one layer as a power ground plane. It is not necessary to have a dedicated analog ground plane. However it is important to have sensitive analog signals referenced to a quiet ground location, avoiding the interference with the high current loop.

The Power QFN is a thermally enhanced package. To effectively remove heat from the device the exposed pad should be connected to the ground plane using via holes. Figure 28 - Figure 33 illustrate the implementation of the layout guidelines outlined above, on the IRDC3826 6-layer demo board.

As shown in the PCB layout:

- Allow enough copper for PVin, GND and Vout
- All bypass capacitors are placed as close as possible to their connecting pins
- Components for loop compensation are placed as close as possible to the COMP pin
- AGND is connected to the inner PGND plane through via holes
- Resistor Rt is placed as close as possible to the Rt pin
- SW node copper should only be routed on the top layer to minimize switching noises
- Fb and Vsns trace routing are kept away from SW node
- Thermal via holes are placed on PVIN and PGND pads to aid thermal dissipation

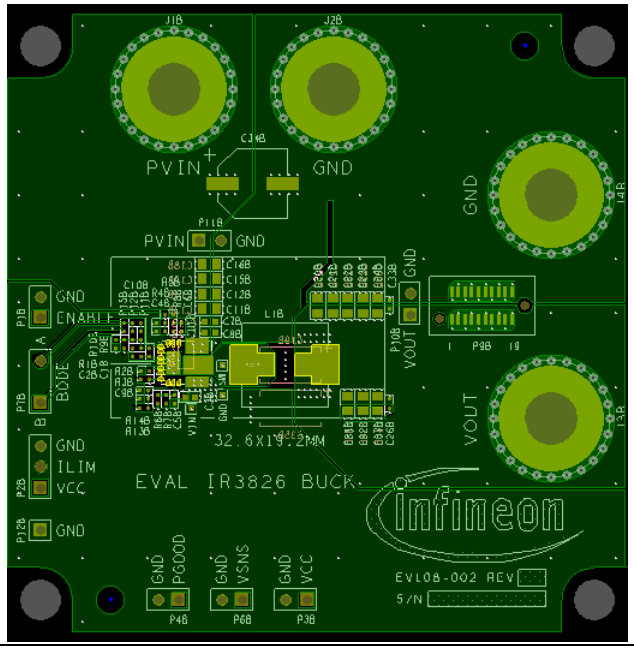


Figure 28 IRDC3826 Demo Board – Top Layer

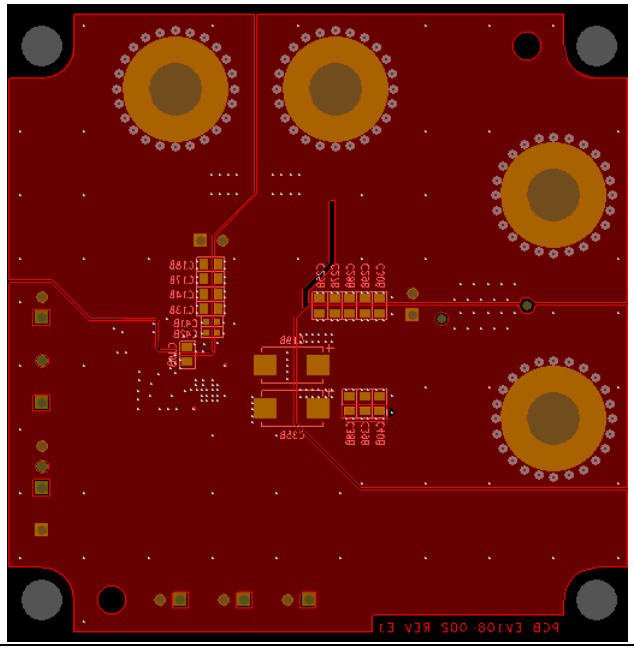


Figure 29 IRDC3826 Demo Board – Bottom Layer

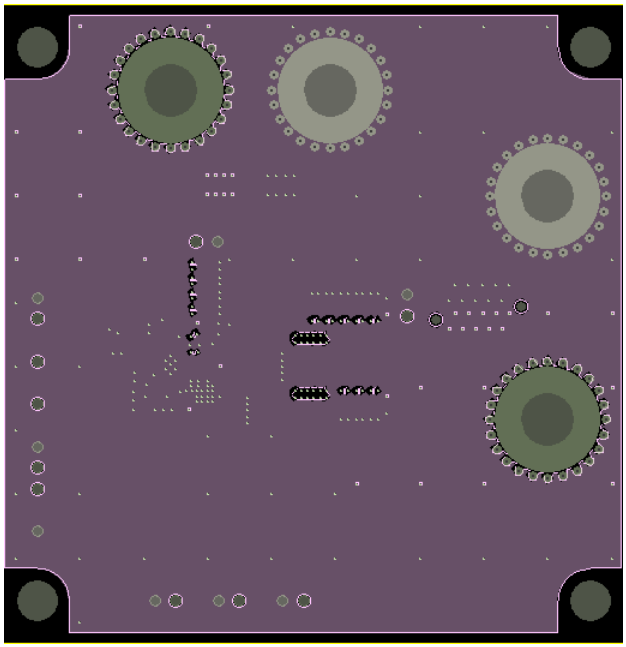


Figure 30 IRDC3826 Demo Board – Middle Layer 1 (Ground)

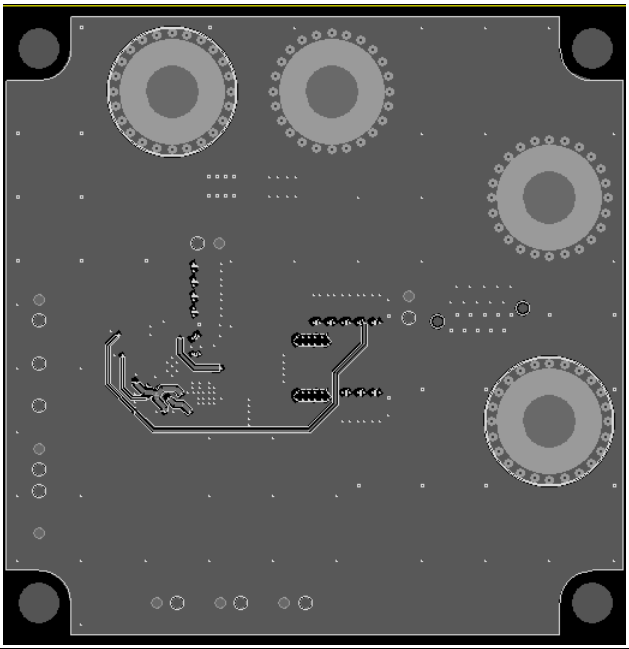


Figure 31 IRDC3826 Demo Board – Middle Layer 2 (Ground & Signal)

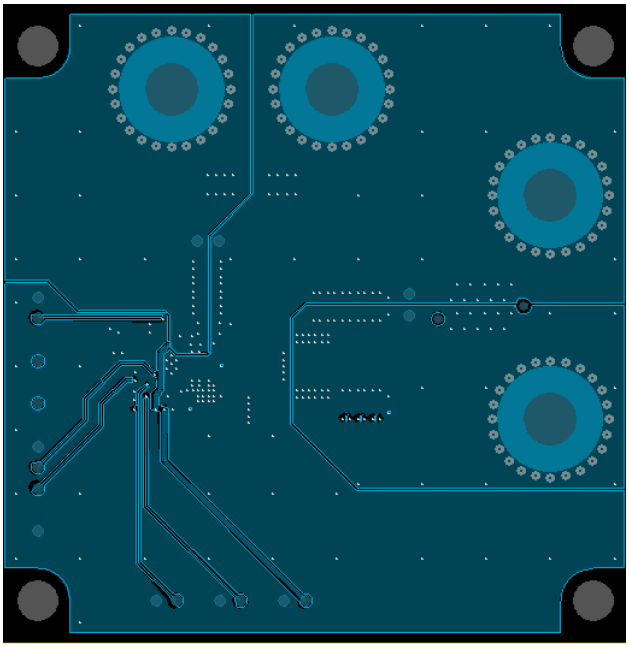


Figure 32 IRDC3826 Demo Board – Middle Layer 3 (Ground & Signal)

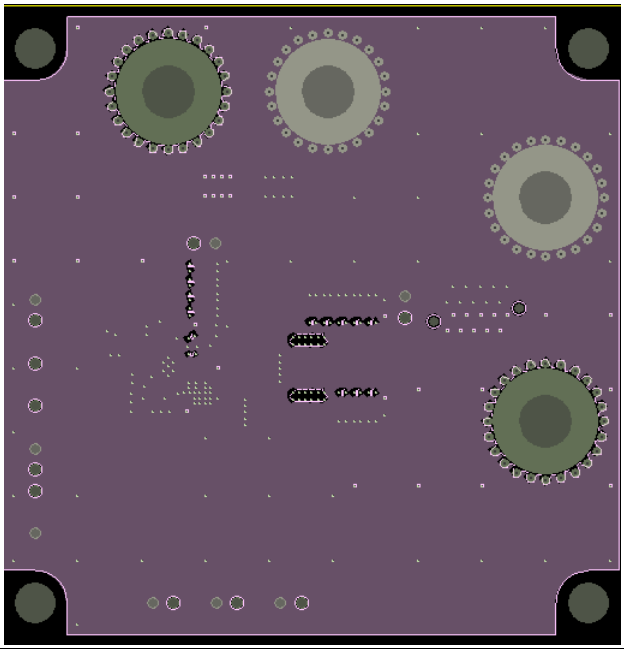


Figure 33 IRDC3826 Demo Board – Middle Layer 4 (Ground)

15.1 PCB Metal and Solder Mask

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resist in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

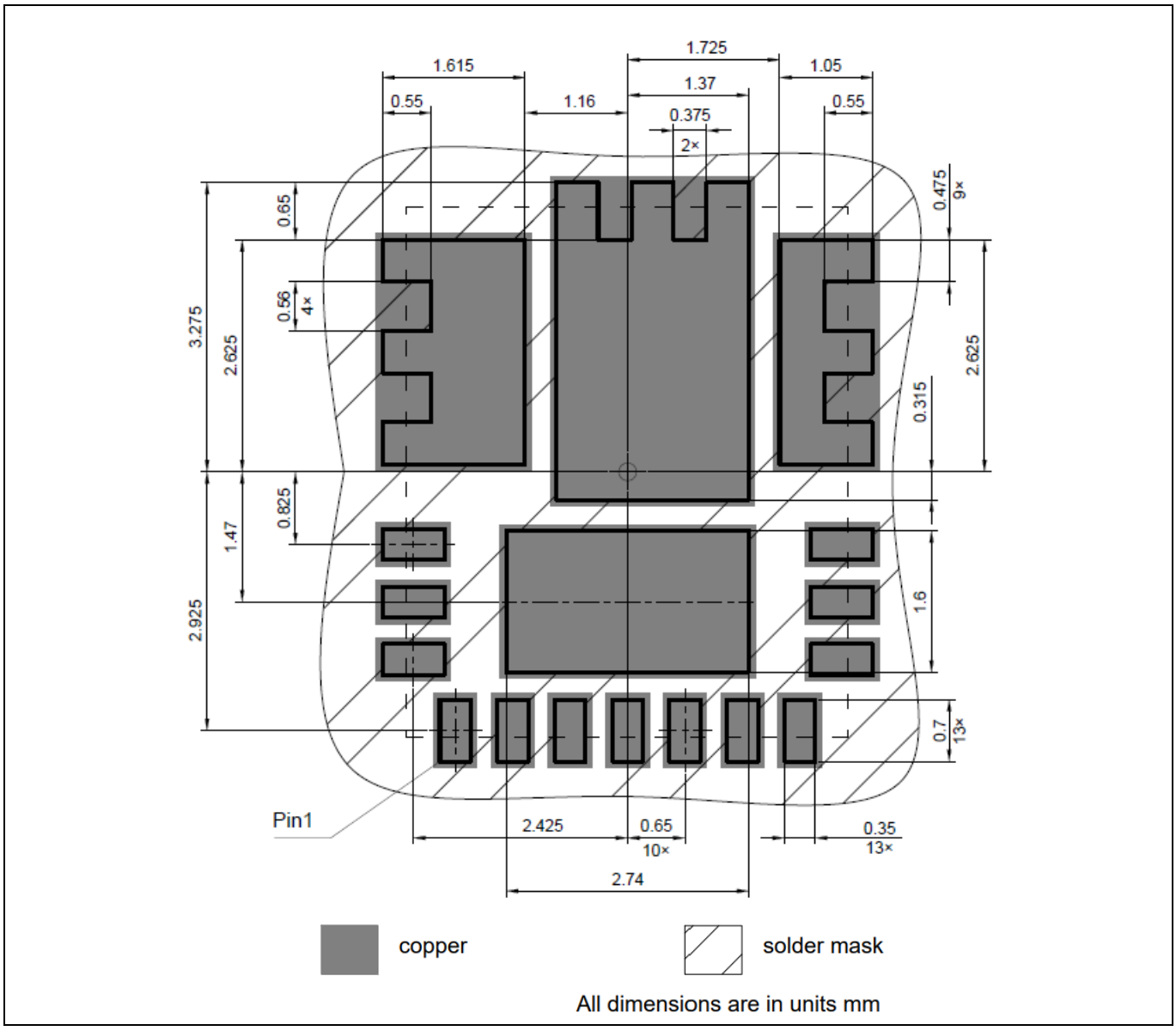


Figure 34 Solder mask (all dimensions in mm)

15.2 Stencil Design

Stencils for PQFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010”). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008”), with suitable reductions, give the best results. A recommended stencil design is shown below. This design is for a stencil thickness of 0.127 mm (0.005”). The reduction should be adjusted for stencils of other thicknesses.

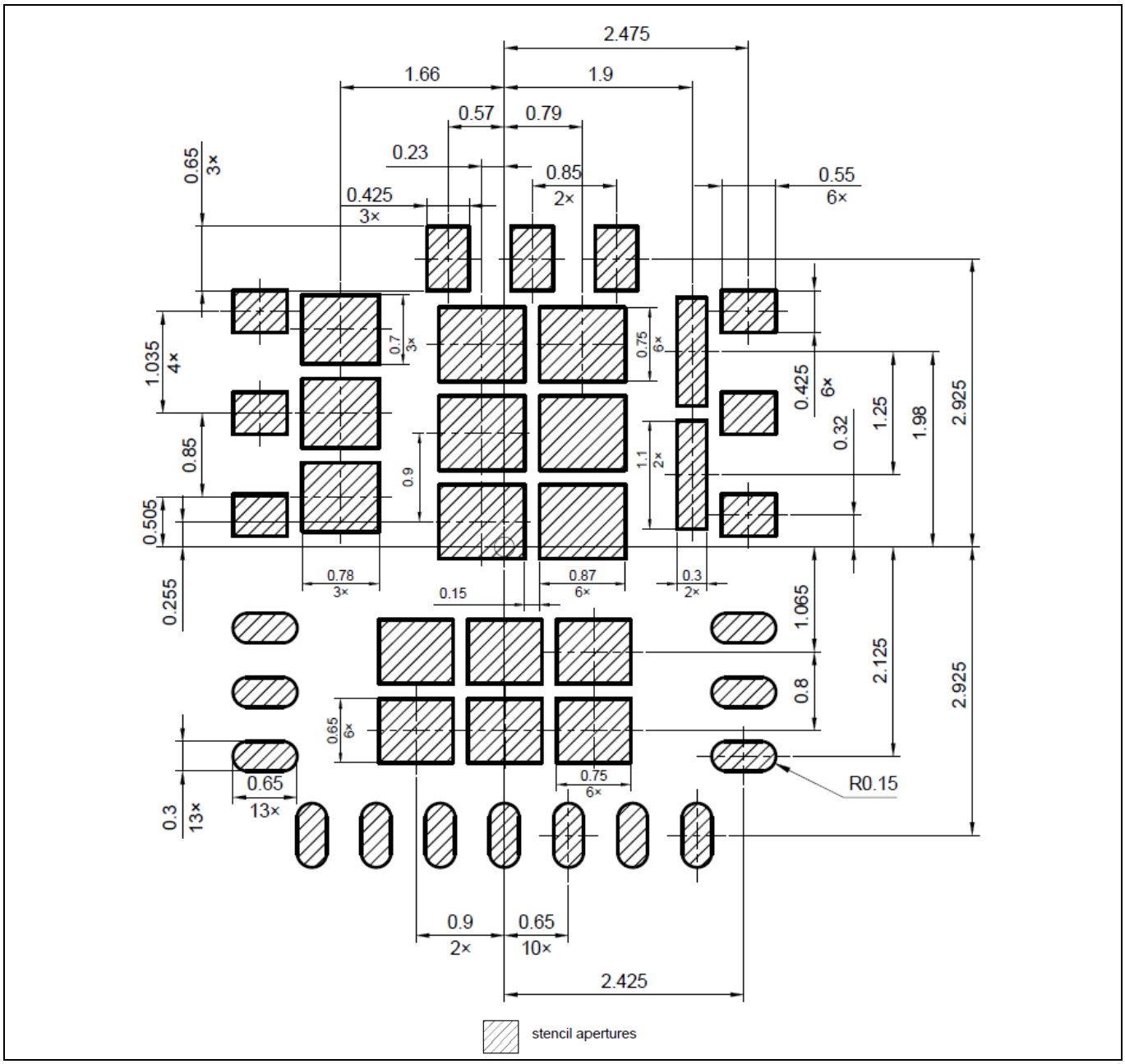


Figure 35 Stencil pad size and spacing (all dimensions in mm)

16 Package

16.1 Marking Information

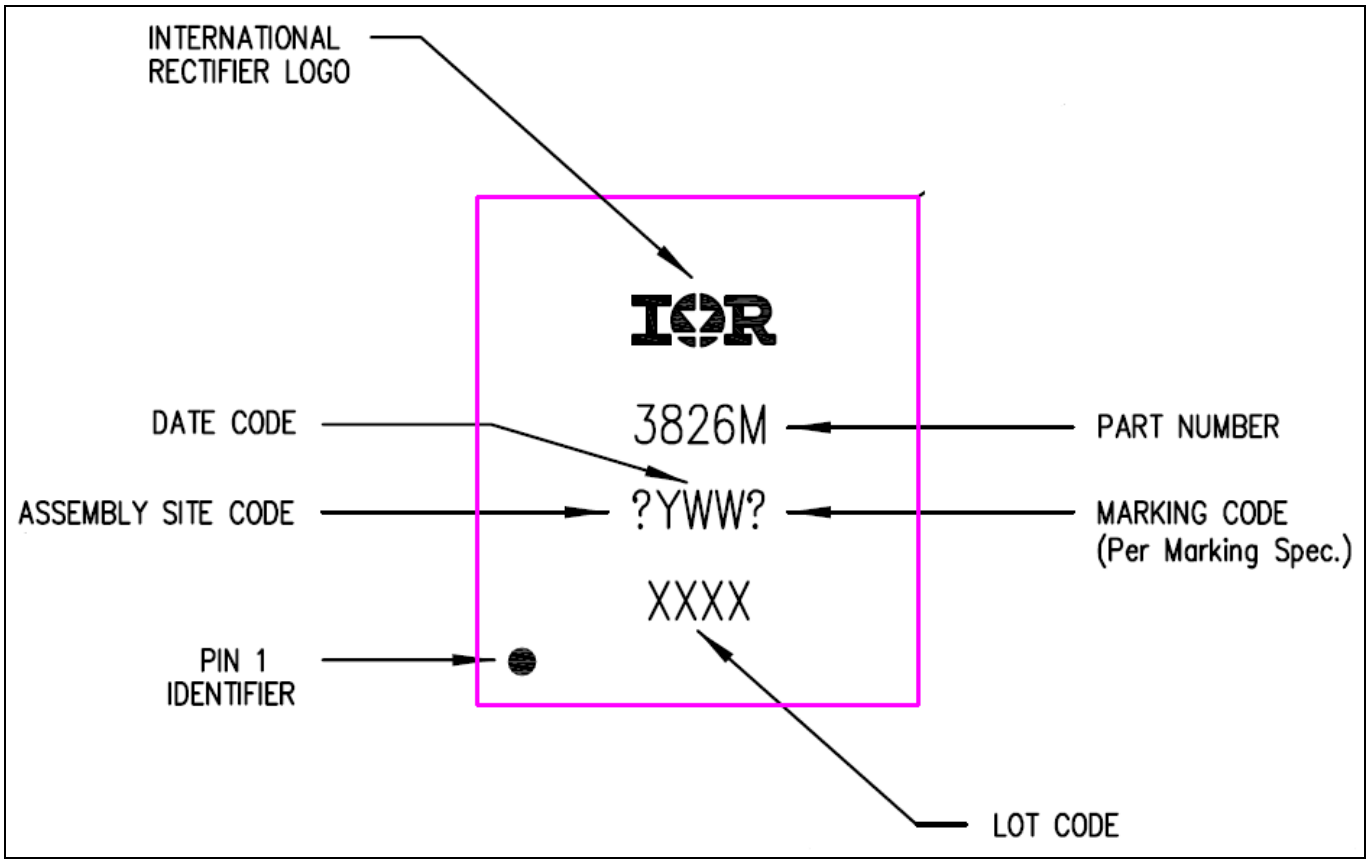


Figure 36 Package Marking

16.2 Dimensions

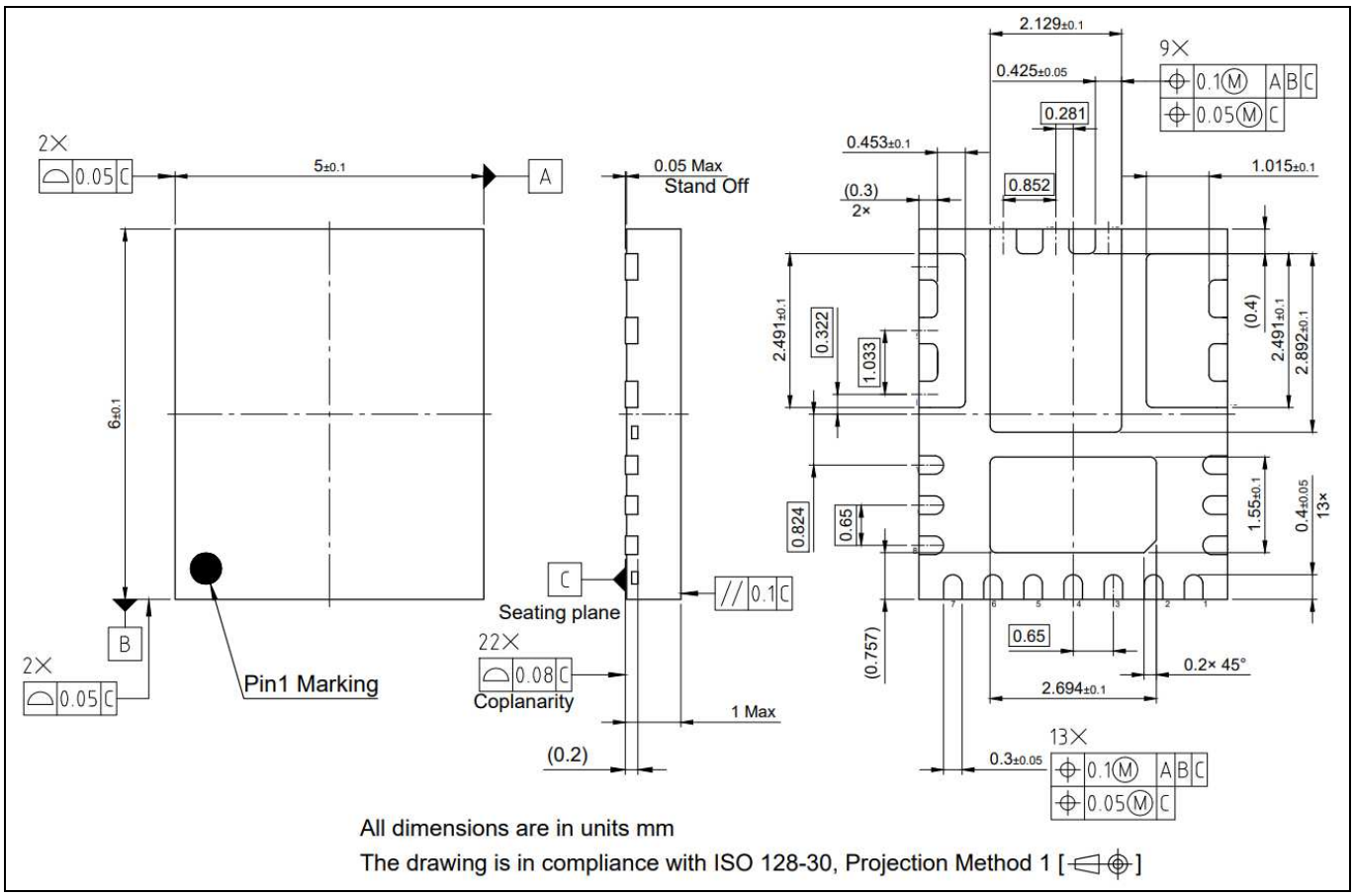


Figure 37 Package Dimensions (all dimensions in mm)

17 Environmental Qualifications

Table 10

Qualification Level		**Industrial**	
Moisture Sensitivity		QFN Package	JEDEC Level 2 @ 260°C
ESD	Human Body Model	JESD22-A114-F, Class 2 (≥ 2000 V to < 4000 V)	
	Charged Device Model	JESD22-C101-D, Class C3 (≥ 500 V to ≤1000 V)	
	Machine Model	JESD22-A115A, Class A (<200 V)	
RoHS2 Compliant		Yes	

Revision History

IR3826

Revision: 2023-03-20, Rev. 2.5

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.2	2018-08-06	Final datasheet
2.3	2019-05-07	Trademark edits
2.4	2019-07-03	Clarify the Bootstrap diode voltage spec by adding spec at Tj = 0degC ~ 125degC . Clarifications added to note 5, and Vcc dropout test conditions. Update Figure 20 and Icc curve in Figure 7.
2.5	2023-03-20	Update PCB footprint and package drawing

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