

FEATURES

- 9-bit latch
- Extended 100E VEE range of -4.2V to -5.5V
- Parity detection/generation
- 800ps max. D to Output
- Reset
- Internal 75KΩ input pull-down resistors
- Fully compatible with Motorola MC10E/100E175
- Available in 28-pin PLCC package

BLOCK DIAGRAM



DESCRIPTION

The SY10/100E175 are 9-bit latches. They also feature a tenth latched output (ODDPAR) which is formed as the odd parity of the nine data inputs (ODDPAR is HIGH if an odd number of the inputs are HIGH).

The E175 can also be used to generate byte parity by using D₈ as the parity-type select (L = even parity, H = odd parity) and using ODDPAR as the byte parity output.

The LEN pin latches the data when asserted with a logical high and makes the latch transparent when placed at a logic low level.

PIN NAMES

Pin	Function
D0 – D8	Data Inputs
LEN	Latch Enable
MR	Master Reset
Q0 – Q8	Data Outputs
ODDPAR	Parity Output
Vcco	Vcc to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E175JC	J28-1	Commercial	SY10E175JC	Sn-Pb
SY10E175JCTR ⁽²⁾	J28-1	Commercial	SY10E175JC	Sn-Pb
SY100E175JC	J28-1	Commercial	SY100E175JC	Sn-Pb
SY100E175JCTR ⁽²⁾	J28-1	Commercial	SY100E175JC	Sn-Pb
SY10E175JZ ⁽³⁾	J28-1	Commercial	SY10E175JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E175JZTR ^(2, 3)	J28-1	Commercial	SY10E175JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E175JZ ⁽³⁾	J28-1	Commercial	SY100E175JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E175JZTR ^(2, 3)	J28-1	Commercial	SY100E175JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^{\circ}C$, DC Electricals only.

2. Tape and Reel.

3. Pb-Free package is recommended for new designs.

TRUTH TABLE

D	LEN	MR	Q	ODDPAR
Н	L	L	Н	H if odd no. of Dn HIGH
L	L	L	L	H if odd no. of Dn HIGH
Х	Н	L	Q0	Q0
Х	Х	Н	L	L

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

		TA = 0°C			Т	TA = +25°C			TA = +85°C			
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
Іін	Input HIGH Current	_	_	150			150			150	μA	
IEE	Power Supply Current										mA	_
	10E	—	110	132	—	110	132	—	110	132		
	100E	—	110	132		110	132		127	152		

AC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

		TA = 0°C			TA = +25°C			TA = +85°C				
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
tPD	Propagation Delay to Output D to Q D to ODDPAR LEN to Q LEN to ODDPAR MR to Q (tPHL) MR to ODDPAR (tPHL)	450 850 525 525 525 525 525	600 1150 700 700 700 700 700	800 1450 900 900 900 900	450 850 525 525 525 525 525	600 1150 700 700 700 700	800 1450 900 900 900 900	450 850 525 525 525 525 525	600 1150 700 700 700 700 700	800 1450 900 900 900 900	ps	
ts	Set-up Time D (Q) D (ODDPAR)	275 900	100 700		275 900		_	275 900			ps	_
tH	Hold Time D (Q) D (ODDPAR)	175 -300	-100 -700		175 –300			175 –300			ps	_
tRR	Reset Recovery Time	850	600	_	850	600	_	850	600		ps	
tskew	Within-Device Skew LEN, MR D to Q D to ODDPAR		75 75 200			75 75 200			75 75 200		ps	1
tr tf	Rise/Fall Times 20–80%	300	500	800	300	500	800	300	500	800	ps	_

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.

28-PIN PLCC (J28-1)



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