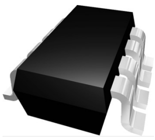
STEF512GR

Datasheet

Dual electronic fuse for 5 V and 12 V rails



TSOT23-8L

Features

- 5 V and 12 V channels into one chip
- 25 V absolute maximum input voltage
- Precise output over voltage clamp
- Fixed current limit: 3 A on 5 V, 4 A on 12 V
- Latched-off thermal protection
- Input undervoltage lockout
- Adjustable output voltage slew-rate for each channel
- Integrated 40 mΩ Power FETs
- SAS disable pin
- TSOT23-8L package

Applications

- HDD and SSD drives
- Set-top boxes
- HDD and SSD array

Maturity status link
STEF512GR

Description

The STEF512GR is an integrated dual electronic fuse, designed to protect circuitry on its output from overcurrent and overvoltage events, in those applications requiring hot swap operation and in-rush current control.

The device embeds two independent electronic fuses, one for the 5 V rails and one for the 12 V rails. Thanks to the very low ON-resistance of the integrated Power FETs, the voltage drop from the main supply to the load is very low during normal operations.

The start-up time can be adjusted by the user for each eFuse, via two small soft-start capacitors, connected to the relevant pins.

In this manner, the inrush current at startup can be kept under control.

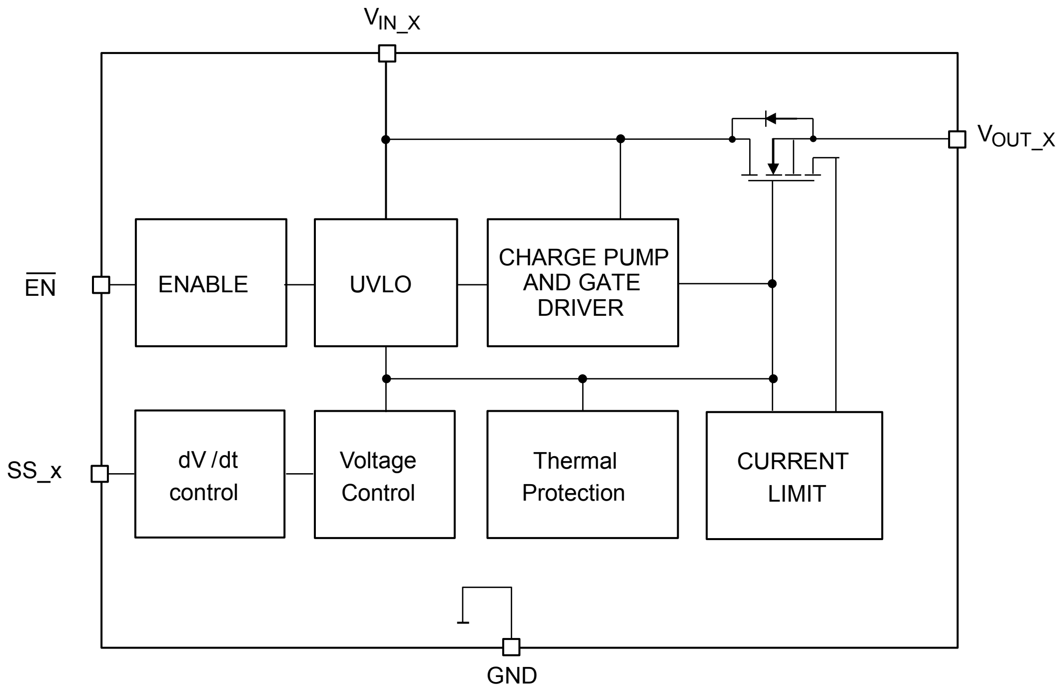
The maximum load current is precisely limited, by utilizing a sense FET topology, to factory-defined values.

The device also provides a precise overvoltage clamp for each channel, preventing the load from being damaged by power supply failures, and undervoltage lockout (UVLO), assuring that the input voltage is above the minimum operating threshold, before the power device is turned on.

When an overload condition occurs, the STEF512GR limits the output current to the predefined safe value. If the anomalous overload condition persists, the device goes into thermal shutdown, the internal switch is opened and the load disconnected from the power supply.

1 Diagram

Figure 1. **Block diagram (one channel)**



2 Pin configuration

Figure 2. Pin connection (top view)

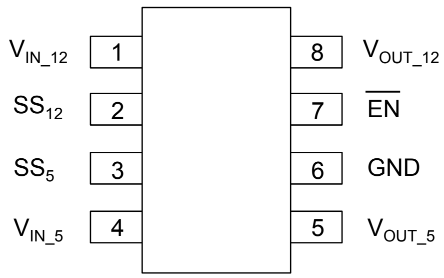


Table 1. Pin description

Pin n°	Symbol	Function
1	V_{IN_12}	12 V rail supply voltage.
2	SS_{12}	Soft-start adjustment pin for the 12 V rail. A capacitor must be connected between this pin and GND to program the output voltage slew-rate. Do not leave floating.
3	SS_5	Soft-start adjustment pin for the 5 V rail. A capacitor must be connected between this pin and GND to program the output voltage slew-rate. Do not leave floating.
4	V_{IN_5}	5 V rail supply voltage.
5	V_{OUT_5}	5 V rail output voltage.
6	GND	Ground.
7	$\overline{EN}$	SAS disable input: set this pin logic-low to turn on the device, high to turn off the device. This pin is internally pulled down via 1 MΩ resistor.
8	V_{OUT_12}	12 V rail output voltage.

3 Typical application

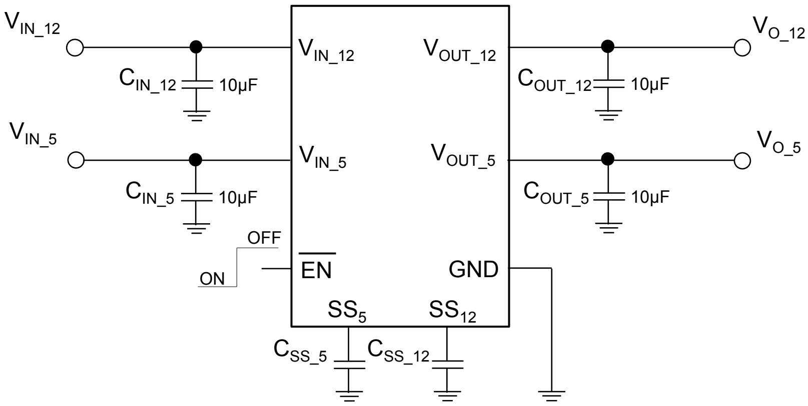


Figure 3. Typical application circuit

4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_5}, V_{IN_12}	Input supply voltage	-0.3 to 25	V
V_{OUT_5}, V_{OUT_12}	Output voltage	-0.3 to V_{IN} + 0.3	V
$V_{\overline{EN}}$	Enable pin voltage	-0.3 to 7	V
SSx	Soft-start pin voltage	-0.3 to 7	V
ESD	Charge device model	±500	V
	Human body model	±2000	
$T_{J\text{-}OP}$	Operating junction temperature	-40 to 125	°C
$T_{J\text{-}MAX}$	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-55 to 150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA} (1)	Thermal resistance junction-ambient	100	°C/W
R_{thJC}	Thermal resistance junction-case	25.5	°C/W

1. *Based on 4-layer JEDEC (2S2P) test board, constructed in accordance with the JESD 51-7 specification.*

5 Electrical characteristics

T_J = 25°C, V_{IN_5} = 5 V, V_{IN_12} = 12 V, $V_{\overline{EN}}$ = 0 V, C_{IN} = 10 µF, C_{OUT} = 10 µF; unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
5 V eFuse						
V_{Clamp_5}	Output clamping voltage	V_{IN_5} = 8 V	5.5	5.7	5.9	V
V_{UVLO_5}	Undervoltage lockout	Turn-on, voltage rising	4.25	4.35	4.45	V
V_{Hyst_5}	UVLO hysteresis	Turn-off, voltage falling		1.78		V
R_{DSon_5}	On-resistance	T_J = 25°C (1)		36		mΩ
		T_J = 125°C (2)			50	
I_{L_5}	Off-state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_5} = GND		1	5	µA
I_{D5}	Maximum continuous current (2) (3)	T_A = 25°C		2.5		A
I_{Short_5}	Short-circuit current limit		0.6	1	1.4	A
I_{Lim_5}	Overload current limit		2.7	3	3.3	A
$dV/dt_{\_5}$	Output voltage ramp time	From 10% to 90% of V_{OUT}, $C_{dv/dt}$ = 100 nF	11	13	15	ms
12 V eFuse						
V_{Clamp_12}	Output clamping voltage	V_{IN_12} = 17 V	14.5	15	15.5	V
V_{UVLO_12}	Undervoltage lockout	Turn-on, voltage rising	9.4	9.7	10	V
V_{Hyst_12}	UVLO hysteresis (12 V rail)	Turn-off, voltage falling		2		V
R_{DSon_12}	On-resistance (12 V rail)	T_J = 25°C (1)		40		mΩ
		T_J = 125°C (2)			70	
I_{L_12}	Off-state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_12} = GND		1	5	µA
I_{D12}	Continuous current (2) (3)	T_A = 25°C		3.5		A
I_{Short_12}	Short-circuit current limit			1.8		A
I_{Lim_12}	Overload current limit		3.6	4	4.5	A
$dV/dt_{\_12}$	Output voltage ramp time	From 10% to 90% of V_{OUT}, $C_{dv/dt}$ = 100 nF	10	12	14	ms
Common features: SAS disable pin, quiescent current						
V_{IL}	$\overline{EN}$ pin low-level input voltage	Output enabled			0.7	V
V_{IH}	$\overline{EN}$ pin high-level input voltage	Output disabled	2.1			V
R_P	$\overline{EN}$ pin internal pull-down resistor			1		MΩ

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_q	Quiescent current (excluding $\overline{EN}$ current)	Device operating		250	1000	μA
		Off-state, $V_{\overline{EN}}$ = 5 V		40	80	μA
$I_{\overline{EN}}$	Sas disable pin current	$V_{\overline{EN}}$ = 5 V			10	μA
Thermal protection						
T_{SD}	Shutdown temperature (2)			165		°C
	Hysteresis			20		

1. *Pulsed test.*
2. *Guaranteed by design or characterization, but not tested in production.*
3. *The maximum continuous current is the current level above which the control loop starts increasing the ON-resistance of the pass element.*

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	Input capacitance	1	47		μF
C_{OUT}	Output capacitance	10	47		

6 Device functional description

The STEF512GR embeds a 5 V and a 12 V electronic fuse (eFuses). Each eFuse is an intelligent load switch, which is able to limit the voltage or the current during fault events, such as: input overvoltage or output overload respectively. For this purpose, it contains 2 analogue control loops, the former limits the output voltage and the latter limits the input current.

The current limiting loop is also used during the start-up phase of the eFuse to limit the inrush current into the output capacitor.

During the normal operation, the eFuse behaves like a low-resistance Power FET, therefore the output voltage follows the input one. In case of overvoltage or overcurrent events, the eFuse limits the V_{GS} of the internal FET, in order to clamp the output voltage or current respectively. During such events the die temperature rises due to the power dissipation and so, if the fault persists and the overtemperature threshold is overcome, the device goes into thermal shutdown, the internal FET is turned-off and the load disconnected from the power supply.

Once the eFuse is in thermal shutdown, it does not restart automatically. The eFuse can be restarted manually by toggling the $\overline{EN}$ pin or performing a power-up cycle, (this becomes effective as soon as the die temperature drops by at least the overtemperature hysteresis).

Each eFuse provides factory-trimmed undervoltage lockout feature and user-adjustable output voltage rise time.

6.1 Undervoltage lockout

The undervoltage lockout circuit prevents each eFuse from turning on if the supply voltage is below the UVLO rising threshold. During this operation, if the input voltage falls below (V_{UVLO_x} - V_{Hyst_x}), the output of the relevant channel is turned off.

If the supply voltage comes back into the operative range, the relevant channel restarts with a soft-start cycle.

6.2 Start-up sequence and voltage clamp

The typical start-up sequence of each eFuse is as follows:

- The power supply is connected to the V_{IN_x} pin and it is higher than the undervoltage lockout threshold
- The disable pin is asserted by the user to low logic level (or left floating), enabling the device
- Typically, 1.2 ms after the eFuse starts ramping up the output voltage
- Each channel ramps up with a rate set by the relevant C_{SSx}
- If the input voltage continues rising, above the overvoltage threshold (V_{Clamp_x}), as a consequence of a failure in the power supply, the eFuse limits the output voltage to V_{Clamp_x}. The eFuse keeps operating in this state until it hits its overtemperature threshold and shuts down.

6.3 Current limit function

Each eFuse provides 2 kinds of current limit protections:

- Operative current limit: in case of overload, i.e. if the load current exceeds the I_{Dxx}, the device starts increasing the power MOS resistance. The overload current limit (I_{Lim_x}) is 3 A typ. for the 5 V fuse and 4 A (typ.) for the 12 V one.
- In case of strong overload or short-circuit, the short-circuit current limit is activated and the current is clamped to I_{Short_x}: 1 A typ. on 5 V channel and 1.8 A typ. on 12 V channel.

7 Typical characteristics

The following plots are referred to the typical application circuit and, unless otherwise noted, at T_A = 25°C.

Figure 4. 5 V channel I_{lim} vs. temperature

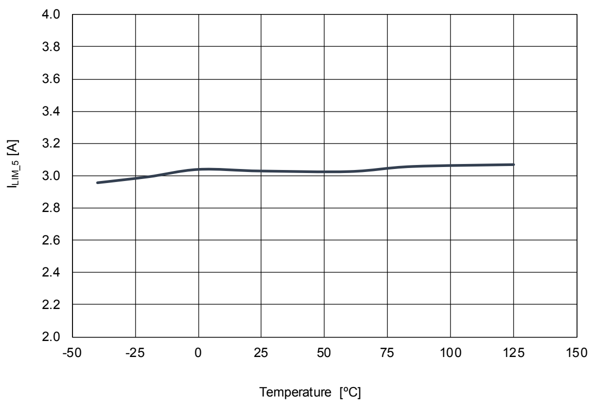


Figure 5. 12 V channel I_{lim} vs. temperature

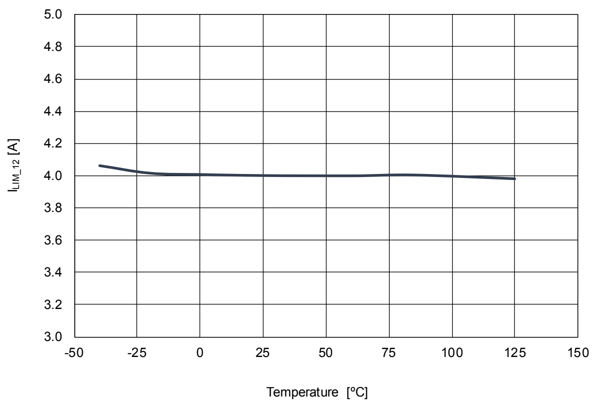


Figure 6. 5 V ch. R_{DS_ON} vs. temperature

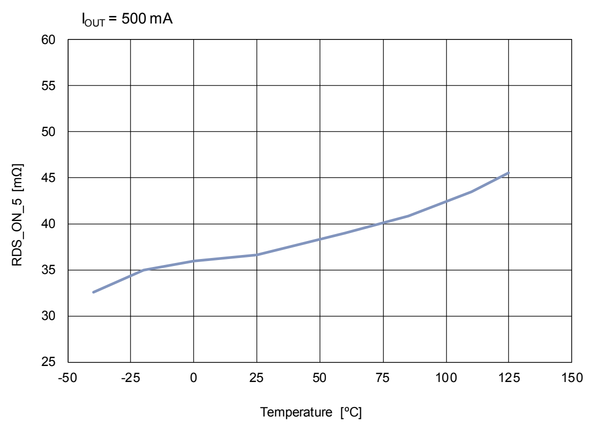


Figure 7. 12 V ch. R_{DS_ON} vs. temperature

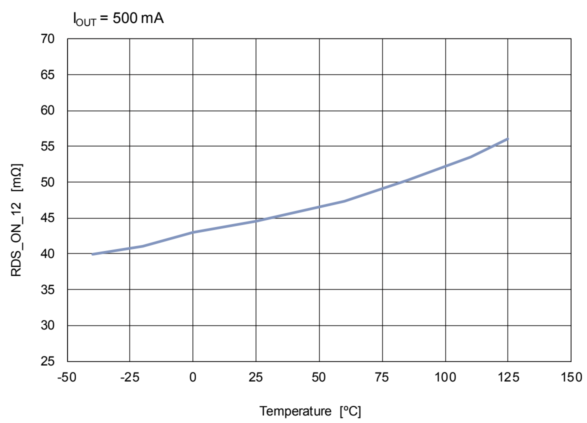


Figure 8. **5 V ch. voltage clamp vs. temperature**

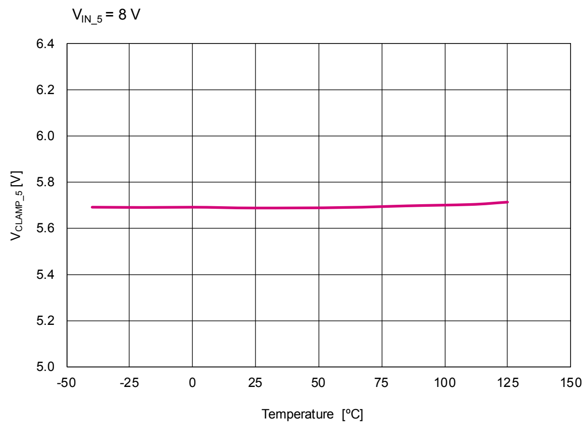


Figure 9. **12 V ch. voltage clamp vs. temperature**

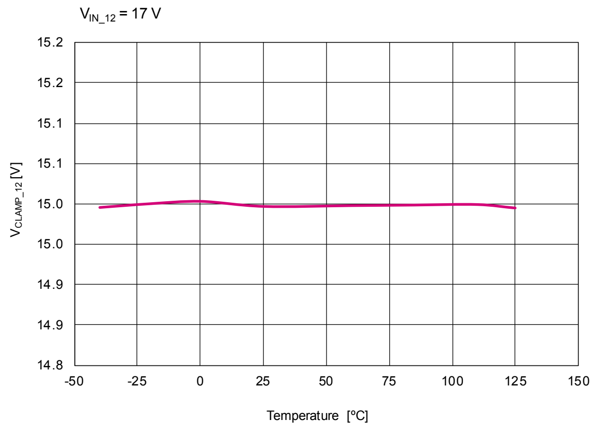


Figure 10. **5 V ch. UVLO vs. temperature**

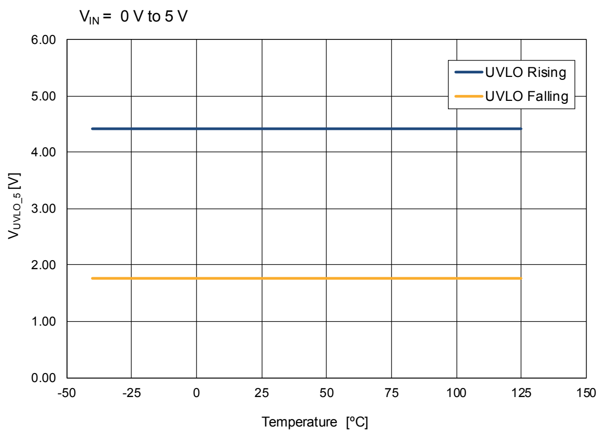


Figure 11. **12 V ch. UVLO vs. temperature**

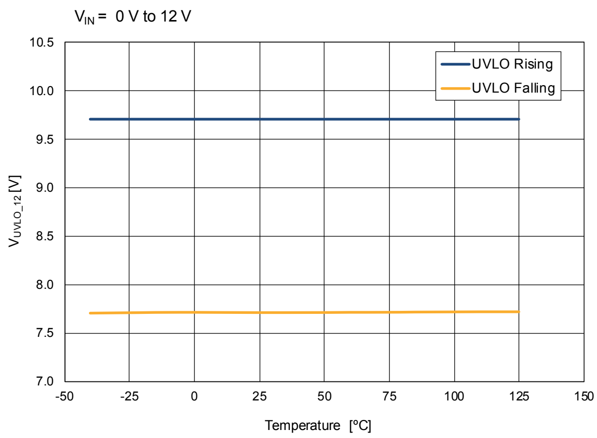


Figure 12. **$\overline{EN}$ pin thresholds vs. temperature**

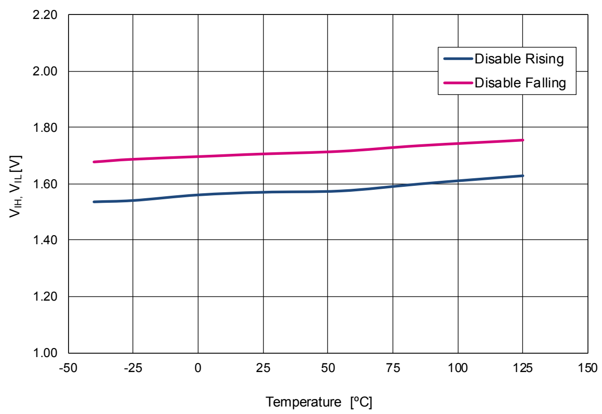


Figure 13. **$\overline{EN}$ pin current vs. temperature**

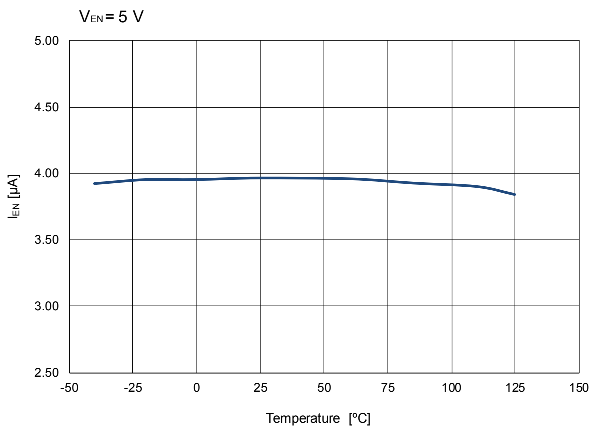


Figure 14. Startup with no load from V_{IN}

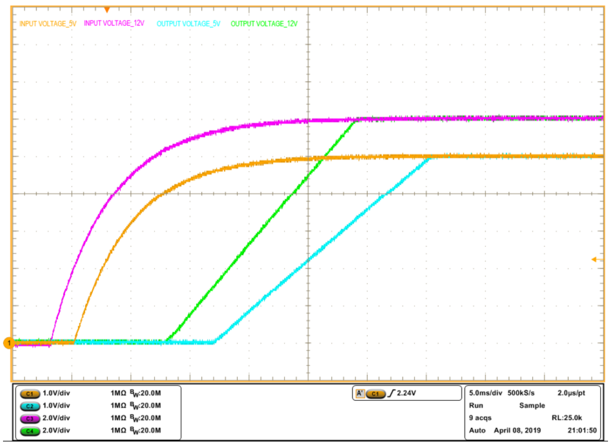


Figure 15. V_{Out_5} startup with 2 A load

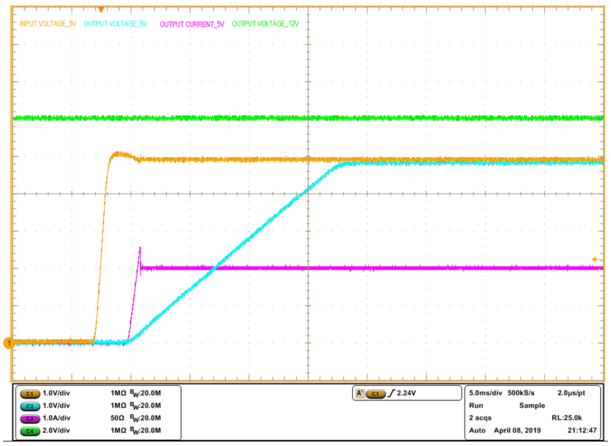


Figure 16. V_{Out_12} startup with 2 A load

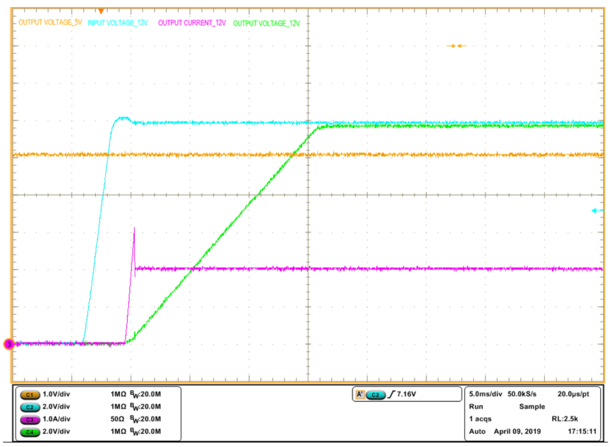


Figure 17. Startup by EN, no load

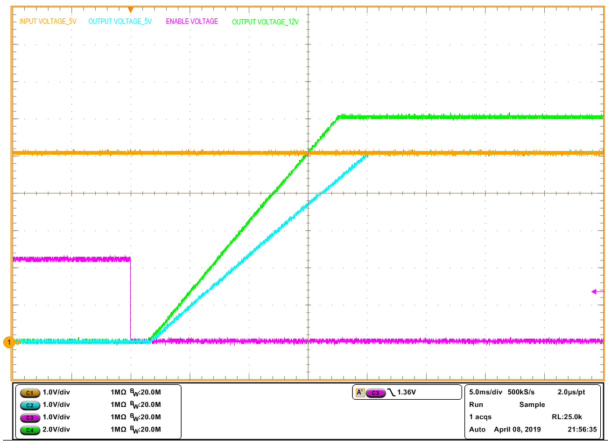


Figure 18. Startup by En @ 2 A load

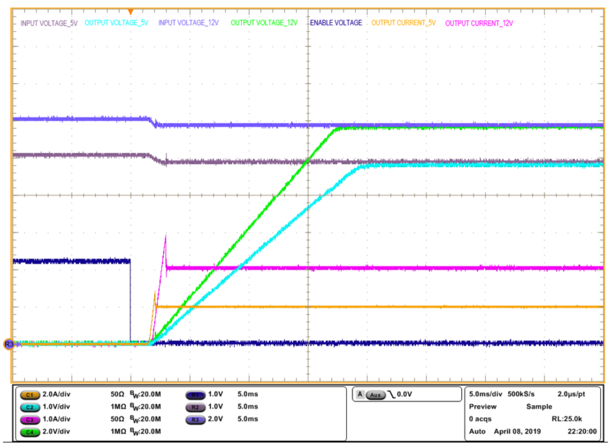


Figure 19. V_{Out_5} current limit and short

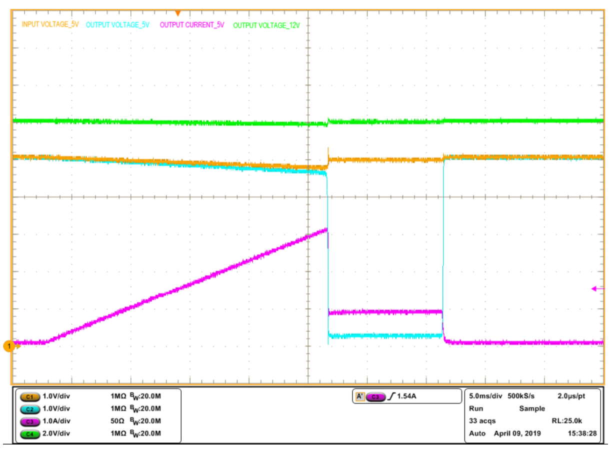


Figure 20. V_{Out_12} current limit and short

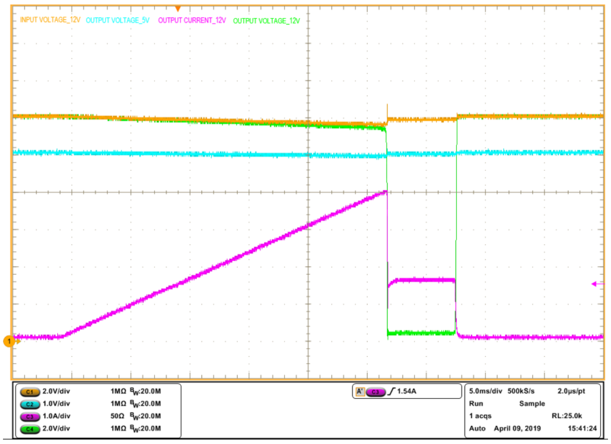


Figure 21. V_{Out_5} UVLO rising

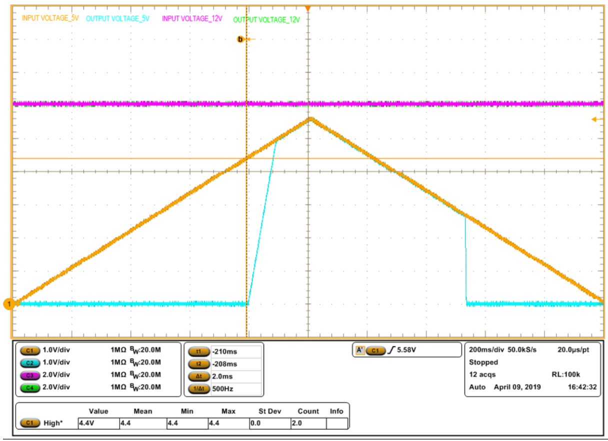


Figure 22. V_{Out_12} UVLO rising

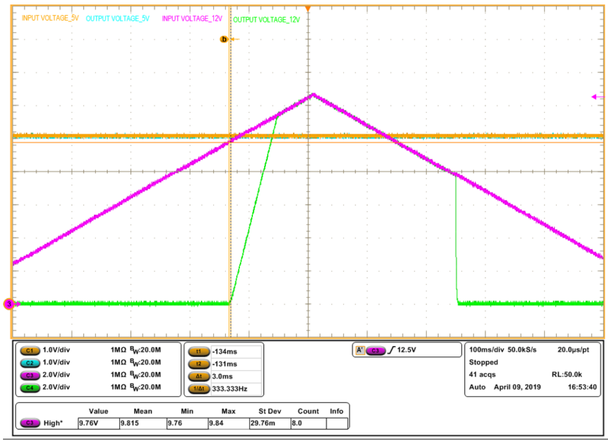


Figure 23. V_{Out_5} startup vs. C_{SS}

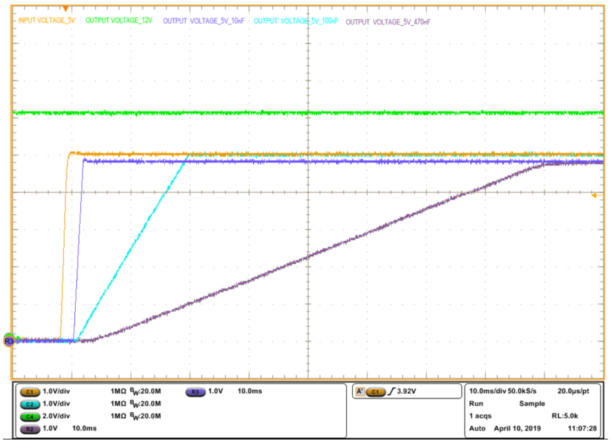


Figure 24. V_{Out_12} startup vs. C_{SS}

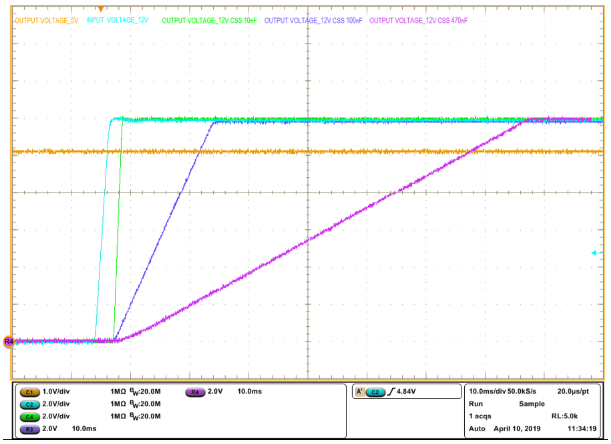


Figure 25. V_{Out_5} voltage clamp

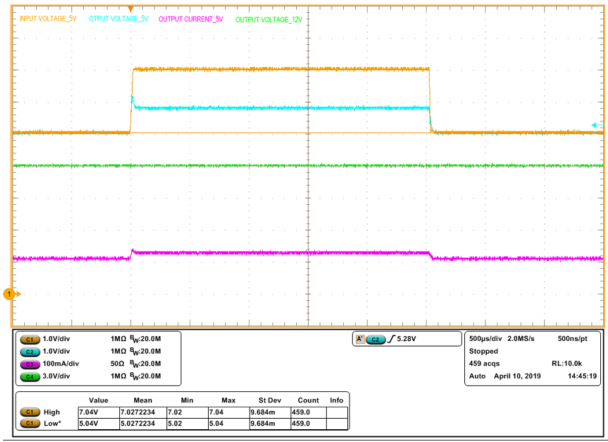
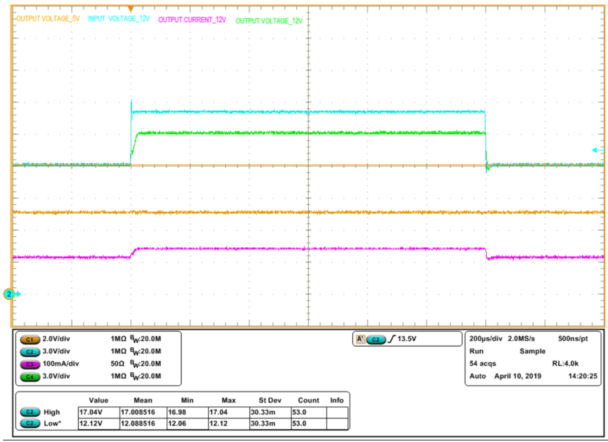


Figure 26. V_{Out_12} voltage clamp



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 TSOT23-8L package information

Figure 27. TSOT23-8L package outline

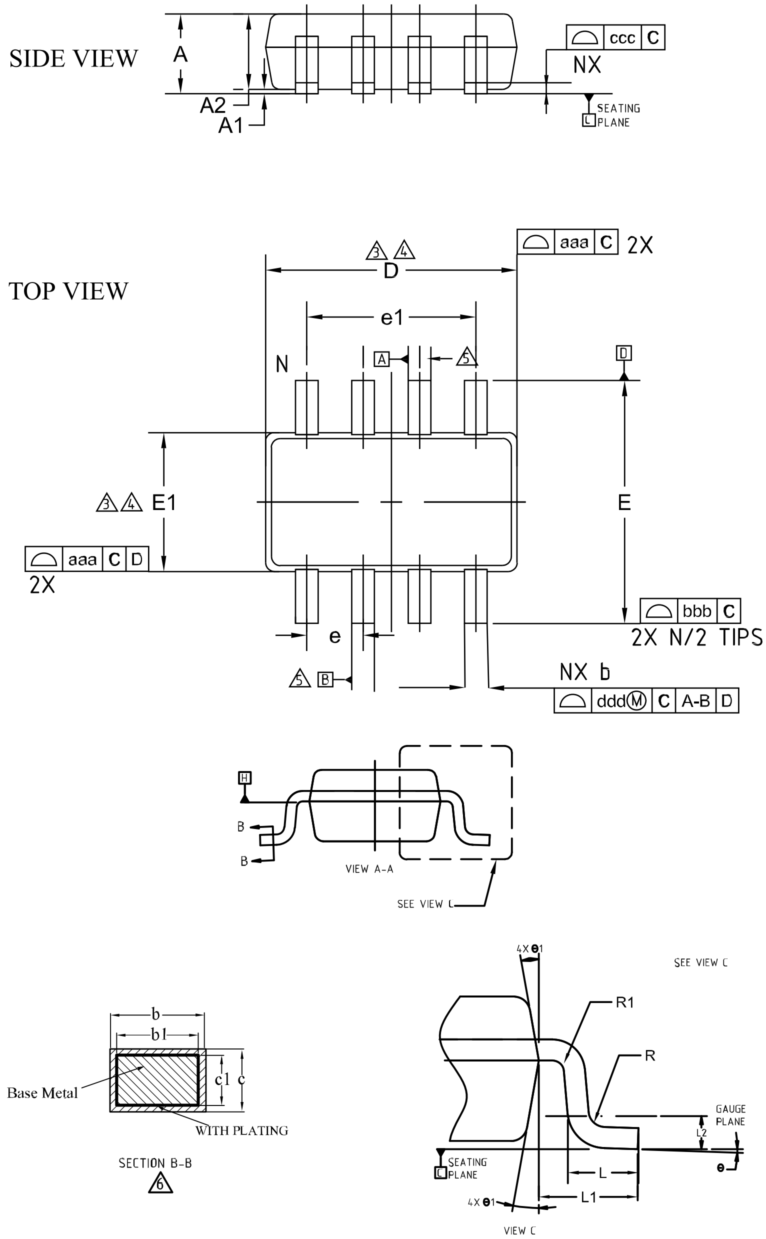
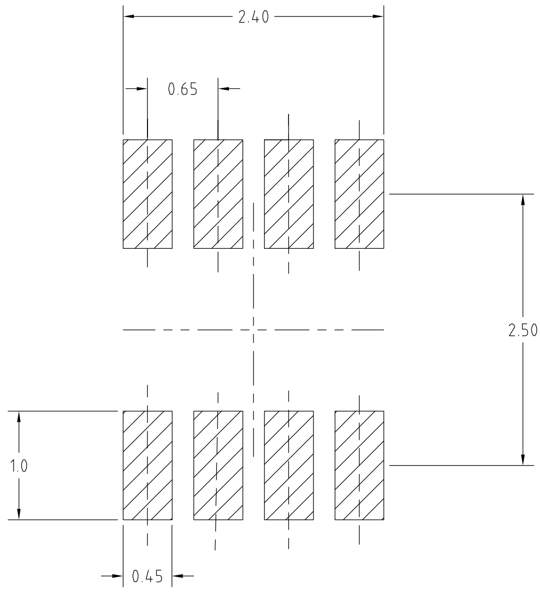


Table 6. TSOT23-8L mechanical data

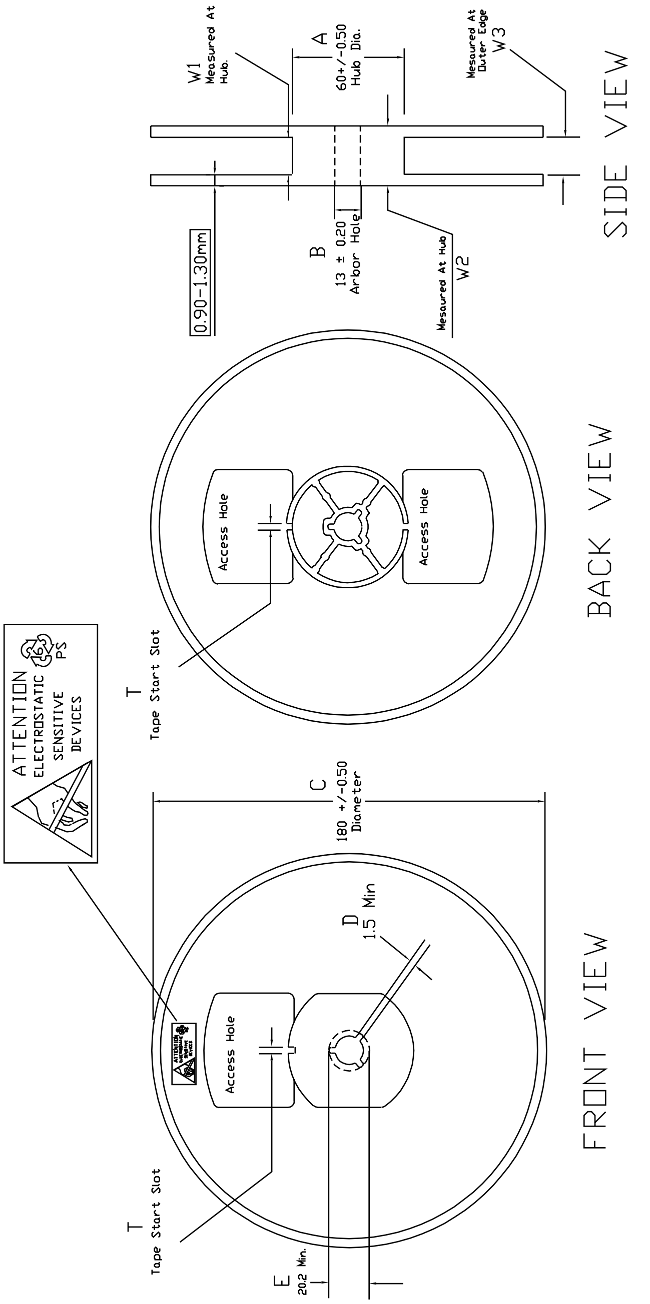
Dim.	mm		
	Min.	Typ.	Max.
A			1
A1	0.01	0.05	0.1
A2	0.84	0.87	0.9
b	0.22	-	0.36
b1	0.22	0.26	0.3
c	0.12	0.15	0.2
c1	0.08	0.13	0.16
D	-	2.90 BSC	-
E	-	2.80 BSC	-
E1	-	1.60 BSC	-
e	-	0.65 BSC	-
e1	-	1.95 BSC	-
L	0.3	0.4	0.5
L1	-	0.60 BSC	-
L2	-	0.25 BSC	-
R	0.1	-	-
R1	0.1	-	0.25
Θ	0	4°	8°
Θ1	4°	10°	12°
Tolerance of form and position			
aaa	0.15		
bbb	0.25		
ccc	0.1		
ddd	0.13		
N	8		
ND	4		

Figure 28. TSOT23-8L recommended footprint



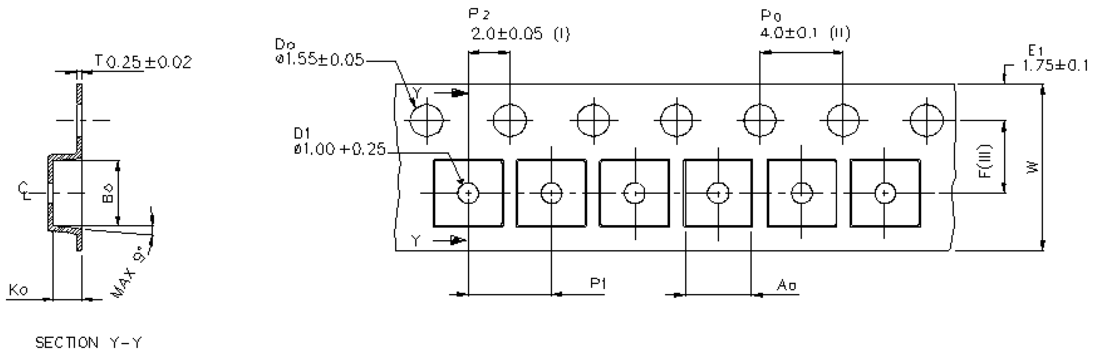
8.2 TSOT23-8L packing information

Figure 29. **TSOT23-8L reel drawing outline**



TAPE WIDTH	T	W1	W2	W3
8MM	3+/-.50	8.4+1.5 -0.0	14.4 MAX	7.9MIN 10.9MAX

Figure 30. TSOT23-8L carrier tape

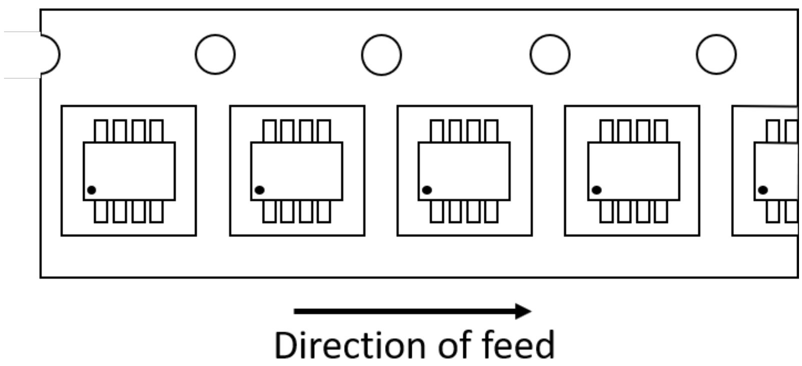


Ao	3.23 +/−0.10
Bo	3.17 +/−0.10
Ko	1.37 +/−0.10
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +0.3/−0.1

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max. 10^{9} OHM/SR

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 31. TSOT23-8L device orientation in tape



9 Ordering information

Table 7. Order code

Order code	Package	Current limit configuration	Marking
STEF512GR	TSOT23-8L	3 A on 5 V, 4 A on 12 V	H512

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
24-Feb-2020	1	Initial release.
02-Mar-2020	2	Updated title in Figure 16. VOut_12 startup with 2 A load.
10-Jun-2021	3	Added new Section 8.2 TSOT23-8L packing information.

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