

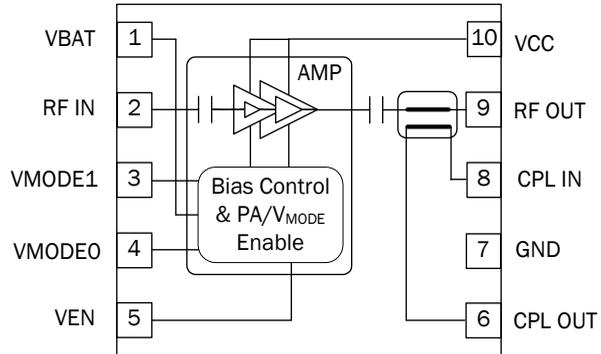


**Features**

- HSDPA and HSPA+ Compliant
- Low Voltage Positive Bias Supply (3.0V to 4.35V)
- +28.0dBm Linear Output Power (+26.5dBm HSDPA)
- High Efficiency Operation  
41% at  $P_{OUT}=+28.0\text{dBm}$   
18% at  $P_{OUT}=+17.0\text{dBm}$   
13% at  $P_{OUT}=+11.0\text{dBm}$
- Low Quiescent Current in Low Power Mode: 6mA
- Internal Voltage Regulator Eliminates the Need for External Reference Voltage ( $V_{REF}$ )
- 3-Mode Power States with Digital Control Interface
- Integrated Power Coupler
- Integrated Blocking and Collector Decoupling Capacitors

**Applications**

- WCDMA/HSDPA Wireless Handsets and Data Cards
- Dual-Mode UMTS Wireless Handsets



Functional Block Diagram

**Product Description**

The RF7221 is a high-power, high-efficiency, linear power amplifier designed for use as the final RF amplifier in 3V, 50Ω W-CDMA mobile cellular equipment and spread-spectrum systems. This PA is developed for UMTS Band 1 which operates in the 1920MHz to 1980MHz frequency band. The RF7221 has two digital control pins to select one of three power modes to optimize performance and current drain at lower power levels. The part also has an integrated directional coupler which eliminates the need for an external discrete coupler at the output. The RF7221 is fully HSDPA and HSPA+ compliant and is assembled in a 10-pin, 3mmx3mm module.

**Ordering Information**

RF7221                      3V W-CDMA Band 1 Linear PA Module  
RF7221PCBA-410       Fully Assembled Evaluation Board

**Optimum Technology Matching® Applied**

- |   |                                      |                                     |                                   |
|---|--------------------------------------|-------------------------------------|-----------------------------------|
| <input type="checkbox"/> GaAs HBT             | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET          | <input type="checkbox"/> Si BiCMOS   | <input type="checkbox"/> Si CMOS    | <input type="checkbox"/> RF MEMS  |
| <input checked="" type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT    | <input type="checkbox"/> Si BJT     | <input type="checkbox"/> LDMOS    |

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## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage in Standby Mode	6.0	V
Supply Voltage in Idle Mode	6.0	V
Supply Voltage in Operating Mode, 50Ω Load	6.0	V
Supply Voltage, V <sub>BAT</sub>	6.0	V
Control Voltage, V <sub>MODE0</sub> , V <sub>MODE1</sub>	3.5	V
Control Voltage, V <sub>EN</sub>	3.5	V
RF - Input Power	+10	dBm
RF - Output Power	+30	dBm
Output Load VSWR (Ruggedness)	10:1	
Operating Ambient Temperature	-30 to +110	°C
Storage Temperature	-55 to +150	°C



**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Recommended Operating Conditions</b>					
Operating Frequency Range	1920		1980	MHz	
V <sub>BAT</sub>	+3.0	+3.4	+4.35	V	
V <sub>CC</sub>	+3.0 <sup>1</sup>	+3.4	+4.35	V	
V <sub>EN</sub>	0		0.5	V	PA disabled.
	1.4	1.8	3.0	V	PA enabled.
V <sub>MODE0</sub> , V <sub>MODE1</sub>	0		0.5	V	Logic "low".
	1.5	1.8	3.0	V	Logic "high".
P <sub>OUT</sub>					
Maximum Linear Output (HPM)	28.0 <sup>2,3</sup>			dBm	High Power Mode (HPM)
Maximum Linear Output (MPM)	17.0 <sup>2,3</sup>			dBm	Medium Power Mode (MPM)
Maximum Linear Output (LPM)	11.0 <sup>2,3</sup>			dBm	Low Power Mode (LPM)
Ambient Temperature	-30	+25	+85	°C	

Notes:

<sup>1</sup>Minimum V<sub>CC</sub> for max P<sub>OUT</sub> is indicated.

<sup>2</sup>For operation at V<sub>CC</sub>=+3.2V, derate P<sub>OUT</sub> by 0.6dB. For operation at V<sub>CC</sub>=3.0V, derate P<sub>OUT</sub> by 1.3dB.

<sup>3</sup>P<sub>OUT</sub> is specified for 3GPP (Rel99) modulation. For HSDPA and HSPA+ operation, derate P<sub>OUT</sub> by 1.5dB:

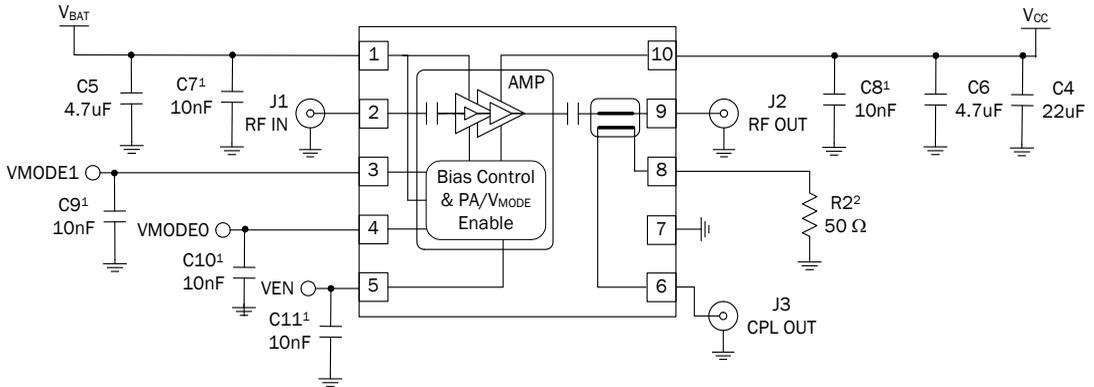
HSDPA Configuration: β<sub>c</sub>=12, β<sub>d</sub>=15, β<sub>hs</sub>=24

HSPA+ Configuration: Rel7 Subtest 1

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Electrical Specifications</b>					T = +25 °C, V <sub>CC</sub> = V <sub>BAT</sub> = +3.4V, V <sub>EN</sub> = +1.8V, 50Ω system, W-CDMA Rel 99 Modulation unless otherwise specified.
Gain	25	26		dB	HPM, P <sub>OUT</sub> = 28.0dBm
	18	20		dB	MPM, P <sub>OUT</sub> ≤ 17.0dBm
	12	13		dB	LPM, P <sub>OUT</sub> ≤ 11.0dBm
Gain Linearity		±0.7		dB	HPM, 17.0dBm ≤ P <sub>OUT</sub> ≤ 28.0dBm
ACLR - 5 MHz Offset		-40		dBc	HPM, P <sub>OUT</sub> = 28.0dBm
		-40		dBc	MPM, P <sub>OUT</sub> = 17.0dBm
		-40		dBc	LPM, P <sub>OUT</sub> = 11.0dBm
ACLR - 10MHz Offset		-52		dBc	HPM, P <sub>OUT</sub> = 28.0dBm
		-60		dBc	MPM, P <sub>OUT</sub> = 17.0dBm
		-60		dBc	LPM, P <sub>OUT</sub> = 11.0dBm
PAE		41		%	HPM, P <sub>OUT</sub> = 28.0dBm
		18		%	MPM, P <sub>OUT</sub> = 17.0dBm
		13		%	P <sub>OUT</sub> = 11.0dBm
Current Drain		470		mA	HPM, P <sub>OUT</sub> = 28.0dBm
		83		mA	MPM, P <sub>OUT</sub> = 17.0dBm
		27		mA	LPM, P <sub>OUT</sub> = 11.0dBm
Quiescent Current		50		mA	HPM, DC only
		15		mA	MPM, DC only
		6		mA	LPM, DC only
Enable Current		0.1		mA	Source or sink current. V <sub>EN</sub> = 1.8V.
Mode Current (I <sub>MODE0</sub> , I <sub>MODE1</sub> )		0.1		mA	Source or sink current. V <sub>MODE0</sub> , V <sub>MODE1</sub> = 1.8V.
Leakage Current		5.0	15.0	μA	DC only. V <sub>CC</sub> = V <sub>BAT</sub> = 4.35V, V <sub>EN</sub> = V <sub>MODE0</sub> = V <sub>MODE1</sub> = 0.5V.
Noise Power in Receive Band		-135		dBm/Hz	All power modes, measured at duplex offset frequency (FTX + 190MHz). Rx: 2110MHz to 2170MHz, P <sub>OUT</sub> ≤ 28.0dBm
Input Impedance		1.5:1		VSWR	No ext. matching, P <sub>OUT</sub> ≤ 28dBm, all modes.
Harmonic, 2FO		-20		dBm	P <sub>OUT</sub> ≤ 28.0dBm, all power modes.
Harmonic, 3FO		-25		dBm	P <sub>OUT</sub> ≤ 28.0dBm, all power modes.
Spurious Output Level			-70	dBc	All spurious, P <sub>OUT</sub> ≤ 28dBm, all conditions, load VSWR ≤ 6:1, all phase angles.
Insertion Phase Shift		±25		°	Phase shift at 17dBm when switching from HPM to MPM and MPM to LPM at 11dBm.
DC Enable Time			10	μS	DC only. Time from V <sub>EN</sub> = high to stable idle current (90% of steady state value).
RF Rise/Fall Time			6	μS	P <sub>OUT</sub> ≤ 28.0dBm, all modes. 90% of target, DC settled prior to RF.
Coupling Factor		-20		dB	P <sub>OUT</sub> ≤ 28.0dBm, all modes.
Coupling Accuracy - Temp/Voltage		±0.5		dB	P <sub>OUT</sub> ≤ 28.0dBm, all modes. -30 °C ≤ T ≤ 85 °C, 3.0V ≤ V <sub>CC</sub> & V <sub>BAT</sub> ≤ 4.35V, referenced to 25 °C, 3.4V conditions.
Coupling Accuracy - VSWR		±0.25		dB	P <sub>OUT</sub> ≤ 28dBm, all modes, load VSWR = 2:1, ±0.25dB accuracy corresponds to 20dB directivity.



**Preliminary Application Schematic**



**NOTES:**

- 1 Place these capacitors as close to PA as possible.
- 2 50 Ω resistor will be removed if pin 8 is connected to another coupler.

**PCB Design Requirements**

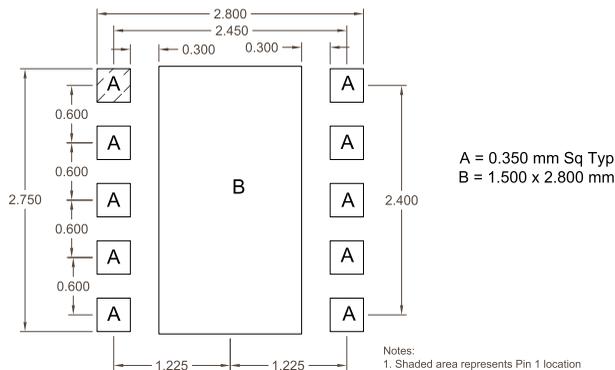
**PCB Surface Finish**

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

**PCB Land Pattern Recommendation**

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

**PCB Metal Land Pattern**



**Figure 1. PCB Metal Land Pattern (Top View)**

## PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

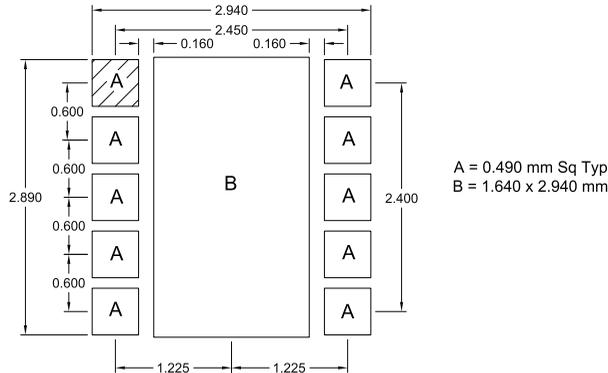


Figure 2. PCB Solder Mask Pattern

## Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.