

**PCN Number: RC134001**

**Notification Date\*:** November 5, 2013

<b>Title:</b> Migration to Marketing Revision Level C of the AT91SAM7X128 and AT91SAM7X256															
<b>Product Identification:</b>															
		<b>Current Part Number</b>	<b>New Part Number</b>												
		AT91SAM7X256B-AU	AT91SAM7X256C-AU												
		AT91SAM7X256B-AU-999	AT91SAM7X256C-AUR												
		AT91SAM7X256B-CU	AT91SAM7X256C-CU												
		AT91SAM7X256B-CU-999	AT91SAM7X256C-CUR												
		AT91SAM7X128B-AU	AT91SAM7X128C-AU												
		AT91SAM7X128B-AU-999	AT91SAM7X128C-AUR												
		AT91SAM7X128B-CU	AT91SAM7X128C-CU												
		AT91SAM7X128B-AU-999	AT91SAM7X128C-CUR												
<b>Reason for Change:</b>	<input type="checkbox"/> Material / Composition														
	<input checked="" type="checkbox"/> Processing / Manufacturing														
	<input checked="" type="checkbox"/> Design / Firmware														
	<input checked="" type="checkbox"/> Datasheet														
	<input type="checkbox"/> Manufacturing Location														
	<input type="checkbox"/> Quality / Reliability														
	<input type="checkbox"/> Logistics														
	<input type="checkbox"/> Other:														
<b>Change Description:</b>															
<p>A complete list of differences between the marketing revision level (MRL) B and C can be found in chapter 41 of the AT91SAM7X series datasheet with Atmel document reference 6120I. Multiple errata have been corrected on the ADC, CAN, EMAC, PWM, SPI, SSC, TWI and USART.</p> <p>The ChipID has been incremented to:</p> <p style="margin-left: 40px;">AT91SAM7X256 Revision C chip ID is 0x275B 0942 AT91SAM7X128 Revision C chip ID is 0x275A 0742</p> <p>The Flash memory access time has been reduced as per the below table:</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 25%;">Flash Wait State</th> <th style="width: 25%;">Read Operations</th> <th style="width: 50%;">Maximum Operating Frequency (MHz)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 cycle</td> <td style="text-align: center;">20</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">2 cycles</td> <td style="text-align: center;">48.1</td> </tr> <tr> <td style="text-align: center;">2</td> <td style="text-align: center;">3 cycles</td> <td style="text-align: center;">55</td> </tr> </tbody> </table> <p>Migration from the current 0.18µm process to the 0.15µm process.</p>				Flash Wait State	Read Operations	Maximum Operating Frequency (MHz)	0	1 cycle	20	1	2 cycles	48.1	2	3 cycles	55
Flash Wait State	Read Operations	Maximum Operating Frequency (MHz)													
0	1 cycle	20													
1	2 cycles	48.1													
2	3 cycles	55													
<b>Identification Method to Distinguish Change:</b>															
Marketing Revision Level (MRL) has been incremented on the top side marking to C.															
<b>Qualification Data:</b>	<input checked="" type="checkbox"/> Available	<input type="checkbox"/> Will be available (mm/dd/yr):	<input type="checkbox"/> Not Applicable												

<b>Samples:</b>	<input checked="" type="checkbox"/> Available	<input type="checkbox"/> Will be available (mm/dd/yr):	<input type="checkbox"/> Not Applicable
<b>Quantifiable Impact on Quality &amp; Reliability:</b> None			
<b>Forecasted Availability Date:</b> September 30, 2013 <b>Last Time Buy Date:</b> January 8, 2014 <b>Last Ship Date:</b> October 31, 2014  <i>*All orders placed after the notification date are non-cancellable and non-returnable (NCNR).</i>			
<b>Atmel Contact:</b> Please contact your Atmel Sales Representative or Distributor for additional information (when replying via e-mail please include the PCN number in subject line).			
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Company: Name: Title: Date: Email Address: Location: Comments:	
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