



64 Mbit (x16) Advanced Multi-Purpose Flash Plus

SST38VF6401B / SST38VF6402B

SST38VF6403B / SST38VF6404B

Preliminary Specification

The SST38VF6401B/6402B/6403B/6404B are 4M x16 CMOS Advanced Multi-Purpose Flash Plus (Advanced MPF+) devices manufactured with SST proprietary, high-performance CMOS Super-Flash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST38VF6401B/6402B/6403B/6404B write (Program or Erase) with a 2.7-3.6V power supply. This device conforms to JEDEC standard pin assignments for x16 memories.

Features

- **Organized as 4M x16**
- **Single Voltage Read and Write Operations**
 - 2.7-3.6V
- **Superior Reliability**
 - Endurance: 100,000 Cycles minimum
 - Greater than 100 years Data Retention
- **Low Power Consumption (typical values at 5 MHz)**
 - Active Current: 25 mA (typical)
 - Standby Current: 5 μ A (typical)
 - Auto Low Power Mode: 5 μ A (typical)
- **128-bit Unique ID**
- **Security-ID Feature**
 - 248 Word, user One-Time-Programmable
- **Protection and Security Features**
 - Hardware Boot Block Protection/WP# Input Pin, Uniform (32 KWord) and Non-Uniform (8 KWord) options available
 - User-controlled individual block (32 KWord) protection, using software only methods
 - Password protection
- **Hardware Reset Pin (RST#)**
- **Fast Read and Page Read Access Times:**
 - 70 ns Read access time
 - 25 ns Page Read access times
 - 8-Word Page Read buffer
- **Latched Address and Data**
- **Fast Erase Times:**
 - Block-Erase Time: 18 ms (typical)
 - Chip-Erase Time: 40 ms (typical)
- **Erase-Suspend/-Resume Capabilities**
- **Fast Word and Write-Buffer Programming Times:**
 - Word-Program Time: 7 μ s (typical)
 - Write Buffer Programming Time: 1.75 μ s / Word (typical)
 - 16-Word Write Buffer
- **Automatic Write Timing**
 - Internal V_{PP} Generation
- **End-of-Write Detection**
 - Toggle Bits
 - Data# Polling
 - RY/BY# Output
- **CMOS I/O Compatibility**
- **JEDEC Standard**
 - Flash EEPROM Pinouts and command sets
- **CFI Compliant**
- **Packages Available**
 - 48-lead TSOP
 - 48-ball TFBGA
- **All non-Pb (lead-free) devices are RoHS compliant**



Product Description

The SST38VF6401B, SST38VF6402B, SST38VF6403B, and SST38VF6404B devices are 4M x16 CMOS Advanced Multi-Purpose Flash Plus (Advanced MPF+) manufactured with SST proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST38VF6401B/6402B/6403B/6404B write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pin assignments for x16 memories.

Featuring high performance Word-Program, the SST38VF6401B/6402B/6403B/6404B provide a typical Word-Program time of 7 μ sec. For faster word-programming performance, the Write-Buffer Programming feature, has a typical word-program time of 1.75 μ sec. These devices use Toggle Bit, Data# Polling, or the RY/BY# pin to indicate Program operation completion. In addition to single-word Read, Advanced MPF+ devices provide a Page-Read feature that enables a faster word read time of 25 ns, eight words on the same page.

To protect against inadvertent write, the SST38VF6401B/6402B/6403B/6404B have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are available with 100,000 cycles minimum endurance. Data retention is rated at greater than 100 years.

The SST38VF6401B/6402B/6403B/6404B are suited for applications that require the convenient and economical updating of program, configuration, or data memory. For all system applications, Advanced MPF+ significantly improve performance and reliability, while lowering power consumption. These devices inherently use less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. For any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time; therefore, the total energy consumed during any Erase or Program operation is less than alternative flash technologies.

These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications. The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

The SST38VF6401B/6402B/6403B/6404B also offer flexible data protection features. Applications that require memory protection from program and erase operations can use the Boot Block, Individual Block Protection, and Advanced Protection features. For applications that require a permanent solution, the Irreversible Block Locking feature provides permanent protection for memory blocks.

To meet high-density, surface mount requirements, the SST38VF6401B/6402B/6403B/6404B devices are offered in 48-lead TSOP and 48-ball TFBGA packages. See Figures 2 and 3 for pin assignments and Table 1 for pin descriptions.



Functional Block Diagram

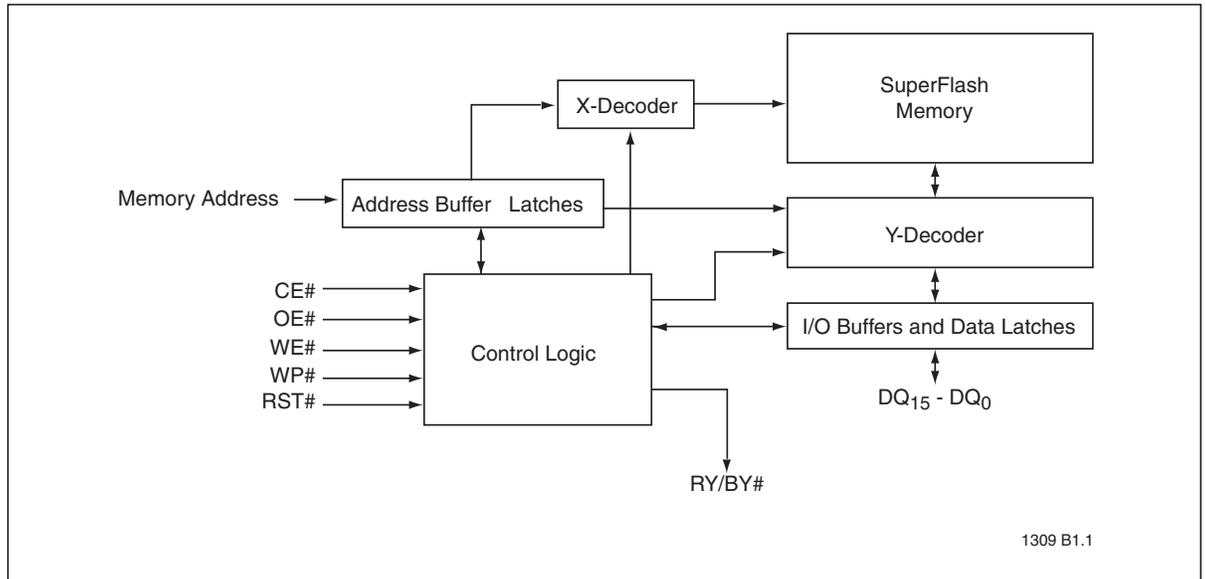


Figure 1: Functional Block Diagram



Pin Assignments

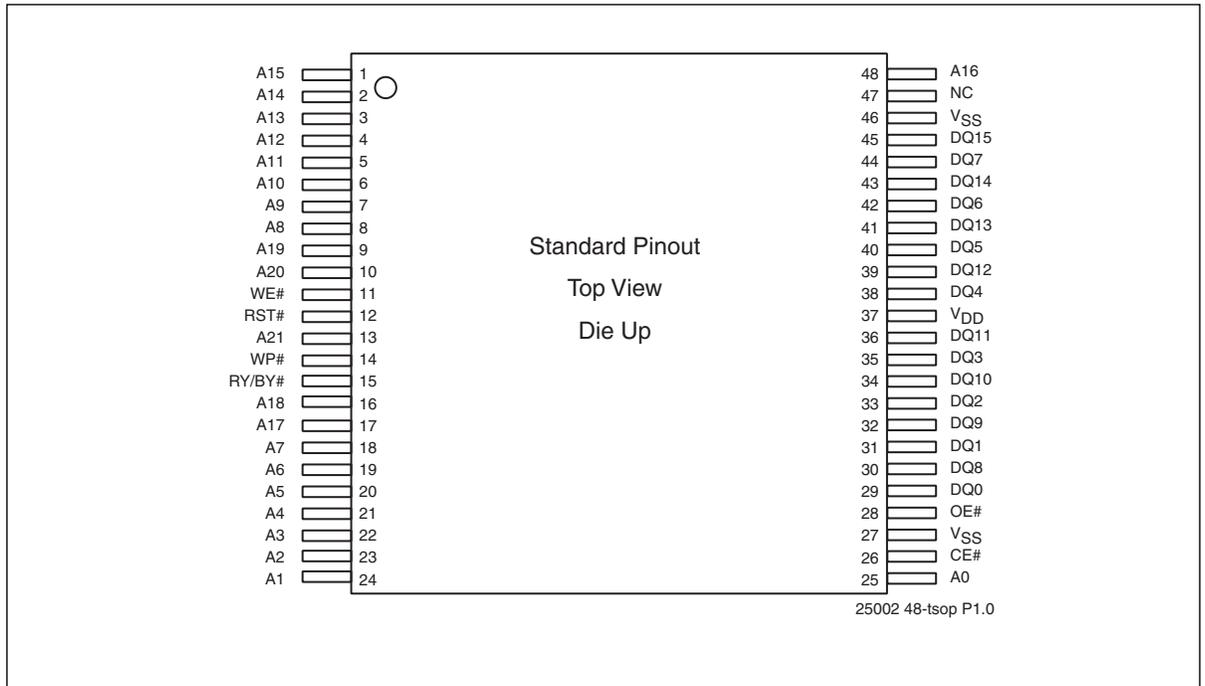


Figure 2: Pin Assignments for 48-lead TSOP

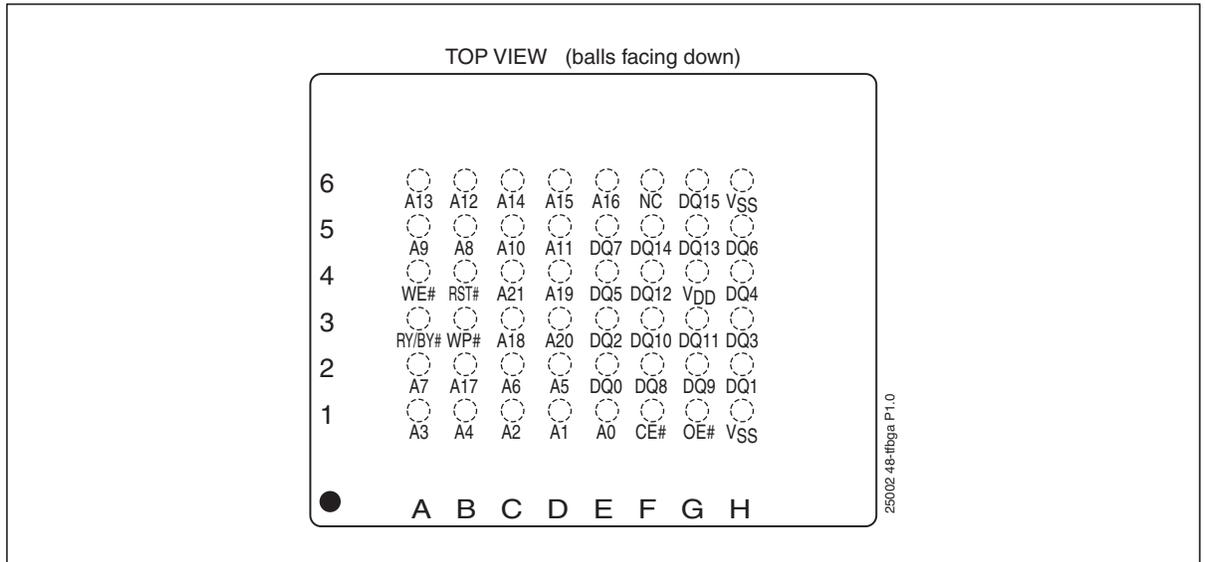


Figure 3: Pin assignments for 48-ball TFBGA



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Table 1: Pin Description

| Symbol | Pin Name | Functions |
|----------------|-------------------|--|
| $A_{MS}^1-A_0$ | Address Inputs | To provide memory addresses. During Block-Erase $A_{MS}-A_{15}$ address lines will select the block. |
| $DQ_{15}-DQ_0$ | Data Input/output | To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high. |
| WP# | Write Protect | To protect the top/bottom boot block from Erase/Program operation when grounded. |
| RY/BY# | Ready/Busy | To indicate when the device is actively programming or erasing. |
| RST# | Reset | To reset and return the device to Read mode. |
| CE# | Chip Enable | To activate the device when CE# is low. |
| OE# | Output Enable | To gate the data output buffers. |
| WE# | Write Enable | To control the Write operations. |
| V_{DD} | Power Supply | To provide power supply voltage: 2.7-3.6V |
| V_{SS} | Ground | |
| NC | No Connection | Unconnected pins. |

1. A_{MS} = Most significant address
 $A_{MS} = A_{21}$ for SST38VF6401B/6402B/6403B/6404B

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Memory Maps

Table 2: SST38VF6401Band SST38VF6402B Memory Maps

| SST38VF6401B | | | | | |
|-----------------------------------|----------|---|------------------|-------------------|------------------|
| Block ¹ | Size | Address A ₂₁ -A ₁₅ ² | VPB ³ | NVPB ³ | WP# ⁴ |
| B0 ⁴ | 32 KWord | 0000000 | YES | YES | YES |
| B1 | 32 KWord | 0000001 | YES | YES | NO |
| B2 | 32 KWord | 0000010 | YES | YES | NO |
| B3 | 32 KWord | 0000011 | YES | YES | NO |
| B4 | 32 KWord | 0000100 | YES | YES | NO |
| B5 | 32 KWord | 0000101 | YES | YES | NO |
| B6 | 32 KWord | 0000110 | YES | YES | NO |
| B7 | 32 KWord | 0000111 | YES | YES | NO |
| B8 - B119 follow the same pattern | | | | | |
| B120 | 32 KWord | 1111000 | YES | YES | NO |
| B121 | 32 KWord | 1111001 | YES | YES | NO |
| B122 | 32 KWord | 1111010 | YES | YES | NO |
| B123 | 32 KWord | 1111011 | YES | YES | NO |
| B124 | 32 KWord | 1111100 | YES | YES | NO |
| B125 | 32 KWord | 1111101 | YES | YES | NO |
| B126 | 32 KWord | 1111110 | YES | YES | NO |
| B127 | 32 KWord | 1111111 | YES | YES | NO |
| SST38VF6402B | | | | | |
| Block ¹ | Size | Address A ₂₁ -A ₁₅ ² | VPB ³ | NVPB ³ | WP# ⁵ |
| B0 | 32 KWord | 0000000 | YES | YES | NO |
| B1 | 32 KWord | 0000001 | YES | YES | NO |
| B2 | 32 KWord | 0000010 | YES | YES | NO |
| B3 | 32 KWord | 0000011 | YES | YES | NO |
| B4 | 32 KWord | 0000100 | YES | YES | NO |
| B5 | 32 KWord | 0000101 | YES | YES | NO |
| B6 | 32 KWord | 0000110 | YES | YES | NO |
| B7 | 32 KWord | 0000111 | YES | YES | NO |
| B8 - B119 follow the same pattern | | | | | |
| B120 | 32 KWord | 1111000 | YES | YES | NO |
| B121 | 32 KWord | 1111001 | YES | YES | NO |
| B122 | 32 KWord | 1111010 | YES | YES | NO |
| B123 | 32 KWord | 1111011 | YES | YES | NO |
| B124 | 32 KWord | 1111100 | YES | YES | NO |
| B125 | 32 KWord | 1111101 | YES | YES | NO |
| B126 | 32 KWord | 1111110 | YES | YES | NO |
| B127 ⁵ | 32 KWord | 1111111 | YES | YES | YES |

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- Each block, B0-B127 is 32KWord.
- X = 0 or 1. Block Address (BA) = A₂₁ - A₁₅
- Each block has an associated VPB and NVPB.
- Block B0 is the boot block.
- Block B127 is the boot block.



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Table 3: SST38VF6403B and SST38VF6404B Memory Maps (1 of 2)

| SST38VF6403B | | | | | |
|------------------------------------|----------|---|------------------|-------------------|------------------|
| Block ¹ | Size | Address A ₂₁ -A ₁₅ ² | VPB ³ | NVPB ³ | WP# ⁴ |
| B0 ^{3,4} | 4 KWord | 000000000 | YES | YES | YES |
| B1 | 4 KWord | 000000001 | YES | YES | YES |
| B2 | 4 KWord | 000000010 | YES | YES | NO |
| B3 | 4 KWord | 000000011 | YES | YES | NO |
| B4 | 4 KWord | 000000100 | YES | YES | NO |
| B5 | 4 KWord | 000000101 | YES | YES | NO |
| B6 | 4 KWord | 000000110 | YES | YES | NO |
| B7 | 4 KWord | 000000111 | YES | YES | NO |
| B8 | 32 KWord | 000001XXX | YES | YES | NO |
| B9 | 32 KWord | 000010XXX | YES | YES | NO |
| B10 | 32 KWord | 000011XXX | YES | YES | NO |
| B11 | 32 KWord | 0000100XXX | YES | YES | NO |
| B12 | 32 KWord | 0000101XXX | YES | YES | NO |
| B13 | 32 KWord | 0000110XXX | YES | YES | NO |
| B14 | 32 KWord | 0000111XXX | YES | YES | NO |
| B15 | 32 KWord | 0001000XXX | YES | YES | NO |
| B16 - B126 follow the same pattern | | | | | |
| B127 | 32 KWord | 1111000XXX | YES | YES | NO |
| B128 | 32 KWord | 1111001XXX | YES | YES | NO |
| B129 | 32 KWord | 1111010XXX | YES | YES | NO |
| B1230 | 32 KWord | 1111011XXX | YES | YES | NO |
| B1231 | 32 KWord | 1111100XXX | YES | YES | NO |
| B1232 | 32 KWord | 1111101XXX | YES | YES | NO |
| B133 | 32 KWord | 1111110XXX | YES | YES | NO |
| B134 | 32 KWord | 1111111XXX | YES | YES | NO |
| SST38VF6404B | | | | | |
| Block ¹ | Size | Address A ₂₁ -A ₁₅ ² | VPB ³ | NVPB ³ | WP# ⁵ |
| B0 | 32 KWord | 0000000XXX | YES | YES | NO |
| B1 | 32 KWord | 0000001XXX | YES | YES | NO |
| B2 | 32 KWord | 0000010XXX | YES | YES | NO |
| B3 | 32 KWord | 0000011XXX | YES | YES | NO |
| B4 | 32 KWord | 0000100XXX | YES | YES | NO |
| B5 | 32 KWord | 0000101XXX | YES | YES | NO |
| B6 | 32 KWord | 0000110XXX | YES | YES | NO |
| B7 | 32 KWord | 0000111XXX | YES | YES | NO |
| B8 - B119 follow the same pattern | | | | | |
| B120 | 32 KWord | 1111000XXX | YES | YES | NO |
| B121 | 32 KWord | 1111001XXX | YES | YES | NO |
| B122 | 32 KWord | 1111010XXX | YES | YES | NO |
| B123 | 32 KWord | 1111011XXX | YES | YES | NO |
| B124 | 32 KWord | 1111100XXX | YES | YES | NO |



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Table 3: SST38VF6403B and SST38VF6404B Memory Maps (Continued) (2 of 2)

| | | | | | |
|----------------------|----------|------------|-----|-----|-----|
| B125 | 32 KWord | 1111101XXX | YES | YES | NO |
| B126 | 32 KWord | 1111110XXX | YES | YES | NO |
| B127 ^{3, 5} | 4 KWord | 1111111000 | YES | YES | NO |
| B128 | 4 KWord | 1111111001 | YES | YES | NO |
| B129 | 4 KWord | 1111111010 | YES | YES | NO |
| B130 | 4 KWord | 1111111011 | YES | YES | NO |
| B131 | 4 KWord | 1111111100 | YES | YES | NO |
| B132 | 4 KWord | 1111111101 | YES | YES | NO |
| B133 | 4 KWord | 1111111110 | YES | YES | YES |
| B134 | 4 KWord | 1111111111 | YES | YES | YES |

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- Each block, B0-B127 is 32KWord.
- X = 0 or 1. Block Address (BA) = $A_{21} - A_{15}$
- Each block has an associated VPB and NVPB, except for some blocks in SST38VF6403B and SST38VF6404B.
In SST38VF6403B, Block B0 does not have a single VPB or NVPB for all 32 KWords. Instead, each block (4 KWord) in Block B0 has its own VPB and NVPB.
In SST38VF6404B, Block B127 does not have a single VPB or NVPB for all 32 KWords. Instead, each block (4 KWord) in Block B127 has its own VPB and NVPB.
- The 8KWord boot block consists of S0 and S1 in Block B0.
- The 8KWord boot block consists of S1022 and S1023 in Block B127.



Device Operation

The memory operations functions of these devices are initiated using commands written to the device using standard microprocessor Write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

The SST38VF6401B/6402B/6403B/6404B also have the Auto Low Power mode which puts the device in a near-standby mode after data has been accessed with a valid Read operation. This reduces the I_{DD} active read current from typically 6 mA to typically 5 μ A. The device requires no access time to exit the Auto Low Power mode after any address transition or control signal transition used to initiate another Read cycle. The device does not enter Auto-Low Power mode after power-up with CE# held steadily low, until the first address transition or CE# is driven high.

Read

The Read operation of the SST38VF6401B/6402B/6403B/6404B is controlled by CE# and OE#, both of which have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to Figure 5, the Read cycle timing diagram, for further details.

Page Read

The Page Read operation utilizes an asynchronous method that enables the system to read data from the SST38VF6401B/6402B/6403B/6404B at a faster rate. This operation allows users to read an eight-word page of data at an average speed of 33 ns per word.

In Page Read, the initial word read from the page requires T_{ACC} to be valid, while the remaining seven words in the page require only T_{PACC}. All eight words in the page have the same address bits, A₂₁-A₃, which are used to select the page. Address bits A₂-A₀ are toggled, in any order, to read the words within the page.

The Page Read operation of the SST38VF6401B/6402B/6403B/6404B is controlled by CE# and OE#. Both CE# and OE# must be low for the system to obtain data from the output pins. CE# controls device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to Figure 6, the Page Read cycle timing diagram, for further details.

Word-Program Operation

The SST38VF6401B/6402B/6403B/6404B can be programmed on a word-by-word basis. Before programming, the block where the word exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load word address and word data. During the Word-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 7 μ s. See Figures 7 and 8 for WE# and CE# controlled Program operation timing diagrams and Figure 23 for flowcharts.



During the Program operation, the only valid reads are Data# Polling, Toggle Bits, and RY/BY#. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored. During the command sequence, WP# should be statically held high or low.

When programming more than a few words, SST recommends Write-Buffer Programming.

Write-Buffer Programming

The SST38VF6401B/6402B/6403B/6404B offer Write-Buffer Programming, a feature that enables faster effective word programming. To use this feature, write up to 16 words with the Write-to-Buffer command, then use the Program Buffer-to-Flash command to program the Write-Buffer to memory.

The Write-to-Buffer command consists of between 5 and 20 write cycles. The total number of write cycles in the Write-to-Buffer command sequence is equal to the number of words to be written to the buffer plus four.

The first three cycles in the command sequence tell the device that a Write-to-Buffer operation will begin.

The fourth cycle tells the device the number of words to be written into the buffer and the block address of these words. Specifically, the write cycle consists of a block address and a data value called the Word Count (WC), which is the number of words to be written to the buffer minus one. If the WC is greater than 15, the maximum buffer size minus 1, then the operation aborts.

For the fifth cycle, and all subsequent cycles of the Write-to-Buffer command, the command sequence consists of the addresses and data of the words to be written into the buffer. All of these cycles must have the same $A_{21} - A_4$ address, otherwise the operation aborts. The number of Write cycles required is equal to the number of words to be written into the Write-Buffer, which is equal to WC plus one. The correct number of Write cycles must be issued or the operation will abort. Each Write cycle decrements the Write-Buffer counter, even if two or more of the Write cycles have identical address values. Only the final data loaded for each buffer location is held in the Write-Buffer.

Once the Write-to-Buffer command sequence is completed, the Program Buffer-to-Flash command should be issued to program the Write-Buffer contents to the specified block in memory. The block address (i.e. $A_{21} - A_{15}$) in this command must match the block address in the 4th write cycle of the Write-to-Buffer command or the operation aborts. See Table 11 for details on Write-to-Buffer and Program-Buffer-to-Flash commands.

While issuing these command sequences, the Write-Buffer Programming Abort detection bit (DQ1) indicates if the operation has aborted. There are several cases in which the device can abort:

- In the fourth write cycle of the Write-to-Buffer command, if the WC is greater than 15, the operation aborts.
- In the fifth and all subsequent cycles of the Write-to-Buffer command, if the address values, $A_{21} - A_4$, are not identical, the operation aborts.
- If the number of write cycles between the fifth to the last cycle of the Write-to-Buffer command is greater than WC + 1, the operation aborts.
- After completing the Write-to-Buffer command sequence, issuing any command other than the Program Buffer-to-Flash command, aborts the operation.
- Loading a block address, i.e. $A_{21}-A_{15}$, in the Program Buffer-to-Flash command that does not match the block address used in the Write-to-Buffer command aborts the operation.



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If the Write-to-Buffer or Program Buffer-to-Flash operation aborts, then $DQ_1 = 1$ and the device enters Write-Buffer-Abort mode. To execute another operation, a Write-to-Buffer Abort-Reset command must be issued to clear DQ_1 and return the device to standard read mode.

After the Write-to-Buffer and Program Buffer-to-Flash commands are successfully issued, the programming operation can be monitored using Data# Polling, Toggle Bits, and RY/BY#.

Block-Erase Operations

The Block-Erase operation allows the system to erase the device on a block-by-block basis.

The Block-Erase architecture is based on block size of 32 KWords. In SST38VF6401B and SST38VF6402B devices, the Block-Erase command can erase any 32KWord Block (B0-B127). For the non-uniform boot block devices, SST38VF6403B and SST38VF6404B, the Block-Erase command can erase any 32 KWord block except the block that contains the boot area. In the boot area, Block-Erase only erases a 4KWord block.

The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The block address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. The RY/BY# pin can also be used to monitor the erase operation. For more information, see Figures 14 and for timing waveforms and Figure 28 for the flowchart.

Any commands, other than Erase-Suspend, issued during the Block-Erase operation are ignored. Any attempt to Block-Erase memory inside a block protected by Volatile Block Protection, Non-Volatile Block Protection, or WP# (low) will be ignored. During the command sequence, WP# should be statically held high or low.

Erase-Suspend/Erase-Resume Commands

The Erase-Suspend operation temporarily suspends a Block-Erase operation thus allowing data to be read or programmed into any block that is not engaged in an Erase operation. The operation is executed with a one-byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode within 20 μ s (max) after the Erase-Suspend command had been issued. Valid data can be read, using a Read or Page Read operation, from any block that is not being erased. Reading at an address location within Erase-Suspended blocks will output DQ_2 toggling and DQ_6 at '1'. While in Erase-Suspend, a Word-Program or Write-Buffer Programming operation is allowed anywhere except the block selected for Erase-Suspend.

To resume a suspended Block-Erase operation, the system must issue the Erase-Resume command. The operation is executed by issuing one byte command sequence with Erase-Resume command (30H) at any address in the last Byte sequence.

When an erase operation is suspended, or re-suspended, after resume the cumulative time needed for the erase operation to complete is greater than the erase time of a non-suspended erase operation. If the hold time from Erase-Resume to the next Erase-Suspend operation is less than 200 μ s, the accumulative erase time can become very long. Therefore, after issuing an Erase-Resume command, the system must wait at least 200 μ s before issuing another Erase-Suspend command. The Erase-Resume command will be ignored until any program operations initiated during Erase-Suspend are complete.



Bypass mode can be entered while in Erase-Suspend, but only Bypass Word-Program is available for those blocks that are not suspended. Bypass Block-Erase, Bypass Chip-Erase, Erase-Suspend, and Erase-Resume are not available. In order to resume an Erase operation, the Bypass mode must be exited before issuing Erase-Resume. For more information about Bypass mode, see "Bypass Mode" on page 17.

Chip-Erase Operation

The SST38VF6401B/6402B/6403B/6404B devices provide a Chip-Erase operation, which erases the entire memory array to the '1' state. This operation is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid reads are Toggle Bit, Data# Polling, or RY/BY#. See Table 11 for the command sequence, Figure 13 for timing diagram, and Figure 28 for the flowchart. Any commands issued during the Chip-Erase operation are ignored. If WP# is low, or any VPBs or NVPBs are in the protect state, any attempt to execute a Chip-Erase operation is ignored. During the command sequence, WP# should be statically held high or low.

Write Operation Status Detection

To optimize the system Write cycle time, the SST38VF6401B/6402B/6403B/6404B provide two software means to detect the completion of a Write (Program or Erase) cycle. The software detection includes two status bits: Data# Polling (DQ₇) and Toggle Bit (DQ₆). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system. Therefore, Data# Polling or Toggle Bit may be read concurrent with the completion of the write cycle. If this occurs, the system may possibly get an incorrect result from the status detection process. For example, valid data may appear to conflict with either DQ₇ or DQ₆. To prevent false results, upon detection of failures, the software routine should loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle, otherwise the failure is valid.

For the Write-Buffer Programming feature, DQ₁ informs the user if either the Write-to-Buffer or Program Buffer-to-Flash operation aborts. If either operation aborts, then DQ₁ = 1. DQ₁ must be cleared to '0' by issuing the Write-to-Buffer Abort Reset command.

The SST38VF6401B/6402B/6403B/6404B also provide a RY/BY# signal. This signal indicates the status of a Program or Erase operation.

If a Program or Erase operation is attempted on a protected block, the operation will abort. After the device initiates an abort, the corresponding Write Operation Status Detection Bits will stay active for approximately 200ns (program or erase) before the device returns to read mode.

For the status of these bits during a Write operation, see Table 4.

Data# Polling (DQ₇)

When the SST38VF6401B/6402B/6403B/6404B are in an internal Program operation, any attempt to read DQ₇ will produce the complement of true data. For a Program Buffer-to-Flash operation, DQ₇ is the complement of the last word loaded in the Write-Buffer using the Write-to-Buffer command. Once



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the Program operation is completed, DQ₇ will produce valid data. Note that even though DQ₇ may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid. Valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 μ s.

During an internal Erase operation, any attempt to read DQ₇ will produce a '0'. Once the internal Erase operation is completed, DQ₇ will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Block- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 11 for Data# Polling timing diagram and Figure 25 for a flowchart.

Toggle Bits (DQ₆ and DQ₂)

During the internal Program or Erase operation, any consecutive attempts to read DQ₆ will produce alternating '1's and '0's, i.e., toggling between '1' and '0'. When the internal Program or Erase operation is completed, the DQ₆ bit will stop toggling, and the device is then ready for the next operation. For Block- or Chip-Erase, the toggle bit (DQ₆) is valid after the rising edge of sixth WE# (or CE#) pulse. DQ₆ will be set to '1' if a Read operation is attempted on an Erase-Suspended Block. If Program operation is initiated in a block not selected in Erase-Suspend mode, DQ₆ will toggle.

An additional Toggle Bit is available on DQ₂, which can be used in conjunction with DQ₆ to check whether a particular block is being actively erased or erase-suspended. Table 4 shows detailed bit status information. The Toggle Bit (DQ₂) is valid after the rising edge of the last WE# (or CE#) pulse of Write operation. See Figure 12 for Toggle Bit timing diagram and Figure 25 for a flowchart.

DQ₁

If an operation aborts during a Write-to-Buffer or Program Buffer-to-Flash operation, DQ₁ is set to '1'. To reset DQ₁ to '0', issue the Write-to-Buffer Abort Reset command to exit the abort state. A power-off/power-on cycle or a Hardware Reset (RST# = 0) will also clear DQ₁.

DQ₃

DQ₃ indicates if a Block-Erase operation has begun. DQ₃ is '0' until the device starts the erasure. Once, Block-Erase begins, DQ₃ is set to '1'. While DQ₃ is '0', additional blocks to be erased can be written to the device.

**RY/BY#**

The RY/BY# pin can be used to determine the status of a Program or Erase operation. The RY/BY# pin is valid after the rising edge of the final WE# pulse in the command sequence. If RY/BY# = 0, then the device is actively programming or erasing. If RY/BY# = 1, the device is in Read mode. The RY/BY# pin is an open drain output pin. This means several RY/BY# can be tied together with a pull-up resistor to V_{DD}.

Table 4: Write Operation Status

| Status | | DQ ₇ ¹ | DQ ₆ | DQ ₃ | DQ ₂ ¹ | DQ ₁ | RY/BY# ² |
|-------------------------|-------------------------------------|--------------------------------|-----------------|-----------------|------------------------------|-----------------|---------------------|
| Normal Operation | Standard Program | DQ ₇ # | Toggle | N/A | No Toggle | 0 | 0 |
| | Standard Erase | 0 | Toggle | 1 | Toggle | N/A | 0 |
| Erase-Suspend Mode | Read from Erase-Suspended Block | 1 | No toggle | N/A | Toggle | N/A | 1 |
| | Read from Non-Erase-Suspended Block | Data | Data | Data | Data | Data | 1 |
| | Program | DQ ₇ # | Toggle | N/A | N/A | N/A | 0 |
| Program Buffer-to-Flash | Busy | DQ ₇ # ³ | Toggle | Not allowed | N/A | 0 | 0 |
| | Abort | DQ ₇ # ³ | Toggle | N/A | N/A | 1 | 0 |

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1. DQ₇ and DQ₂ require a valid address when reading status information.
2. RY/BY# is an open drain pin. RY/BY# is high in Read mode, and Read in Erase-Suspend mode.
3. During a Program Buffer-to-Flash operation, the datum on the DQ₇ pin is the complement of DQ₇ of the last word loaded in the Write-Buffer using the Write-to-Buffer command.

Data Protection

The SST38VF6401B/6402B/6403B/6404B provide both hardware and software features to protect non-volatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.



Hardware Block Protection

The SST38VF6402B and SST38VF6404B devices support top hardware block protection, which protects the top boot block of the device. For SST38VF6402B, the boot block consists of the top 32 KWord block, and for SST38VF6404B the boot block consists of the top two 4 KWord blocks (8 KWord total).

The SST38VF6401B and SST38VF6403B devices support bottom hardware block protection, which protects the bottom boot block of the device. For SST38VF6401B, the boot block consists of the bottom 32 KWord block, and for SST38VF6403B the Boot Block consists of the bottom two 4 KWord blocks (8 KWord total). The boot block addresses are described in Table 5.

Table 5: Boot Block Address Ranges

| Product | Size | Address Range |
|--|-------|------------------|
| Bottom Boot Uniform SST38VF6401B | 32 KW | 000000H-007FFFFH |
| Top Boot Uniform SST38VF6402B | 32 KW | 3F8000H-3FFFFFFH |
| Bottom Boot Non-Uniform SST38VF6403B | 8 KW | 000000H-001FFFFH |
| Top Boot Non-Uniform SST38VF6404B | 8 KW | 3FE000H-3FFFFFFH |

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Program and Erase operations are prevented on the Boot Block when WP# is low. If WP# is left floating, it is internally held high via a pull-up resistor. When WP# is high, the Boot Block is unprotected, which allows Program and Erase operations on that area.

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP} , any in-progress operation will terminate and return to Read mode. When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place. See Figure 19 for more information.

The interrupted Erase or Program operation must be re-initiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

The SST38VF6401B/6402B/6403B/6404B devices implement the JEDEC approved Software Data Protection (SDP) scheme for all data alteration operations, such as Program and Erase. These devices are shipped with the Software Data Protection permanently enabled. See Table 11 for the specific software command codes.

All Program operations require the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations. SDP for Erase operations is similar to Program, but a six-byte load sequence is required for Erase operations.

During SDP command sequence, invalid commands will abort the device to read mode within T_{RC} . The contents of DQ₁₅-DQ₈ can be V_{IL} or V_{IH} , but no other value, during any SDP command sequence.



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The SST38VF6401B/6402B/6403B/6404B devices provide Bypass Mode, which allows for reduced Program and Erase command sequence lengths. In this mode, the SDP portion of Program and Erase command sequences are omitted. See “Bypass Mode” on page 17 for further details.

Common Flash Memory Interface (CFI)

The SST38VF6401B/6402B/6403B/6404B contain Common Flash Memory Interface (CFI) information that describes the characteristics of the device. In order to enter the CFI Query mode, the system can write a one-byte sequence using a standard CFI Query Entry command. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 13 through 16.

The system must write the CFI Exit command to return to Read mode. Note that the CFI Exit command is ignored during an internal Program or Erase operation. See Table 11 for software command codes, Figures 16 and 17 for timing waveform, and Figures 26 and 27 for flowcharts.

Product Identification

The Product Identification mode identifies the devices as the SST38VF6401B, SST38VF6402B, SST38VF6403B, or SST38VF6404B, and the manufacturer as SST. See Table 6 for specific address and data information. Product Identification mode is accessed through software operations. The software Product Identification operations identify the part, and can be useful when using multiple manufacturers in the same socket. For details, see Table 11 for software operation, Figure 15 for the software ID Entry and Read timing diagram, and Figure 26 for the software ID Entry command sequence flowchart.

Table 6: Product Identification

| | Address | Data | Address | Data | Address | Data |
|-------------------|---------|-------|---------|-------|---------|-------|
| Manufacturer's ID | 00H | BFH | | | | |
| Device ID | | | | | | |
| SST38VF6401B | 01H | 227EH | 0EH | 220CH | 0FH | 2200H |
| SST38VF6402B | 01H | 227EH | 0EH | 220CH | 0FH | 2201H |
| SST38VF6403B | 01H | 227EH | 0EH | 2210H | 0FH | 2200H |
| SST38VF6404B | 01H | 227EH | 0EH | 2210H | 0FH | 2201H |

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While in Product Identification mode, the Read Block Protection Status command determines if a block is protected. The status returned indicates if the block has been protected, but does not differentiate between Volatile Block Protection and Non-Volatile Block Protection. See Table 11 for further details.

The Read-Irreversible Block-Lock Status command indicates if the Irreversible Block Command has been issued. If $DQ_0 = 0$, then the Irreversible Lock command has been previously issued.

In order to return to the standard Read mode, the software Product Identification mode must be exited. The exit is accomplished by issuing the software ID Exit command sequence, which returns the device to the Read mode. See Table 11 for software command codes, Figure 17 for timing waveform, and Figures 26 and 27 for flowcharts.



Security ID

The SST38VF6401B/6402B/6403B/6404B devices offer a Security ID feature. The Secure ID space is divided into two segments — one factory programmed 128 bit segment and one user programmable 248 word segment. See Table 7 for address information. The first segment is programmed and locked at SST and contains a 128 bit Unique ID which uniquely identifies the device. The user segment is left un-programmed for the customer to program as desired.

Table 7: Address Range for Sec ID

| | Size | Address |
|---------------|----------|-------------|
| SST Unique ID | 128 bits | 000H – 007H |
| User | 248 W | 008H – 0FFH |

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The user segment of the Security ID can be programmed in several ways. For smaller datasets, use the Security ID Word-Program command for word-programming. To program larger sets of data more quickly, use the SEC ID Entry command to enter the Secure ID space. Once in the Secure ID space, for smaller data sets, use the Word-Program command to program data. To program larger sets of data more quickly, use the Write-Buffer Programming feature. Note that Bypass Mode is not available.

To detect end-of-write for the SEC ID, read the toggle bits. Do not use Data# Polling to detect end of Write. Once the programming is complete, lock the Sec ID by issuing the User Sec ID Program Lock-Out command or by programming bit '0' in the PSR with the PSR Program command. Locking the Sec ID disables any corruption of this space. Note that regardless of whether or not the Sec ID is locked, the Sec ID segments can not be erased.

The Secure ID space can be queried by executing a three-byte command sequence with Enter Sec ID command (88H) at address 555H in the last byte sequence. To exit this mode, the Exit Sec ID command should be executed. Refer to Table 11 for software commands and Figures 26 and 27 for flow charts.

Bypass Mode

Bypass mode shortens the time needed to issue program and erase commands by reducing these commands to two write cycles each. After using the Bypass Entry command to enter the Bypass mode, only the Bypass Word-Program, Bypass Block Erase, Bypass Chip Erase, Erase-Suspend, and Erase-Resume commands are available. The Bypass Exit command exits Bypass mode. See Table 11 for further details.

Entering Bypass Mode while already in Erase-Suspend limits the available commands. See “Erase-Suspend/Erase-Resume Commands” on page 11 for more information.



Protection Settings Register (PSR)

The Protection Settings Register (PSR) is a user-programmable register that allows for further customization of the SST38VF6401B/6402B/6403B/6404B protection features. The 16-bit PSR provides four One Time Programmable (OTP) bits for users, each of which can be programmed individually. However, once an OTP bit is programmed to '0', the value cannot be changed back to a '1'. The other 12 bits of the PSR are reserved. See Table 8 for the definition of all 16-bits of the PSR.

Table 8: PSR Bit Definitions

| Bit | Default from Factory | Definition |
|-----------------------------------|----------------------|---|
| DQ ₁₅ -DQ ₅ | FFFh | Reserved |
| DQ ₄ | 1 | VPB power-up / hardware reset state 0 = all protected 1 = all unprotected |
| DQ ₃ | 1 | Reserved |
| DQ ₂ | 1 | Password mode 0 = Password only mode 1 = Pass-Through mode |
| DQ ₁ | 1 | Pass-Through mode 0 = Pass-Through only mode 1 = Pass-Through mode |
| DQ ₀ | 1 | SEC ID Lock Out Bit 0 = locked 1 = unlocked |

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Note that DQ₄, DQ₂, DQ₁, DQ₀ do not have to be programmed at the same time. In addition, DQ₂ and DQ₁ cannot both be programmed to '0'. The valid combinations of states of DQ₂ and DQ₁ are shown in Table 9.

Table 9: Valid DQ₂ and DQ₁ Combinations

| Combination | Definition |
|--|-------------------------------------|
| DQ ₂ , DQ ₁ = 11 | Pass-Through mode (factory default) |
| DQ ₂ , DQ ₁ = 10 | Pass-Through only mode |
| DQ ₂ , DQ ₁ = 01 | Password only mode |
| DQ ₂ , DQ ₁ = 00 | Not Allowed |

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The PSR can be accessed by issuing the PSR Entry command. Users can then use the PSR Program and PSR Read commands. The PSR Exit command must be issued to leave this mode. See Table 11 for further details.



Individual Block Protection

The SST38VF6401B/6402B/6403B/6404B provide two methods for Individual Block protection: Volatile Block Protection and Non-Volatile Block Protection. Data in protected blocks cannot be altered.

Volatile Block Protection

The Volatile Block Protection feature provides a faster method than Non-Volatile Protection to protect and unprotect 32 KWord blocks. Each block has its own Volatile Protection Bit (VPB). In the SST38VF6401B/6402B, the 32 KWord boot block also has a VPB. In the SST38VF6403B/6404B devices, each of the two 4 KWord blocks in the 8 KWord boot area has its own VPB.

After using the Volatile Block Protection Mode Entry command to enter the Volatile Block Protection mode, individual VPBs can be set or reset with VPB Set/Clear, or be read with VPB Status Read. If the VPB is '0', then the block is protected from Program and Erase. If the VPB is '1', then the block is unprotected. The Volatile Block Protection Exit command must be issued to exit Volatile Block Protection mode. See Table 11 for further details on the commands and Figure 30 for a flow chart.

If the device experiences a hardware reset or a power cycle, all the VPBs return to their default state as determined by user-programmable bit DQ₄ in the PSR. If DQ₄ is '0', then all VPBs default to '0' (protected). If DQ₄ is '1', then all VPBs default to '1' (unprotected).

Non-Volatile Block Protection

The Non-Volatile Block Protection feature provides protection to individual blocks using Non-Volatile Protection Bits (NVPBs). Each block has its own Non-Volatile Protection Bit. In the SST38VF6401B/2, the 32 KWord boot block also has its own NVPB. In the SST38VF6403B/6404B, each 4 KWord block in the 8KWord boot area has its own NVPB. All NVPBs come from the factory set to '1', the unprotected state.

Use the Non-Volatile Block Protection Mode Entry command to enter the Non-Volatile Block Protection mode. Once in this mode, the NVPB Program command can be used to protect individual blocks by setting individual NVPBs to '0'. The time needed to program an NVPB is two times T_{BP}, which is a maximum of 20μs. The NVPB Status Read command can be used to check the protection state of an individual NVPB.

To change an NVPB to '1', the unprotected state, the NVPB must be erased using NVPBs Erase command. This command erases all NVPBs to '1'. NVPB Program should be used to set the NVPBs of any blocks that are to be protected before exiting the Non-Volatile Block Protection mode. See Table 11 and Figure 31 for further details.

Upon a power cycle or hardware reset, the NVPBs retain their states. Memory areas that are protected using Non-Volatile Block Protection remain protected. The NVPB Program and NVPBs Erase commands are permanently disabled once the Irreversible Block Lock command is issued. See "Irreversible Block Locking" on page 22 for further information.



Advanced Protection

The SST38VF6401B/6402B/6403B/6404B provide Advanced Protection features that allow users to implement conditional access to the NVPBs. Specifically, Advanced Protection uses the Global Lock Bit to protect the NVPBs. If the Global Lock bit is '0' then all the NVPBs states are frozen and cannot be modified in any mode. If the Global Lock bit is '1', then all the NVPBs can be modified in Non-Volatile Block Protection mode. After using the Global Lock of NVPBs Entry command to enter the Global Lock of NVPBs mode, the Global Lock Bit can be activated by issuing a Set Global Lock Bit command, which sets the Global Lock Bit to '0'. The Global Lock bit cannot be set to '1' with this command. The status of the bit can be read with the Global Lock Bit Status command. Use the Global Lock of NVPBs Exit command to exit Global Lock of NVPBs mode. See Table 11 and Figure 32 for further details.

The steps used to change the Global Lock Bit from '0' to '1', to allow access to the NVPBs, depend on whether the device has been set to use Pass-Through or Password mode. When using Advanced Protection, select either Pass-Through only mode or Password only mode by programming the DQ₂ and DQ₁ bits in the PSR. Although the factory default is Pass-Through mode (DQ₂ = 1, DQ₁ = 1), the user should explicitly chose either Pass-Through only mode (DQ₂ = 1, DQ₁ = 0), or Password only mode (DQ₂ = 0, DQ₁ = 1). Keeping the SST38VF6401B/6402B/6403B/6404B in the factory default Pass-Through mode leaves the device open to unauthorized changes of DQ₂ and DQ₁ in the PSR. See "Protection Settings Register (PSR)" on page 18. for more information about the PSR.

Pass-Through Mode (DQ₂, DQ₁ = 1,0)

The Pass-Through Mode allows the Global Lock Bit state to be cleared to '1' by a power-down power-up sequence or a hardware reset (RST# pin = 0). No password is required in Pass-Through mode.

To set the Global Lock Bit to '0', use the Set Global Lock Bit command while in the Global Lock of NVPBs mode. Select the Pass-Through only mode by programming PSR bit DQ₂ = 1 and DQ₁ = 0.

Password Mode (DQ₂, DQ₁ = 0,1)

In the Password Mode, the Global Lock Bit is set to '0' by the Set Global Lock Bit command, a power-down power-up sequence, or a hardware reset (RST# pin = 0). Select the Password only mode by programming PSR bit DQ₂ = 0 and DQ₁ = 1. Note that when the PSR Program command is issued in Password mode, the Global Lock bit is automatically set to '0'.

In contrast to the Pass-Through Mode, in the Password mode, the only way to clear the Global Lock Bit to '1' is to submit the correct 64-bit password using the Submit Password command in Password Commands Mode. The words of the password can be submitted in any order as long as each 16 bit section of the password is matched with its correct address. After the entire 64 bit password is submitted, the device takes approximately 1 μs to verify the password. A subsequent Submit Password command cannot be issued until this verification time has elapsed.

The 64-bit password must be chosen by the user before programming the DQ₂ and DQ₁ OTP bits of the PSR to choose Password Mode. The default 64 bit password on the device from the factory is FFFFFFFFFFFFFFFFFFh.

Enter the Password Commands mode by issuing the Password Commands Entry command. Then, use the Password Program command to program the desired password. Use caution when programming the password because there is no method to reset the password to FFFFFFFFFFFFFFFFFFh. Once a password bit has been set to '0', it cannot be changed back to '1'. See Table 11 for further details about Password-related commands.



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The password can be read using the Password Read command to verify the desired password has been programmed. SST recommends testing the password before permanently choosing Password Mode.

To test the password, do the following:

1. Enter the Global Lock of NVPBs mode.
2. Set the Global Lock Bit to '0', and verify the value.
3. Exit the Global Lock of NVPBs mode.
4. Enter the Password Commands mode.
5. Submit the 64-bit password with the Submit Password command.
6. Wait 2 μ s for the device to verify the password.
7. Exit the Password Commands mode.
8. Re-enter the Global Lock of NVPBs mode
9. Read the Global Lock Bit with the Global Lock Bit Status Read command. The Global Lock bit should now be '1'.

After verifying the password, program the DQ₂ and DQ₁ OTP bits of the PSR to explicitly choose Password mode. Once the Password mode has been selected, the Password Read and Password Program commands are permanently disabled. There is no longer any method for reading or modifying the password. In addition, SST is unable to read or modify the password. If a Password Read command is issued while in Password mode, the data presented for each word of the password is FFFFh.

If the Password Mode is not explicitly chosen in the PSR, then the password can still be read and modified. Therefore, SST strongly recommends that users explicitly choose Password Mode in the PSR.



Irreversible Block Locking

The SST38VF6401B/6402B/6403B/6404B provides Irreversible Block Locking, a feature that allows users to customize the size of Read-Only Memory (ROM) on the device and provides more flexibility than One-Time Programmable (OTP) memory.

Applying Irreversible Block Locking turns user-selected memory areas into ROM by permanently disabling Program and Erase operations to these chosen areas. Any area that becomes ROM cannot be changed back to Flash.

Any memory blocks in the main memory, including boot blocks, can be irreversibly locked. In non-uniform boot block devices (SST38VF6403B and SST38VF6404B) each 4 KW block in the boot area can be irreversibly locked. If desired, all blocks in the main memory can be irreversibly locked.

To use Irreversible Block Locking do the following:

1. Global Lock Bit should be '1'. The Irreversible Block Lock command is disabled when Global Lock Bit is '0'.
2. Enter the Non-Volatile Block Protection mode.
3. Use the NVPB Program command to protect only the blocks that are to be changed into ROM.
4. Exit the Non-Volatile Block Protection mode.
5. Issue the Irreversible Block Lock command (see Table 11 for details).

The Irreversible Block Lock command can only be used once. Issuing the command after the first time has no effect on the device.

Important: Once the Irreversible Block Lock command is used, the state of the NVPBs can no longer be changed or overridden. Therefore, the following features no longer have any effect on the device:

- Global Lock of NVPBs feature
- Password feature
- NVPB Program command
- NVPB Erase command
- DQ2 and DQ1 of PSR

In addition, WP# has no effect on any memory in the boot block area that has been irreversibly locked.

To verify whether the Irreversible Block Lock command has already been issued, enter the Product ID mode and read address 5FEH. If $DQ_0 = 0$, then Irreversible Block Lock has already been executed. When using this feature to determine if a specific block is ROM, use the NVPB Status Read.



Operations

Table 10: Operation Modes Selection

| Mode | CE# | OE# | WE# | RST# | WP# | DQ | Address |
|------------------------|-----------------|-----------------|-----------------|-----------------|---|-----------------------------|--------------------------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | H | X | D _{OUT} | A _{IN} |
| Program | V _{IL} | V _{IH} | V _{IL} | H | V _{IL} /V _{IH} ¹ | D _{IN} | A _{IN} |
| Erase | V _{IL} | V _{IH} | V _{IL} | H | V _{IL} /V _{IH} ¹ | X ² | Block address, XXH for Chip-Erase |
| Standby | V _{IH} | X | X | V _{IH} | X | High Z | X |
| Write Inhibit | X | V _{IL} | X | X | X | High Z/ D _{OUT} | X |
| Product Identification | X | X | V _{IH} | H | X | High Z/ D _{OUT} | X |
| Reset | X | X | X | L | X | High Z | X |
| Software Mode | V _{IL} | V _{IH} | V _{IL} | H | X | See Table 11 | See Table 11 |

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1. WP# can be V_{IL} when programming or erasing outside of the bootblock.
WP# must be V_{IH} when programming or erasing inside the bootblock area.
2. X can be V_{IL} or V_{IH}, but no other value.

Table 11: Software Command Sequence (1 of 4)

| Command Sequence | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | | 4th Bus Cycle | | 5th Bus Cycle | | 6th Bus Cycle | | 7th Bus Cycle | |
|---------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| | Addr ¹ | Data ² |
| Read³ | WA | Data | | | | | | | | | | | | |
| Page Read³ | WA ₀ | Data ₀ | WA ₁ | Data ₁ | WA ₂ | Data ₂ | WA ₃ | Data ₃ | | | | | | |
| Word-Program | 555H | AAH | 2AAH | 55H | 555H | A0H | WA | Data | | | | | | |
| Reset | XXH | F0H | | | | | | | | | | | | |
| Write-Buffer Programming | | | | | | | | | | | | | | |
| Write-to-Buffer ⁴ | 555H | AAH | 2AAH | 55H | BA | 25H | BA | WC | WA _x | Data | WA _x | Data | WA _x | Data |
| Program Buffer-to-Flash | BA _x | 29H | | | | | | | | | | | | |
| Write-to-Buffer Abort-Reset | 555H | AAH | 2AAH | 55H | 555H | F0H | | | | | | | | |
| Bypass Mode⁵ | | | | | | | | | | | | | | |
| Bypass Mode Entry | 555H | AAH | 2AAH | 55H | 555H | 20H | | | | | | | | |
| Bypass Word-Program | XXXH | A0H | WA | Data | | | | | | | | | | |
| Bypass Block Erase | XXXH | 80H | BA | 30H | | | | | | | | | | |
| Bypass Chip Erase | XXXH | 80H | 555H | 10H | | | | | | | | | | |
| Bypass Mode Exit | XXXH | 90H | XXXH | 00H | | | | | | | | | | |



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Table 11: Software Command Sequence (Continued) (2 of 4)

| Command Sequence | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | | 4th Bus Cycle | | 5th Bus Cycle | | 6th Bus Cycle | | 7th Bus Cycle | |
|--|---------------------|--------------------|-------------------------------|--------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² |
| Erase Related | | | | | | | | | | | | | | |
| Block-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | BAx | 30H | | |
| Chip-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H | | |
| Erase Suspend | XXXH | B0H | | | | | | | | | | | | |
| Erase Resume | XXXH | 30H | | | | | | | | | | | | |
| Security ID | | | | | | | | | | | | | | |
| SEC ID Entry ⁶ | 555H | AAH | 2AAH | 55H | 555H | 88H | | | | | | | | |
| SEC ID Read^{3,7} | WA _x | Data | | | | | | | | | | | | |
| SEC ID Exit | 555H | AAH | 2AAH | 55H | 555H | 90H | XXH | 00H | | | | | | |
| Product Identification | | | | | | | | | | | | | | |
| Software ID Entry ⁸ | 555H | AAH | 2AAH | 55H | 555H | 90H | | | | | | | | |
| Manufacturer ID^{3,9} | X00 | BFH | | | | | | | | | | | | |
| Device ID^{3,9} | X01 | Data | | | | | | | | | | | | |
| Read Block Protection Status³ | BAX02 ¹⁰ | Data ¹¹ | | | | | | | | | | | | |
| Read Irreversible Block Lock Status³ | 5FEH | Data ¹² | | | | | | | | | | | | |
| Read Global Lock Bit Status³ | 9FFH | Data ¹³ | | | | | | | | | | | | |
| Software ID Exit /CFI Exit ¹⁴ | XXH | F0H | | | | | | | | | | | | |
| Volatile Block Protection | | | | | | | | | | | | | | |
| Volatile Block Protection Mode Entry | 555H | AAH | 2AAH | 55H | 555H | E0H | | | | | | | | |
| Volatile Protection Bit (VPB) Set/ Clear | XXH | A0H | BA _x ¹⁵ | Data ¹⁶ | | | | | | | | | | |
| VPB Status Read³ | BA _x | Data ¹⁶ | | | | | | | | | | | | |
| Volatile Block Protection Mode Exit | XXH | 90H | XXH | 00H | | | | | | | | | | |
| Non-Volatile Block Protection | | | | | | | | | | | | | | |
| Non-Volatile Block Protection Mode Entry | 555H | AAH | 2AAH | 55H | 555H | C0H | | | | | | | | |
| Non-Volatile Protect Bit (NVPB) Program | XXH | A0H | BA _x ¹⁵ | 00H | | | | | | | | | | |



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Table 11: Software Command Sequence (Continued) (3 of 4)

| Command Sequence | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | | 4th Bus Cycle | | 5th Bus Cycle | | 6th Bus Cycle | | 7th Bus Cycle | |
|--|-------------------------------|--------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² |
| Non-Volatile Protect Bits (NVPB) Erase ¹⁷ | XXH | 80H | 00H | 30H | | | | | | | | | | |
| NVPB Status Read³ | BA _x ¹⁵ | Data ¹⁶ | | | | | | | | | | | | |
| Non-Volatile Block Protection Mode Exit | XXH | 90H | XXH | 00H | | | | | | | | | | |
| Global Lock of NVPBs | | | | | | | | | | | | | | |
| Global Lock of NVPBs Entry | 555H | AAH | 2AAH | 55H | 555H | 50H | | | | | | | | |
| Set Global Lock Bit | XXH | A0H | XXH | 00H | | | | | | | | | | |
| Global Lock Bit Status Read³ | XXXH | Data ¹³ | | | | | | | | | | | | |
| Global Lock of NVPBs Exit | XXH | 90H | XXH | 00H | | | | | | | | | | |
| Password Commands | | | | | | | | | | | | | | |
| Password Commands Mode Entry | 555H | AAH | 2AAH | 55H | 555H | 60H | | | | | | | | |
| Password Program ¹⁸ | XXH | A0H | PWA _x | PWD _x | | | | | | | | | | |
| Password Read³ | PWA _x | PWD _x | | | | | | | | | | | | |
| Submit Password ¹⁹ | 00H | 25H | 00H | 03H | 00H | PWD ₀ | 01H | PWD ₁ | 02H | PWD ₂ | 03H | PWD ₃ | 00H | 29H |
| Password Commands Mode Exit | XXH | 90H | XXH | 00H | | | | | | | | | | |
| Program and Settings Register (PSR) | | | | | | | | | | | | | | |
| PSR Entry | 555H | AAH | 2AAH | 55H | 555H | 40H | | | | | | | | |
| PSR Program | XXH | A0H | XXXH | Data | | | | | | | | | | |
| PSR Read³ | XXH | Data | | | | | | | | | | | | |
| PSR Exit | XXH | 90H | XXH | 00H | | | | | | | | | | |
| CFI | | | | | | | | | | | | | | |
| CFI Query Entry | 55H | 98H | | | | | | | | | | | | |
| Software ID Exit/CFI Exit ¹⁴ | XXH | F0H | | | | | | | | | | | | |



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Table 11: Software Command Sequence (Continued) (4 of 4)

| Command Sequence | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | | 4th Bus Cycle | | 5th Bus Cycle | | 6th Bus Cycle | | 7th Bus Cycle | |
|---------------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| | Addr ¹ | Data ² |
| Irreversible Block Lock | | | | | | | | | | | | | | |
| Irreversible Block Lock ²⁰ | 555H | AAH | 2AA H | 55H | 555H | 87H | XXH | 00H | | | | | | |

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- Address format A₁₀-A₀ (Hex). Addresses A₁₁- A₂₁ can be V_{IL} or V_{IH}, but no other value, for the SST38VF6401B/6402B/6403B/6404B command sequence.
- DQ₁₅-DQ₈ can be V_{IL} or V_{IH}, but no other value, for command sequence
- All read commands are in ***Bold Italics***.
- Total number of cycles in this command sequence depends on the number of words to be written to the buffer. Additional words are written by repeating Write Cycle 5. Address (WA_x) values for Write Cycle 6 and later must have the same A₂₁-A₄ values as WA_x in Write Cycle 5. WC = Word Count. The value of WC is the number of words to be written into the buffer, minus 1. Maximum WC value is 15 (i.e. F Hex)
- Erase-Suspend and Erase-Resume commands are also available in Bypass Mode.
- Once in SEC ID mode, the Word-Program, Write-Buffer Programming, and Bypass Word-Program features can be used to program the SEC ID area.
- Lock-out Status is read with A₇-A₀ = FFH. Unlocked: DQ₃ = 1 / Locked: DQ₃ = 0. Lock status can also be checked by reading Bit '0' in the PSR.
- The device does not remain in Software Product ID Mode if powered down.
- With A_{MS}-A₁ = 0; SST Manufacturer ID = 00BFH, is read with A₀ = 0, SST38VF6401B/6402B/6403B/6404B Device IDs are read with the results shown in Table 6 on page 16.
- BA_{X02}: A_{MS}-A₁₅ = Block Address; A₁₄-A₈ = xxxxxx; A₇-A₀ = 02
- Data = 00H unprotected block; Data = 01H protected block.
- DQ₀ = 0 means the Irreversible Block Lock command has been previously used. DQ₀ = 1 means the Irreversible Block Lock command has not yet been used.
- DQ₀ = 0 means that the Global Lock Bit is locked. DQ₀ = 1 means that the Global Lock Bit is unlocked.
- Both Software ID Exit operations are equivalent.
- For Non-Uniform Boot Block devices (i.e. 8 KWord size), in the boot area, use BA_x = Block Address.
- DQ₀ = 0 means protected; DQ₀ = 1 means unprotected
- Erases all NVPBs to '1' (unprotected)
- Entire two-bus cycle sequence must be entered for each portion of the password.
- Entire password sequence required for validation. The word order doesn't matter as long as the Address and Data pair match.
- Global Lock Bit must be '1' before executing this command.

Note: Table 11 uses the following abbreviations:

X = Don't care (V_{IL} or V_{IH}, but no other value).

BA_x = Block Address; uses A_{MS}-A₁₅ address lines

WA = Word Address

WC = Word Count

PWA_x = Password Address; PWA_x = PWA₀, PWA₁, PWA₂ or PWA₃; A₁ and A₀ are used to select each 16-bit portion of the password

PWD_x = Password Data; PWD_x = PSWD₀, PWD₁, PWD₂, or PWD₃

A_{MS} = Most significant Address

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Table 12:Protection Priority for Main Array

| NVPB ¹ | VPB ¹ | Protection State of Block |
|-------------------|------------------|---------------------------|
| protect | X | protected |
| X | protect | protected |
| unprotect | unprotect | unprotected |

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1. X = protect or unprotect

Table 13:CFI Query Identification String¹ for SST38VF6401B/6402B/6403B/6404B

| Address | Data | Description |
|---------|-------|--|
| 10H | 0051H | Query Unique ASCII string "QRY" |
| 11H | 0052H | |
| 12H | 0059H | |
| 13H | 0002H | Primary OEM command set |
| 14H | 0000H | |
| 15H | 0040H | Address for Primary Extended Table |
| 16H | 0000H | |
| 17H | 0000H | Alternate OEM command set (00H = none exists) |
| 18H | 0000H | |
| 19H | 0000H | Address for Alternate OEM Extended Table (00H = none exists) |
| 1AH | 0000H | |

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1. Refer to CFI publication 100 for more details.



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Table 14: System Interface Information for SST38VF6401B/6402B/6403B/6404B

| Address | Data | Description |
|---------|-------|--|
| 1BH | 0027H | V _{DD} Min (Program/Erase) DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts |
| 1CH | 0036H | V _{DD} Max (Program/Erase) DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts |
| 1DH | 0000H | V _{PP} min. (00H = no V _{PP} pin) |
| 1EH | 0000H | V _{PP} max. (00H = no V _{PP} pin) |
| 1FH | 0003H | Typical time out for Word-Program 2 ^N μs (2 ³ = 8 μs) |
| 20H | 0003H | Typical time out for min. size buffer program 2 ^N μs (00H = not supported) |
| 21H | 0004H | Typical time out for individual Block-Erase 2 ^N ms (2 ⁴ = 16 ms) |
| 22H | 0005H | Typical time out for Chip-Erase 2 ^N ms (2 ⁵ = 32 ms) |
| 23H | 0001H | Maximum time out for Word-Program 2 ^N times typical (2 ¹ x 2 ³ = 16 μs) |
| 24H | 0003H | Maximum time out for buffer program 2 ^N times typical |
| 25H | 0001H | Maximum time out for individual Block-Erase 2 ^N times typical (2 ¹ x 2 ⁴ = 32 ms) |
| 26H | 0001H | Maximum time out for Chip-Erase 2 ^N times typical (2 ¹ x 2 ⁵ = 64 ms) |

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Table 15: Device Geometry Information for SST38VF6401B/6402B/6403B/6404B

| Address | Data | Description |
|---------|-------|---|
| 27H | 0017H | Device size = 2 ^N Bytes (17H = 23; 2 ²³ = 8 MByte) |
| 28H | 0001H | Flash Device Interface description; 0001H = x16-only asynchronous interface |
| 29H | 0000H | |
| 2AH | 0005H | Maximum number of bytes in multi-byte write = 2 ^N (00H = not supported) |
| 2BH | 0000H | |
| 2CH | 000xH | Number of Erase Block regions in the device (01H = uniform boot device, 02H = non-uniform boot device). |
| 2DH | 00xxH | Erase Block Region 1 Information 007FH, 0000H, 0000H, 0001H, for SST38VF6401B/6402B 0007H, 0000H, 0020H, 0000H for SST38VF6403B/6404B |
| 2EH | 000xH | |
| 2FH | 00x0H | |
| 30H | 000xH | |
| 31H | | Erase Block Region 2 Information 0000H, 0000H, 0000H, 0000H, for SST38VF6401B/6402B 007EH, 0000H, 0000H, 0001H for SST38VF6403B/6404B |
| 32H | | |
| 33H | | |
| 34H | | |

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Table 16: Primary Vendor-Specific Extended Information for SST38VF6401B/6402B/6403B/6404B

| Address | Data | Description |
|---------|-------|---|
| 40H | 0050H | Query-unique ASCII string "PRI" |
| 41H | 0052H | |
| 42H | 0049H | |
| 43H | FFFFH | Reserved |
| 44H | FFFFH | Reserved |
| 45H | FFFFH | Reserved |
| 46H | 0002H | Erase Suspend 0 = Not supported 1 = Only read during Erase Suspend, 2 = Read and Program during Erase Suspend. |
| 47H | 0001H | Individual Block Protection 0 = Not supported 1 = Supported |
| 48H | FFFFH | Reserved |
| 49H | 0008H | Protection 0008H = Advanced |
| 4AH | 0000H | Simultaneous Operation 00 = Not supported |
| 4BH | 0000H | Burst Mode 00 = Not supported |
| 4CH | 0002H | Page Mode 00 = Not supported 02 = 8 Word page. |
| 4DH | 0000H | Acceleration Supply Minimum 00 = Not supported |
| 4EH | 0000H | Acceleration Supply Maximum 00 = Not supported |
| 4FH | 00XXH | Top / Bottom Boot Block 02H = 8 KWord Bottom Boot 03H = 8 KWord Top Boot 04H = Uniform (32 KWord) Bottom Boot 05H = Uniform (32 KWord) Top Boot |
| 50H | 0000H | Program Suspend 00H = Not Supported 01H = Supported |

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

| | |
|--|--------------------------------|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| D. C. Voltage on Any Pin to Ground Potential | -0.5V to V _{DD} +0.5V |
| Transient Voltage (<20 ns) on Any Pin to Ground Potential | -2.0V to V _{DD} +2.0V |
| Voltage on A ₉ Pin to Ground Potential | -0.5V to 12.5V |
| Voltage on RST# Pin to Ground Potential | -0.5V to 12.5V |
| Voltage on WP# Pin to Ground Potential | -0.5V to 12.5V |
| Package Power Dissipation Capability (T _A = 25°C) | 1.0W |
| Surface Mount Solder Reflow Temperature | 260°C for 10 seconds |
| Output Short Circuit Current ¹ | 50 mA |

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 17:Operating Range

| Range | Ambient Temp | V _{DD} |
|------------|----------------|-----------------|
| Commercial | 0°C to +70°C | 2.7-3.6V |
| Industrial | -40°C to +85°C | 2.7-3.6V |

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Table 18:AC Conditions of Test¹

| Input Rise/Fall Time | Output Load |
|----------------------|------------------------|
| 5ns | C _L = 30 pF |

1. See Figures 21 and 22

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Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate faster than 1V per 100 ms (0V to 3V in less than 300 ms). If the V_{DD} ramp rate is slower than 1V per 100 ms, a hardware reset is required. The recommended V_{DD} power-up to RESET# high time should be greater than 100 μ s to ensure a proper reset. See Table 19 and Figure 4 for more information.

Table 19: Recommended System Power-up Timings

| Symbol | Parameter | Minimum | Units |
|------------------|-------------------------------------|---------|---------|
| $T_{PU-READ}^1$ | Power-up to Read Operation | 100 | μ s |
| $T_{PU-WRITE}^1$ | Power-up to Erase/Program Operation | 100 | μ s |

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter. T19.0 25002

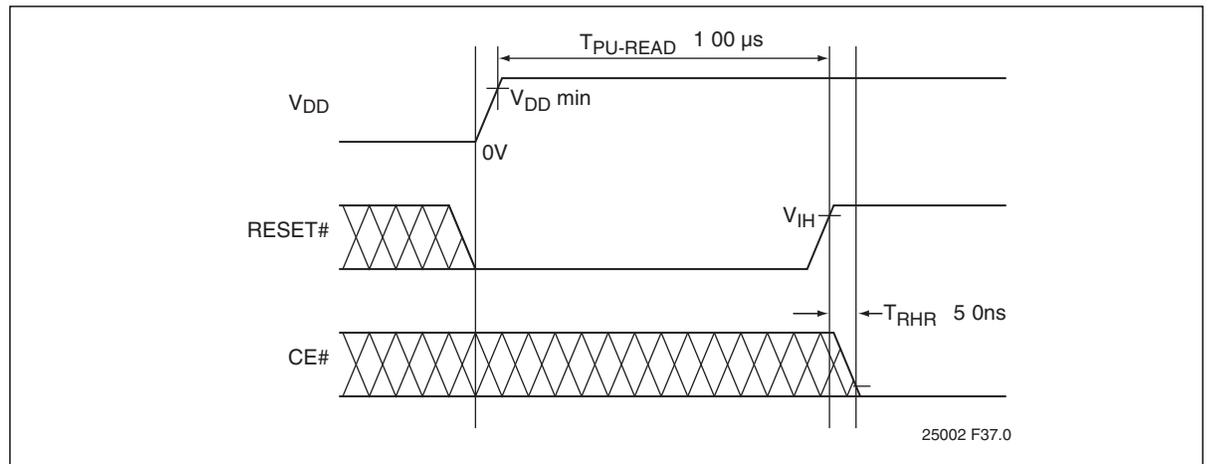


Figure 4: Power-Up Diagram



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DC Characteristics

Table 20: DC Operating Characteristics $V_{DD} = 2.7\text{-}3.6\text{V}^1$

| Symbol | Parameter | Limits | | | Test Conditions |
|------------------|---|----------------------|-----|-------|--|
| | | Min | Max | Units | |
| I _{DD} | Power Supply Current | | | | Address input= V_{ILT}/V_{IHT}^2 , $V_{DD}=V_{DD}$ Max |
| | Read ³ | | 30 | mA | CE#=V _{IL} , OE#=WE#=V _{IH} at f= 5 MHz |
| | Intra-Page Read @5 MHz | | 2.5 | mA | CE#=V _{IL} , OE#=WE#=V _{IH} |
| | Intra-Page Read @40 MHz | | 20 | mA | CE#=V _{IL} , OE#=WE#=V _{IH} |
| | Program and Erase | | 35 | mA | CE#=WE#=V _{IL} , OE#=V _{IH} |
| | Program-Write-Buffer-to-Flash | | 50 | mA | CE#=WE#=V _{IL} , OE#=V _{IH} |
| I _{SB} | Standby V _{DD} Current | | 30 | μA | CE#=V _{IHC} , $V_{DD}=V_{DD}$ Max |
| I _{ALP} | Auto Low Power | | 30 | μA | CE#=V _{ILC} , $V_{DD}=V_{DD}$ Max All inputs=V _{SS} or V _{DD} , WE#=V _{IHC} |
| I _{LI} | Input Leakage Current | | 1 | μA | V _{IN} =GND to V _{DD} , $V_{DD}=V_{DD}$ Max |
| I _{LIW} | Input Leakage Current on WP# pin and RST# | | 10 | μA | WP#=GND to V _{DD} or RST#=GND to V _{DD} |
| I _{LO} | Output Leakage Current | | 10 | μA | V _{OUT} =GND to V _{DD} , $V_{DD}=V_{DD}$ Max |
| V _{IL} | Input Low Voltage | | 0.8 | V | $V_{DD}=V_{DD}$ Min |
| V _{ILC} | Input Low Voltage (CMOS) | | 0.3 | V | $V_{DD}=V_{DD}$ Max |
| V _{IH} | Input High Voltage | 0.7V _{DD} | | V | $V_{DD}=V_{DD}$ Max |
| V _{IHC} | Input High Voltage (CMOS) | V _{DD} -0.3 | | V | $V_{DD}=V_{DD}$ Max |
| V _{OL} | Output Low Voltage | | 0.2 | V | I _{OL} =100 μA, $V_{DD}=V_{DD}$ Min |
| V _{OH} | Output High Voltage | V _{DD} -0.2 | | V | I _{OH} =-100 μA, $V_{DD}=V_{DD}$ Min |

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1. Typical conditions for the Active Current shown on the front page of the data sheet are average values at 25°C (room temperature), and $V_{DD} = 3\text{V}$. Not 100% tested.
2. See Figure 26
3. The I_{DD} current listed is typically less than 2mA/MHz, with OE# at V_{IH}. Typical V_{DD} is 3V.

Table 21: Capacitance ($T_A = 25^\circ\text{C}$, f=1 MHz, other pins open)

| Parameter | Description | Test Condition | Maximum |
|-------------------------------|---------------------|-----------------------|---------|
| C _{I/O} ¹ | I/O Pin Capacitance | V _{I/O} = 0V | 12 pF |
| C _{IN} ¹ | Input Capacitance | V _{IN} = 0V | 6 pF |

T21.0 25002

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 22: Reliability Characteristics

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|---------------------------------|----------------|-----------------------|--------|---------------------|
| N _{END} ^{1,2} | Endurance | 100,000 | Cycles | JEDEC Standard A117 |
| T _{DR} ¹ | Data Retention | 100 | Years | JEDEC Standard A103 |
| I _{LTH} ¹ | Latch Up | 100 + I _{DD} | mA | JEDEC Standard 78 |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. N_{END} endurance rating is qualified as 100,000 cycles minimum per block.



AC Characteristics

Table 23: Read Cycle Timing Parameters $V_{DD} = 2.7-3.6V$

| Symbol | Parameter | Min | Max | Units |
|-----------------|---|-----|-----|---------|
| T_{RC} | Read Cycle Time | 70 | | ns |
| T_{CE} | Chip Enable Access Time | | 70 | ns |
| T_{AA} | Address Access Time | | 70 | ns |
| T_{PACC} | Page Access Time | | 25 | ns |
| T_{OE} | Output Enable Access Time | | 25 | ns |
| T_{CLZ}^1 | CE# Low to Active Output | 0 | | ns |
| T_{OLZ}^1 | OE# Low to Active Output | 0 | | ns |
| T_{CHZ}^1 | CE# High to High-Z Output | | 20 | ns |
| T_{OHZ}^1 | OE# High to High-Z Output | | 20 | ns |
| T_{OH}^1 | Output Hold from Address Change | 0 | | ns |
| T_{RP}^1 | RST# Pulse Width | 500 | | ns |
| T_{RHR}^1 | RST# High before Read | 50 | | ns |
| $T_{RYE}^{1,2}$ | RST# Pin Low to Read Mode | | 20 | μs |
| T_{RY}^1 | RST# Pin Low to Read Mode – not during Program or Erase algorithms. | | 500 | ns |
| T_{RPD}^1 | RST# Input Low to Standby mode | 20 | | μs |
| T_{RB}^1 | RY / BY# Output high to CE# / OE# pin Low | 0 | | ns |
| T_{PWD} | Delay for each password check | 1 | | μs |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Block-Erase and Program operations.
This parameter does not apply to Chip-Erase operations.



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Table 24: Program/Erase Cycle Timing Parameters

| Symbol | Parameter | Min | Max | Units |
|--------------------------------|---|-----|-----|-------|
| T _{BP} | Word-Program Time | | 10 | μs |
| T _{WBP} ¹ | Program Buffer-to-Flash Time | | 40 | μs |
| T _{AS} | Address Setup Time | 0 | | ns |
| T _{AH} | Address Hold Time | 30 | | ns |
| T _{CS} | WE# and CE# Setup Time | 0 | | ns |
| T _{CH} | WE# and CE# Hold Time | 0 | | ns |
| T _{OES} | OE# High Setup Time | 0 | | ns |
| T _{OEH} | OE# High Hold Time | 10 | | ns |
| T _{CP} | CE# Pulse Width | 40 | | ns |
| T _{WP} | WE# Pulse Width | 40 | | ns |
| T _{WPH} ² | WE# Pulse Width High | 30 | | ns |
| T _{CPH} ² | CE# Pulse Width High | 30 | | ns |
| T _{DS} | Data Setup Time | 30 | | ns |
| T _{CEPH} | CE# Pulse Width High During Toggle Bit Polling | 20 | | ns |
| T _{OEPH} | OE# Pulse Width High During Toggle bit Polling | 20 | | ns |
| T _{DH} ² | Data Hold Time | 0 | | ns |
| T _{IDA} ² | Software ID, Volatile Protect, Non-Volatile Protect, Global Lock Bit, Password mode, Lock Bit, Bypass Entry, and Exit Times | | 150 | ns |
| T _{BE} | Block-Erase | | 25 | ms |
| T _{SCE} | Chip-Erase | | 50 | ms |
| T _{BUSY} ² | CE# High or WE# High to RY / BY# Low | 90 | | ns |
| T _{ETO} | Erase Time-out | | 50 | ns |

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1. Effective programming time is 2.5 μs per word if 16-words are programmed during this operation.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



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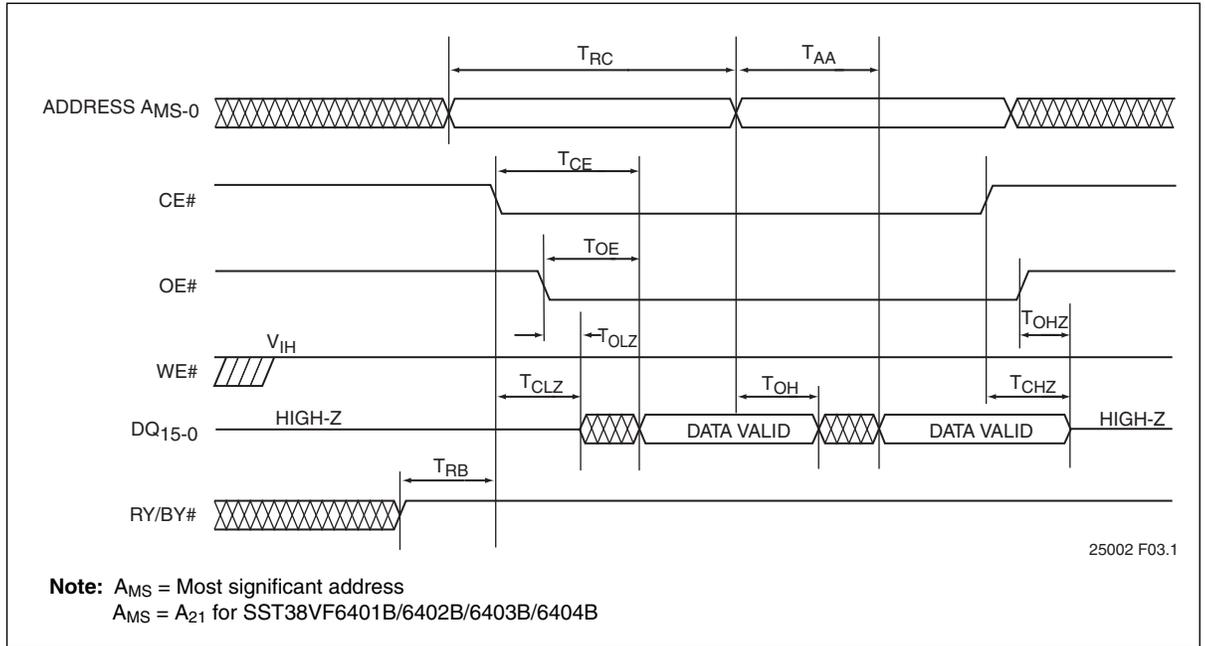


Figure 5: Read Cycle Timing Diagram

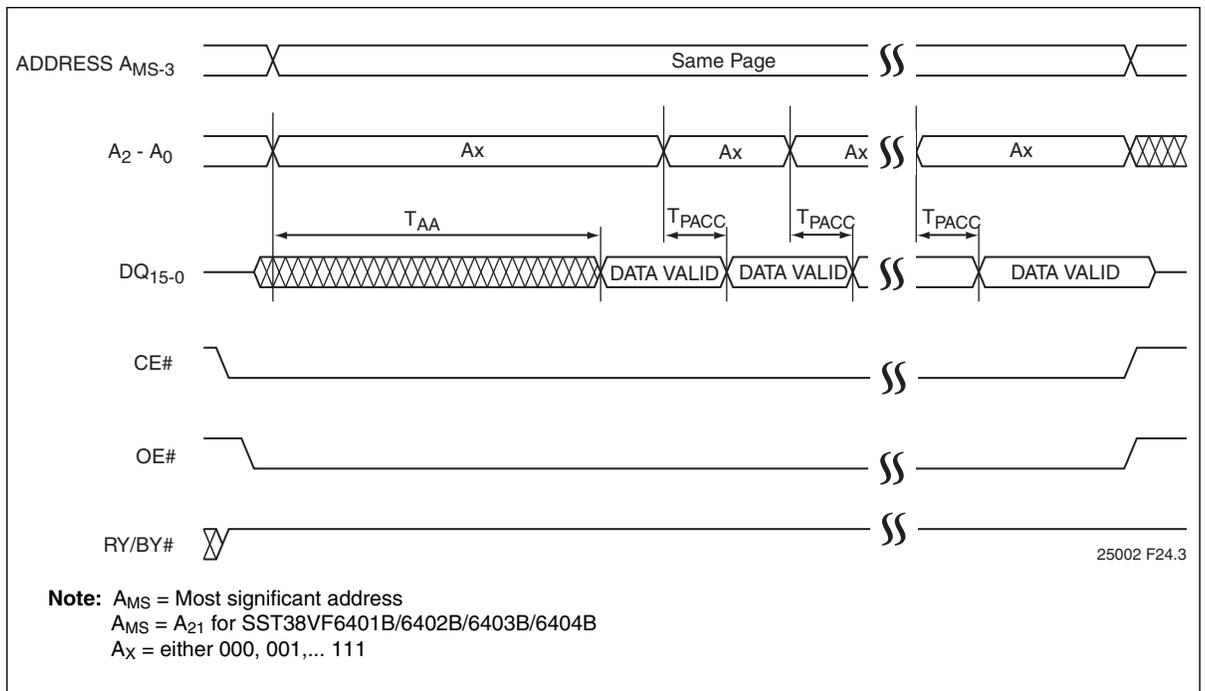


Figure 6: Page Read Timing Diagram



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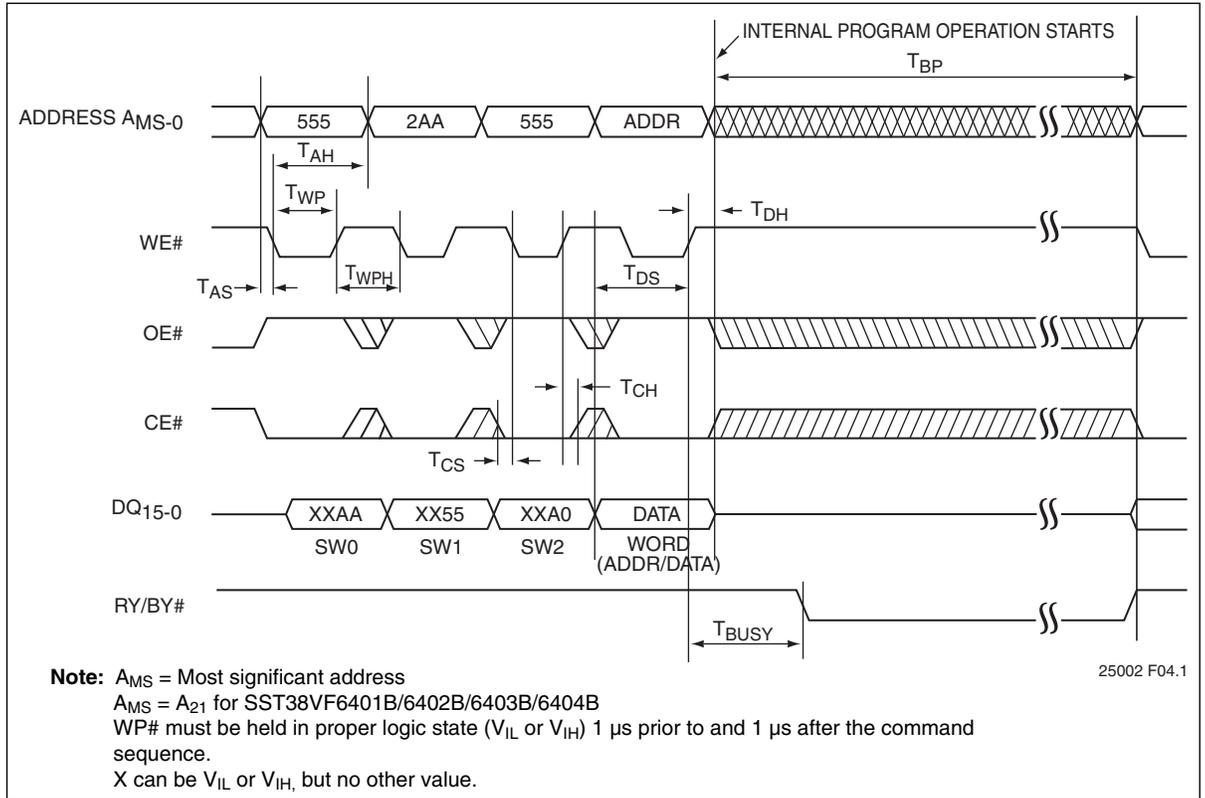


Figure 7: WE# Controlled Program Cycle Timing Diagram



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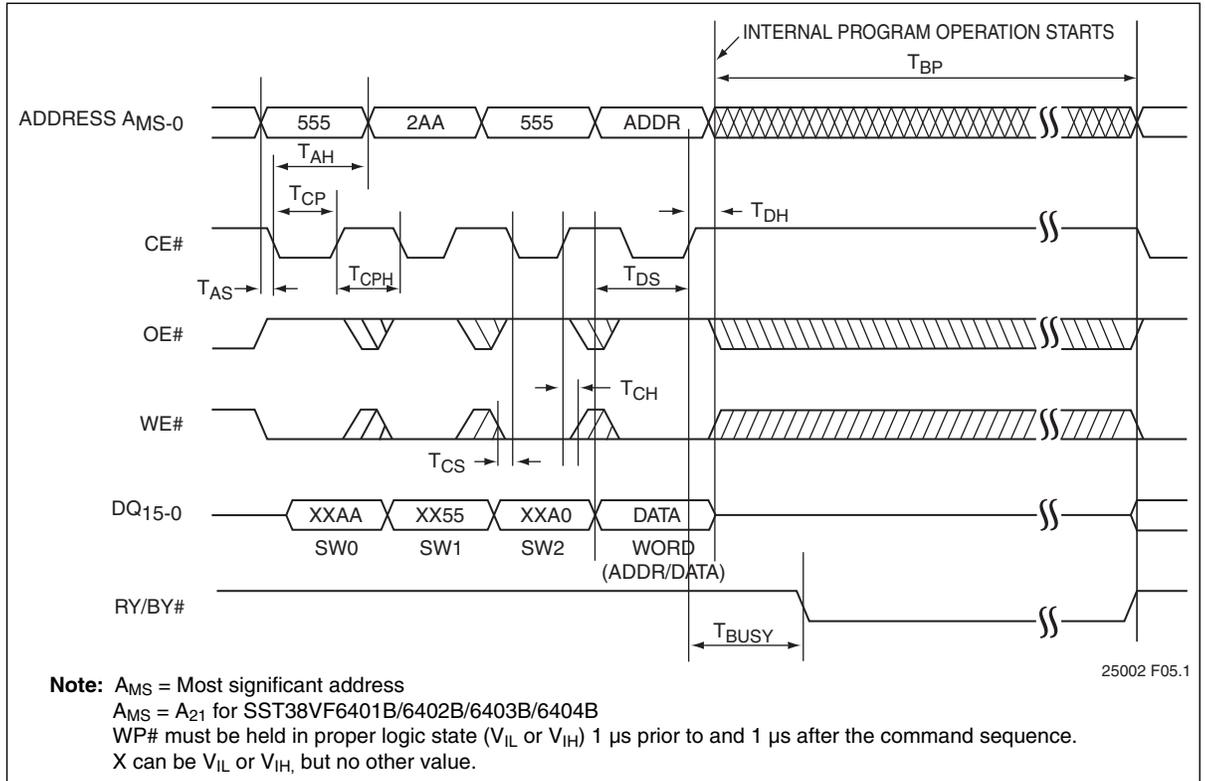


Figure 8: CE# Controlled Program Cycle Timing Diagram



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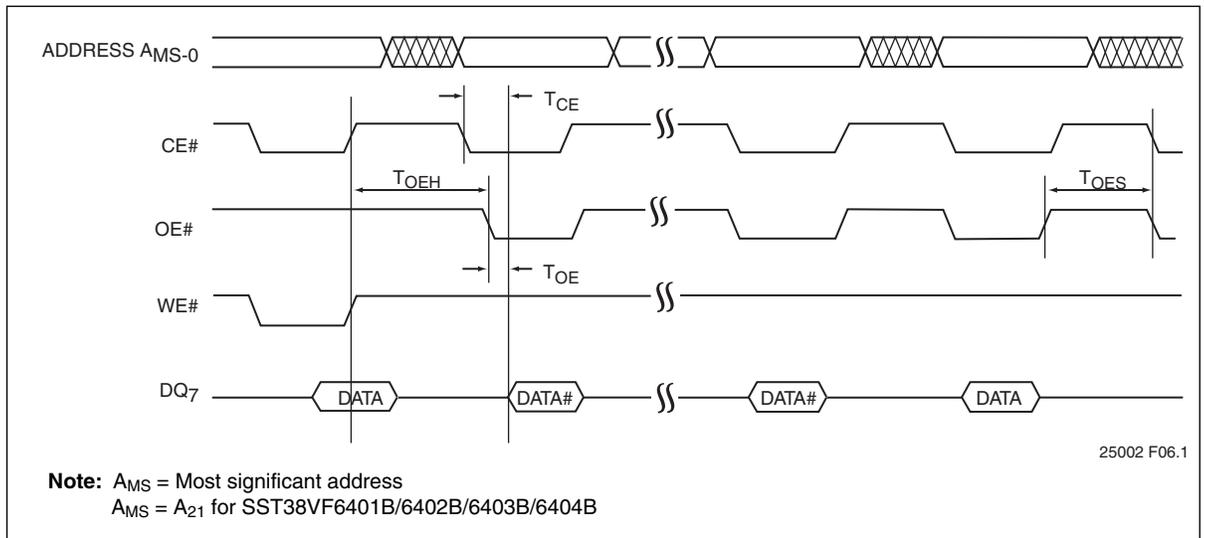


Figure 11: Data# Polling Timing Diagram

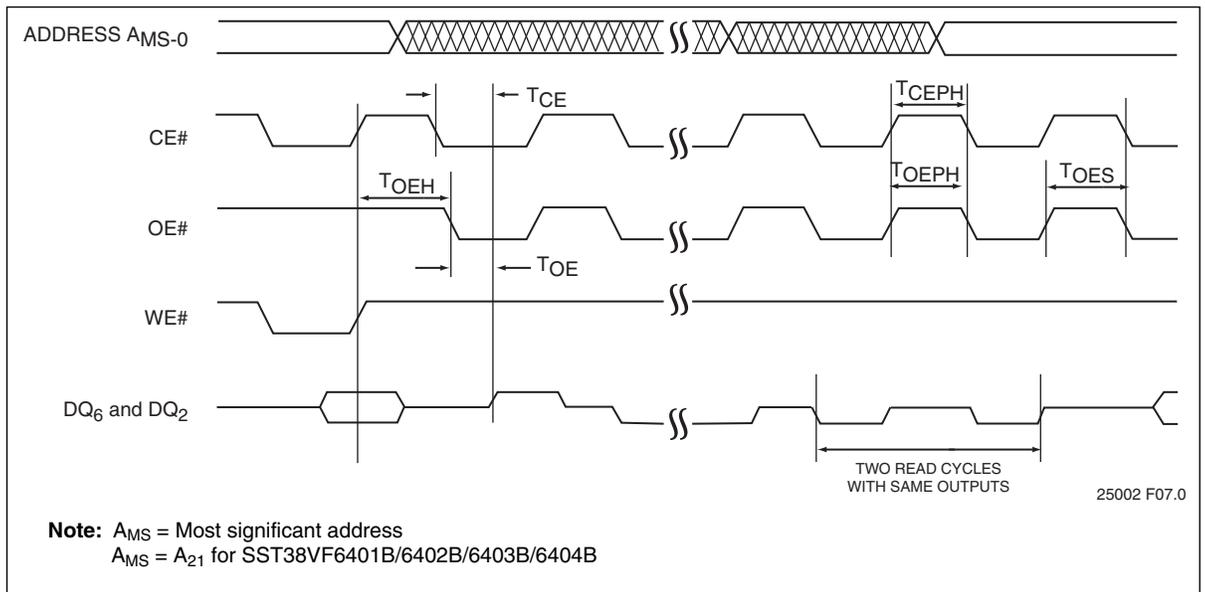


Figure 12: Toggle Bits Timing Diagram



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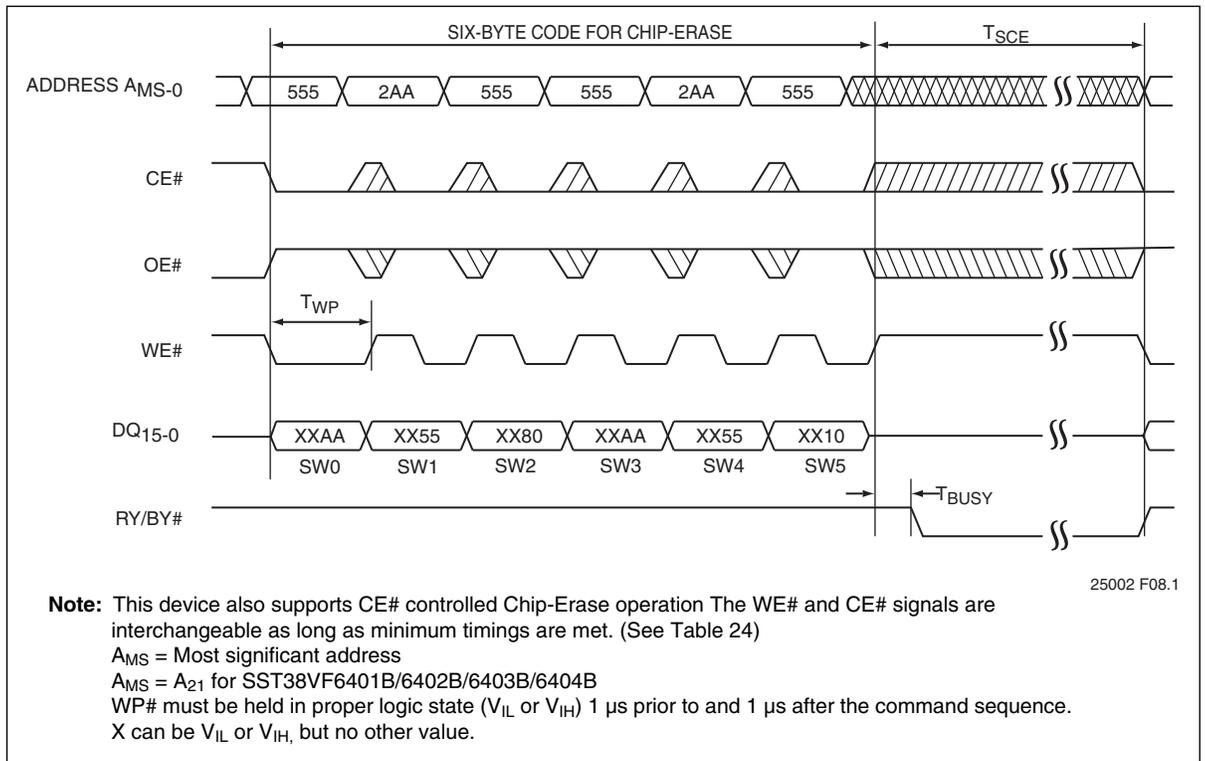


Figure 13: WE# Controlled Chip-Erase Timing Diagram



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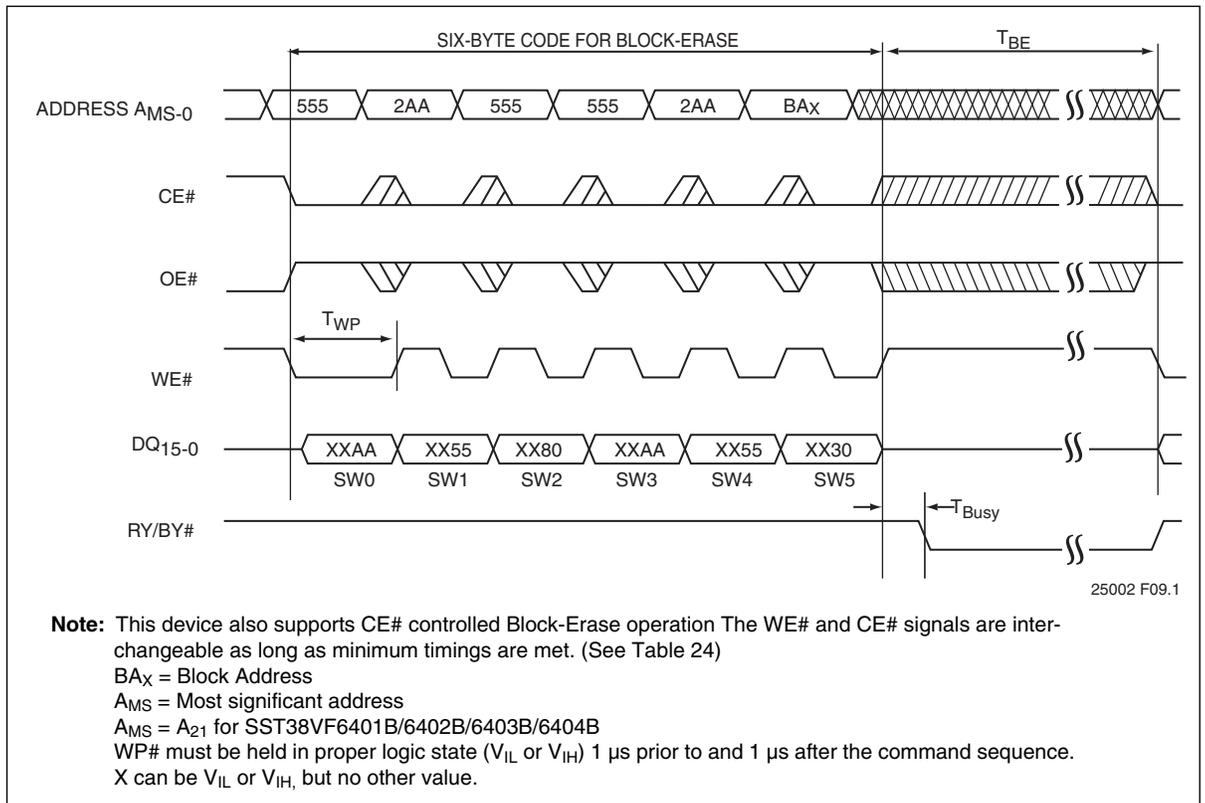


Figure 14: WE# Controlled Block-Erase Timing Diagram



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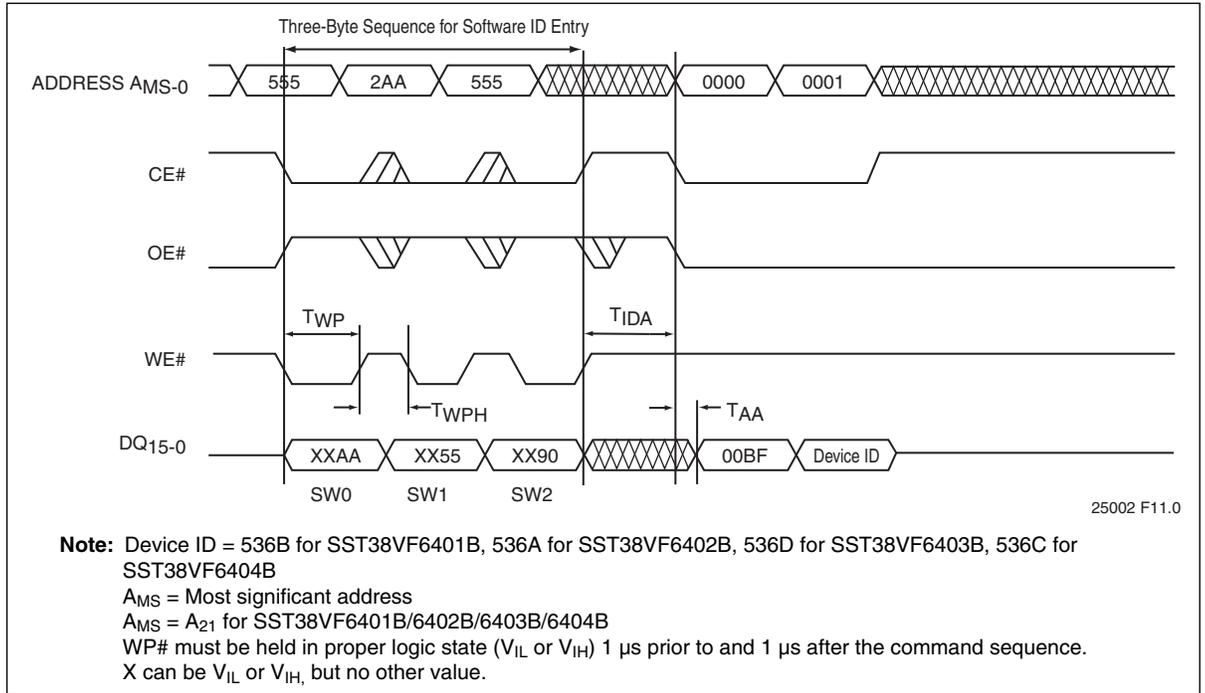


Figure 15: Software ID Entry and Read

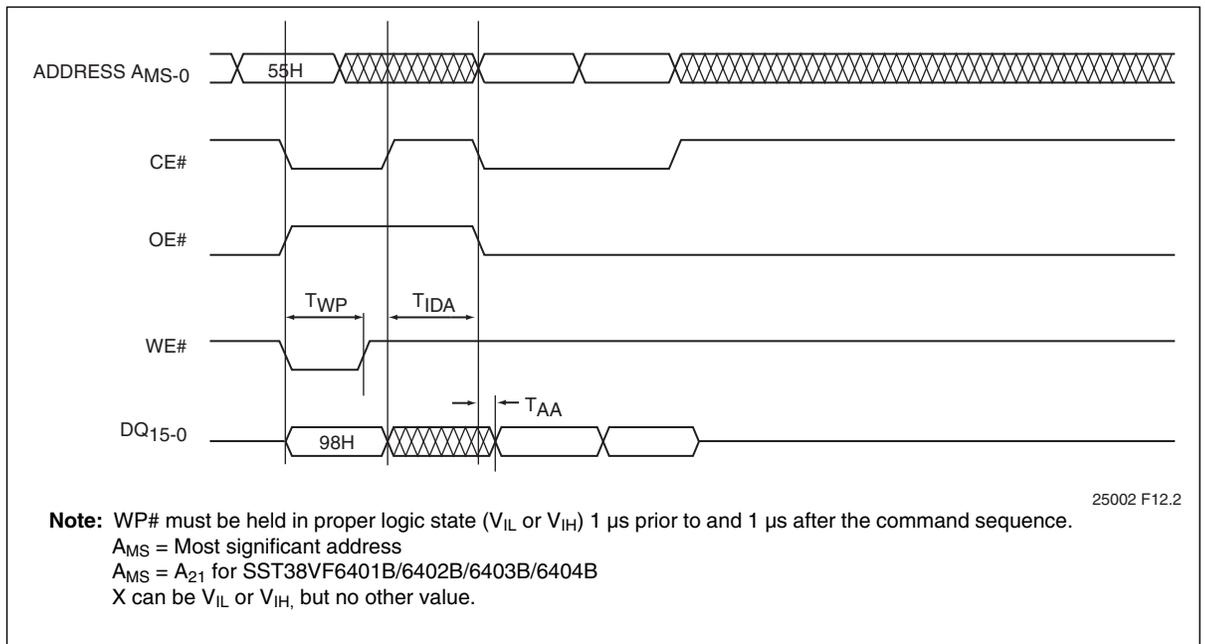


Figure 16: CFI Query Entry and Read

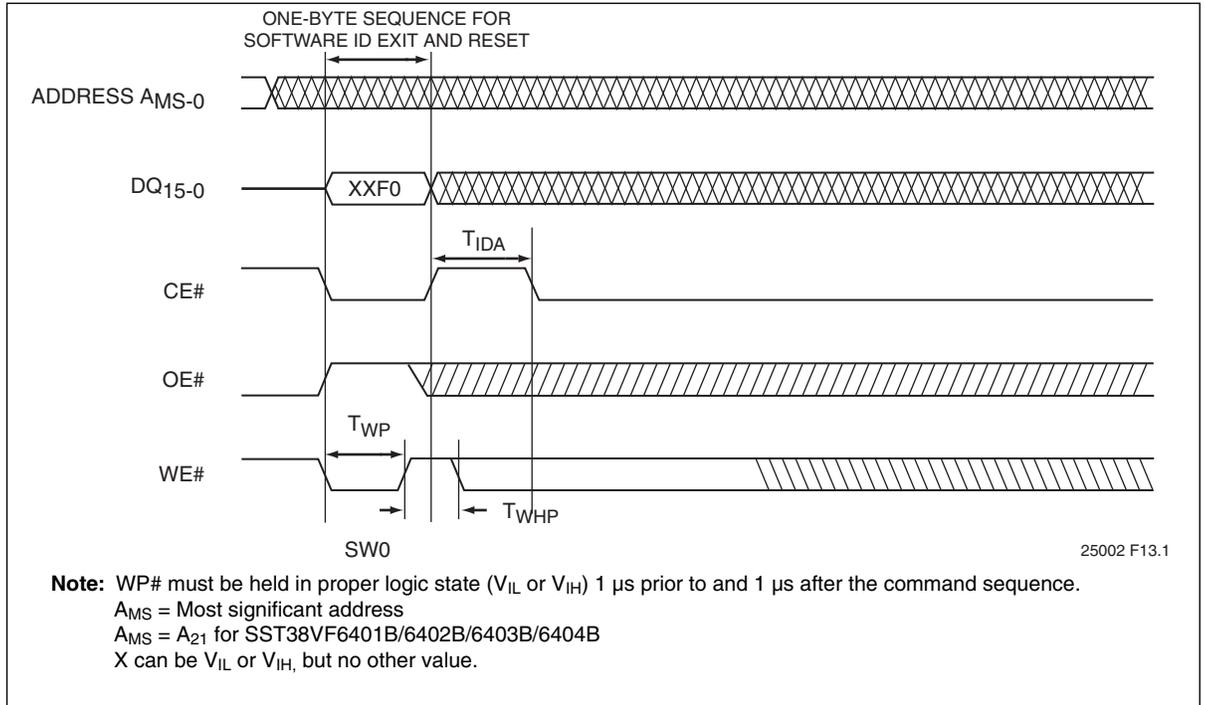


Figure 17:Software ID Exit/CFI Exit

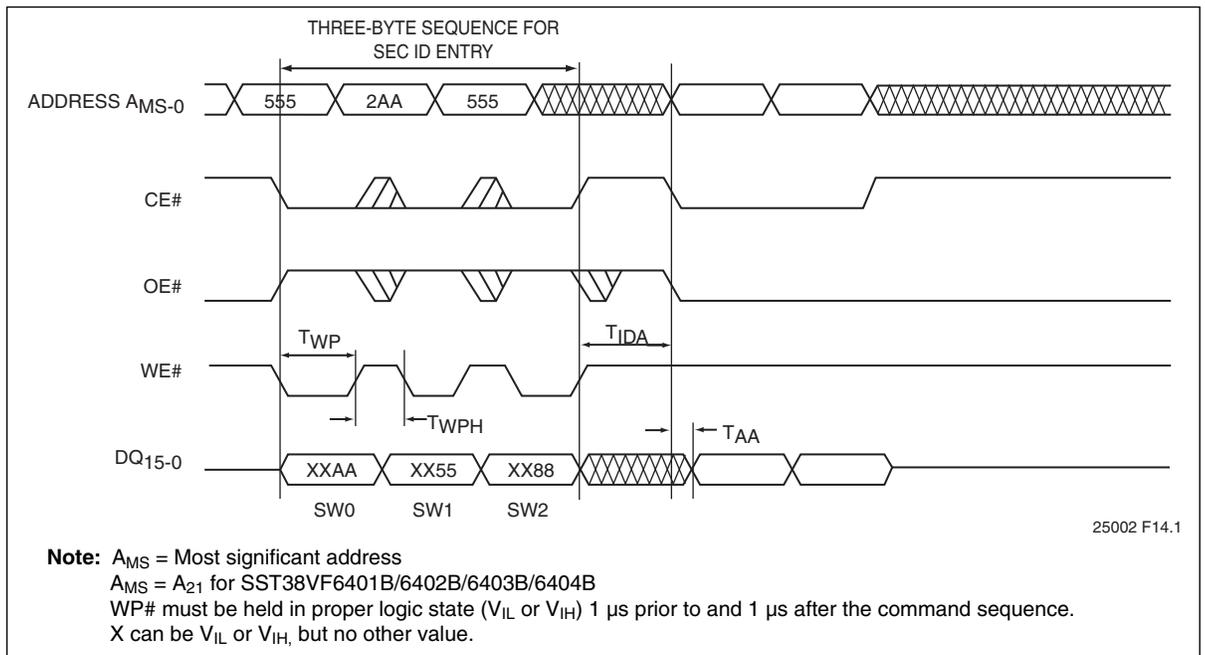


Figure 18:Sec ID Entry



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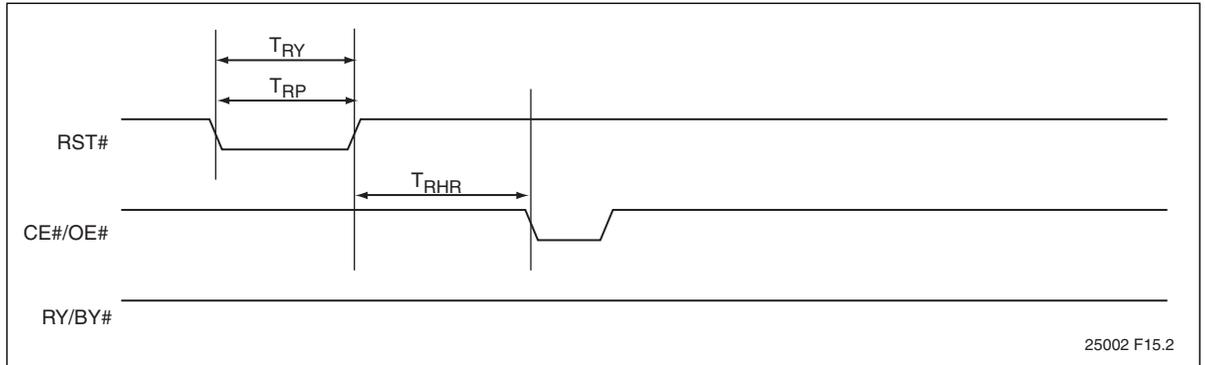


Figure 19:RST# Timing Diagram (When no internal operation is in progress)

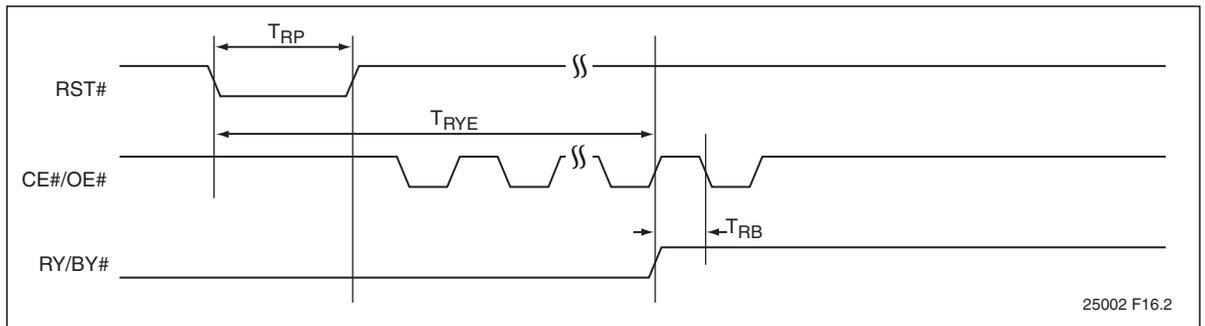


Figure 20:RST# Timing Diagram (During Program or Erase operation)

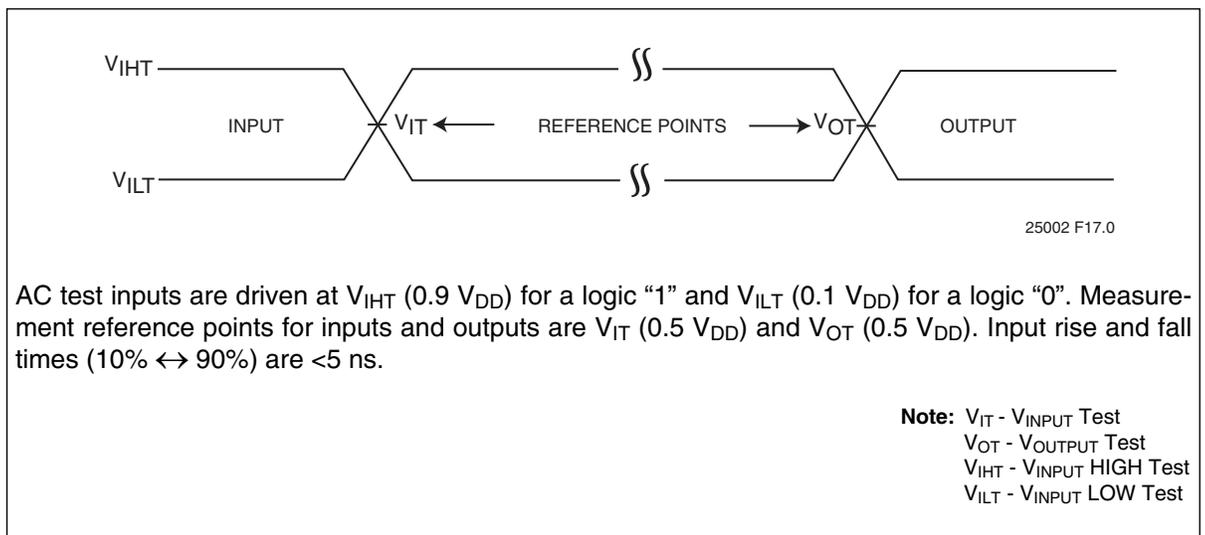


Figure 21:AC Input/Output Reference Waveforms



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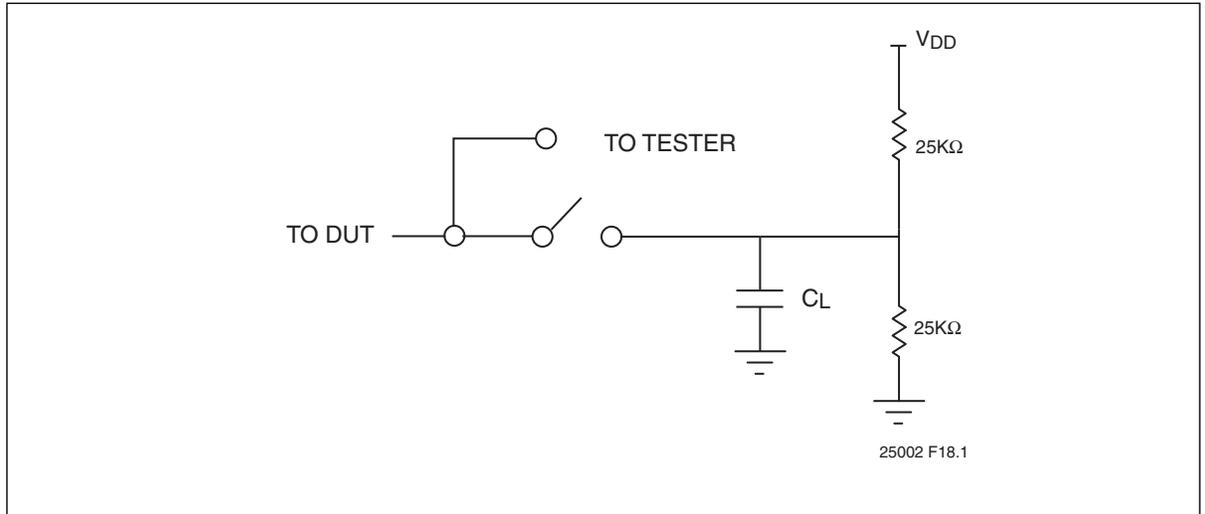


Figure 22:A Test Load Example



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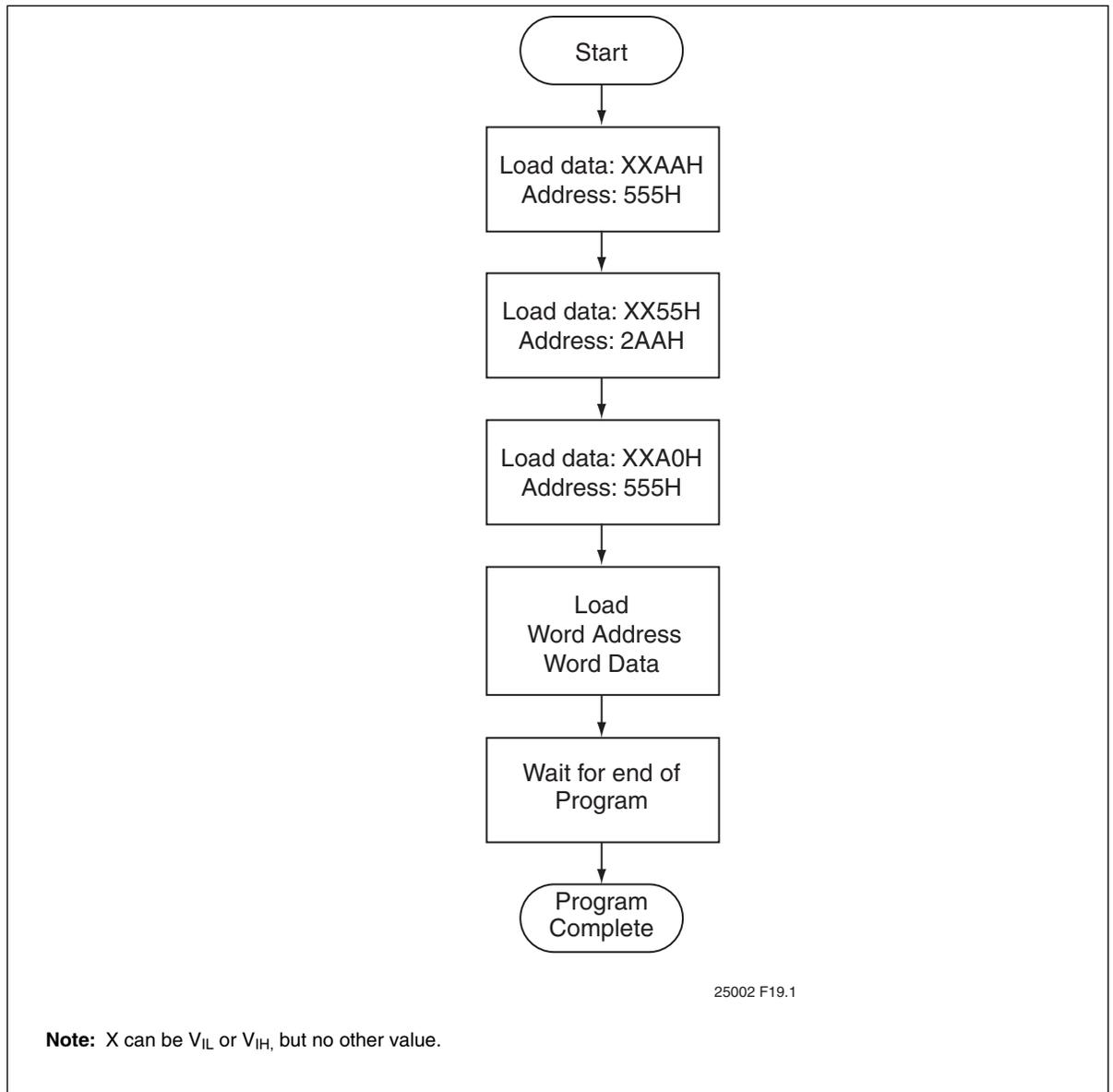


Figure 23: Word-Program Algorithm



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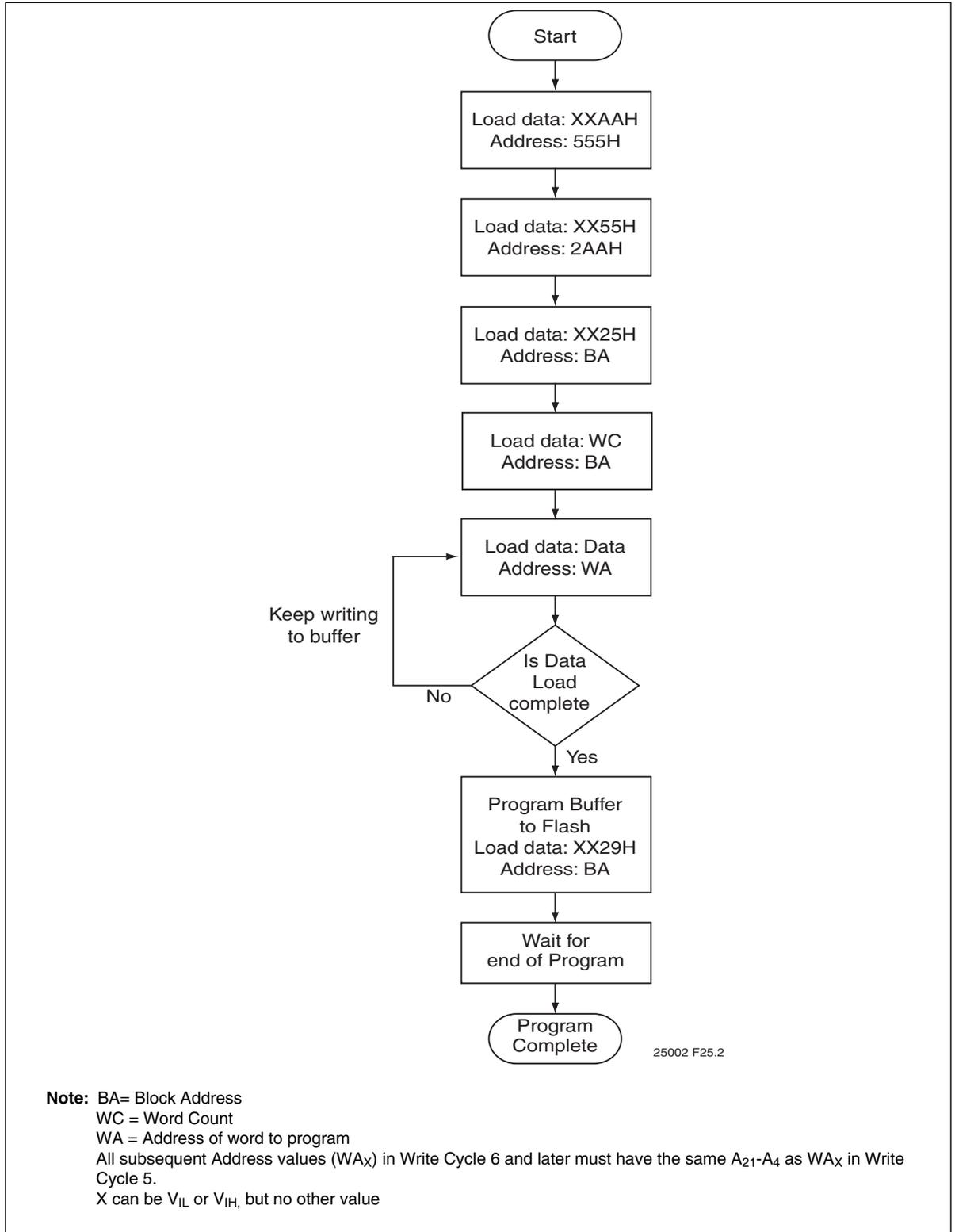


Figure 24:Write-Buffer Programming

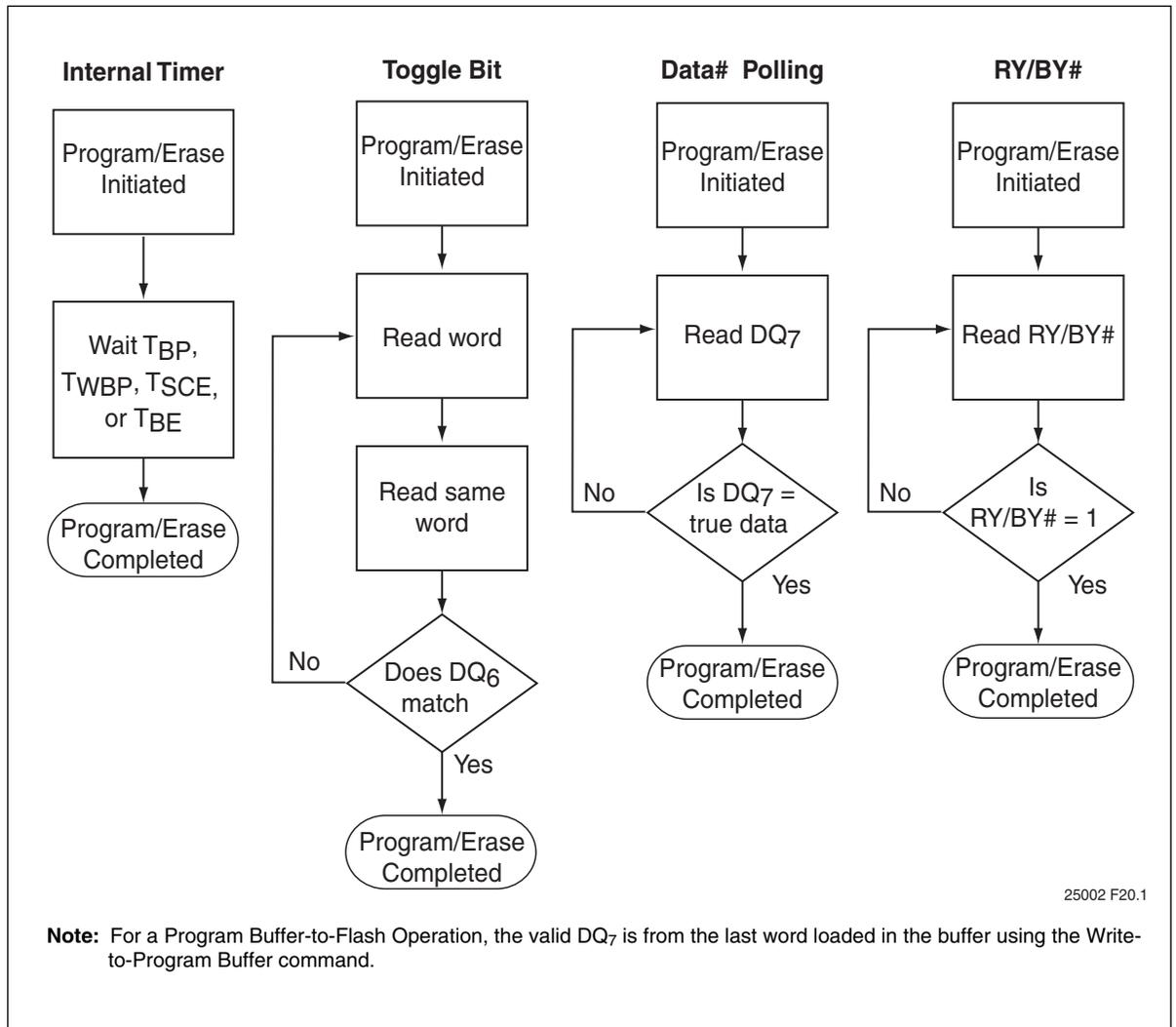


Figure 25:Wait Options



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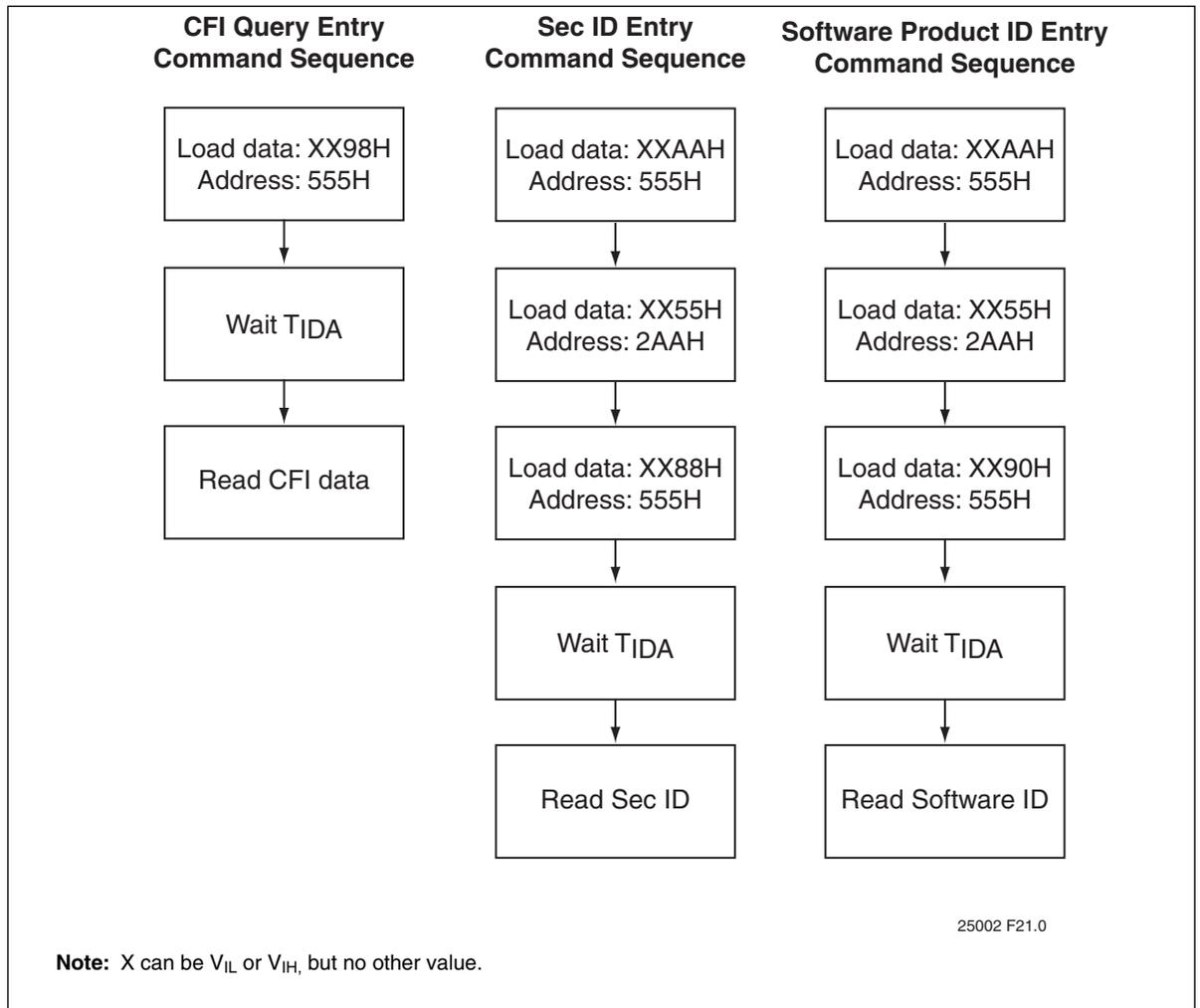


Figure 26:CFI/SEC ID/Software ID Entry Command Flowcharts



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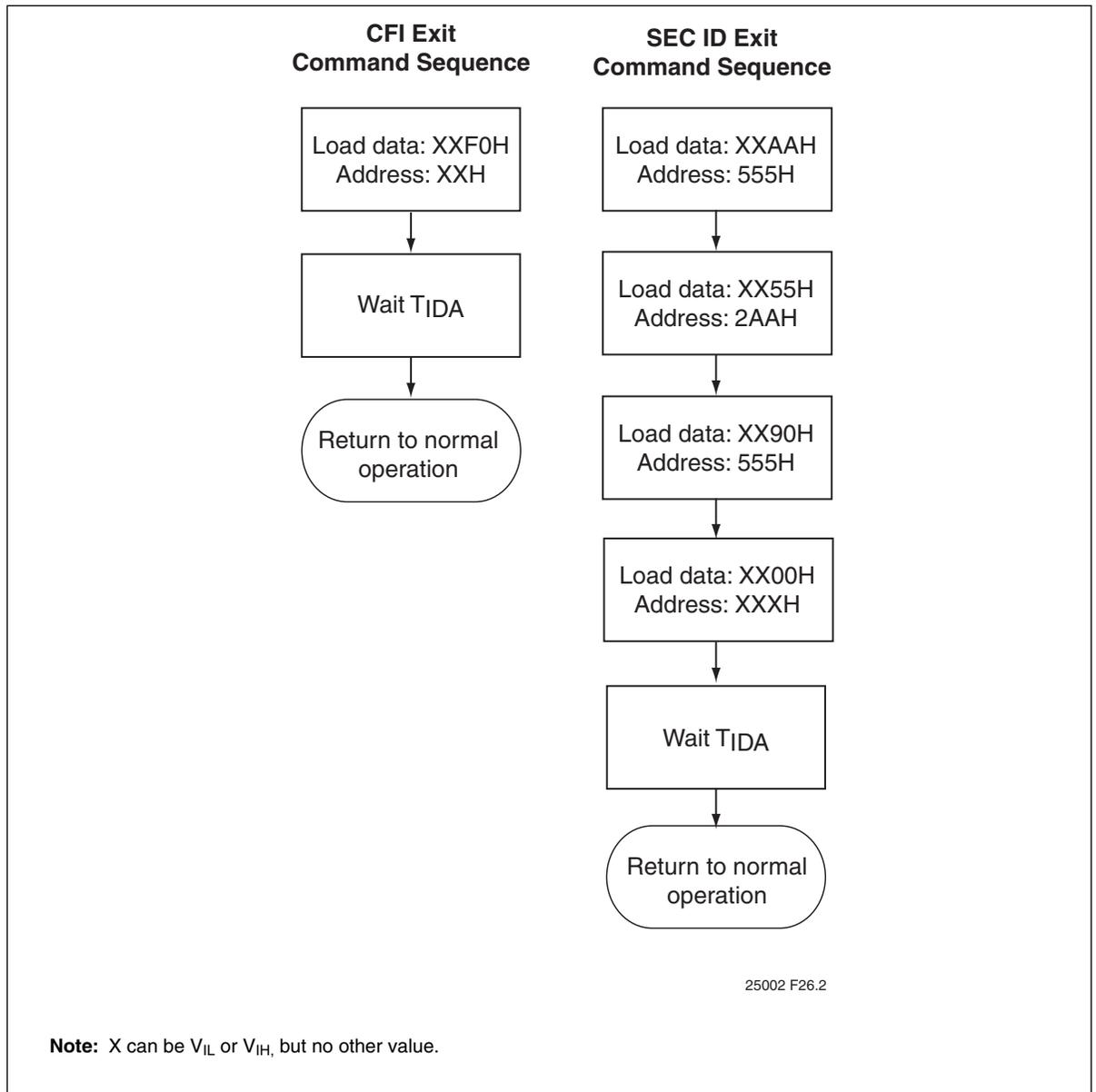


Figure 27: Software ID/CFI/SEC ID Exit Command Flowcharts



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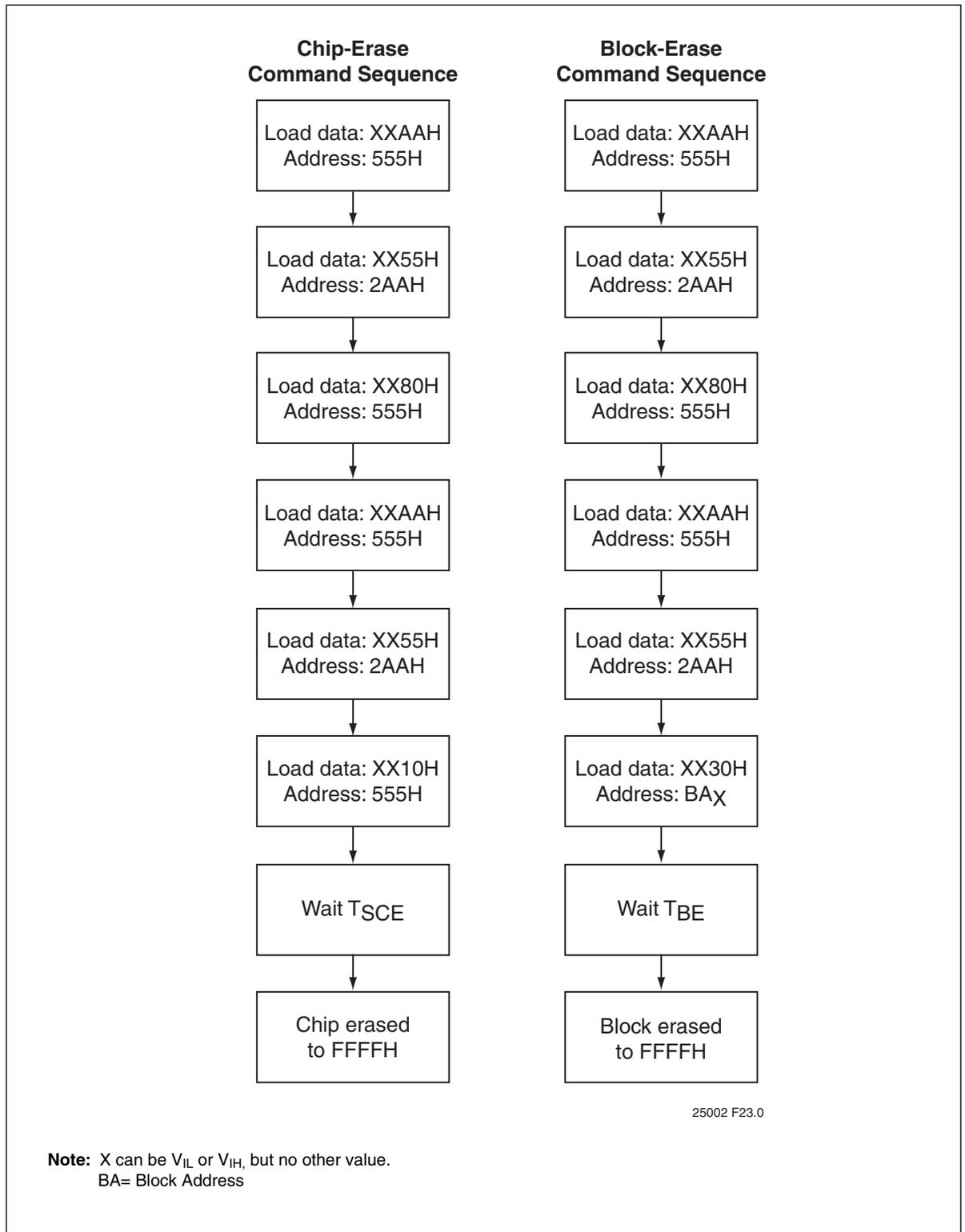


Figure 28: Erase Command Sequence

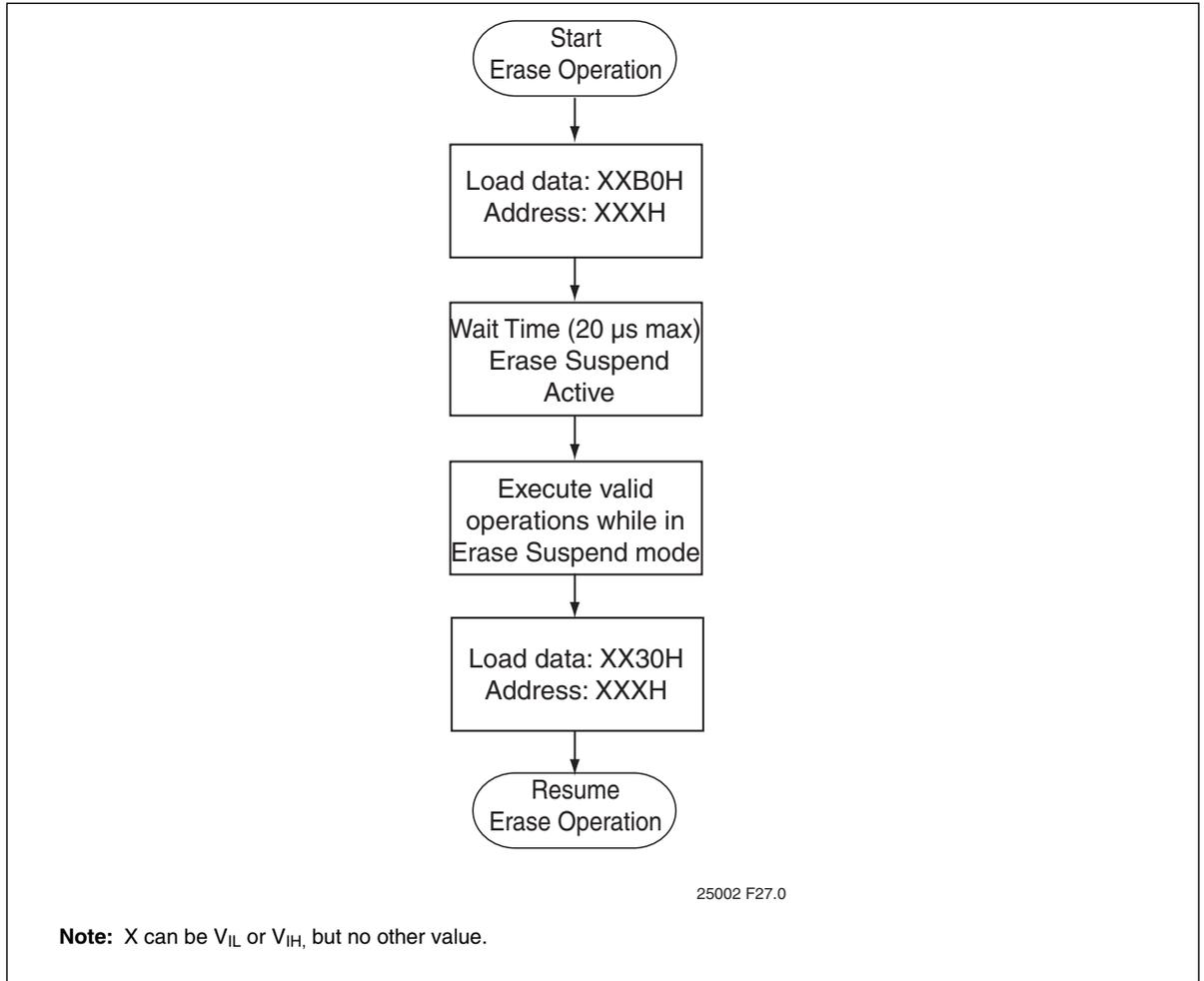


Figure 29:Erase Suspend/Resume



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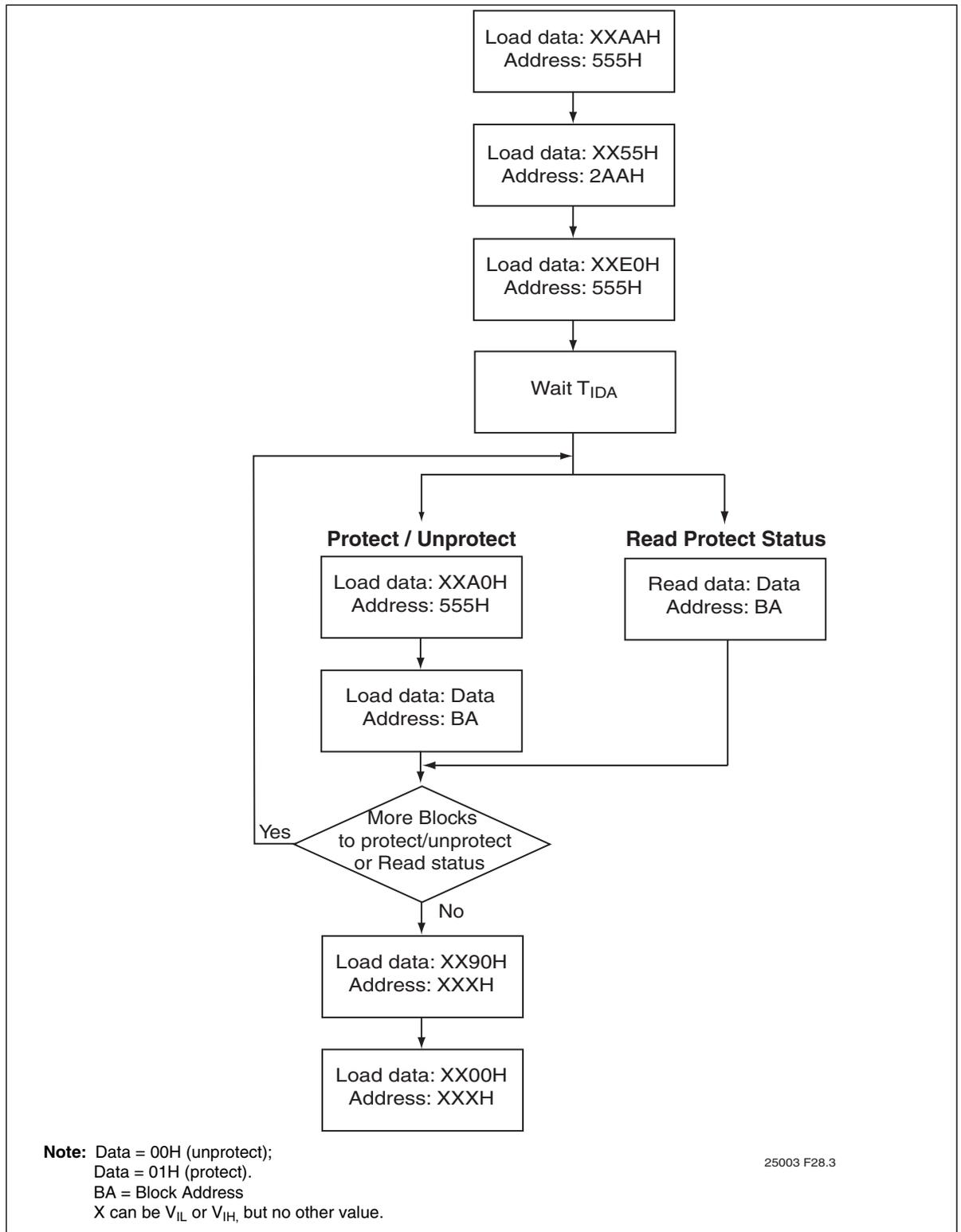


Figure 30: Volatile Block Protection



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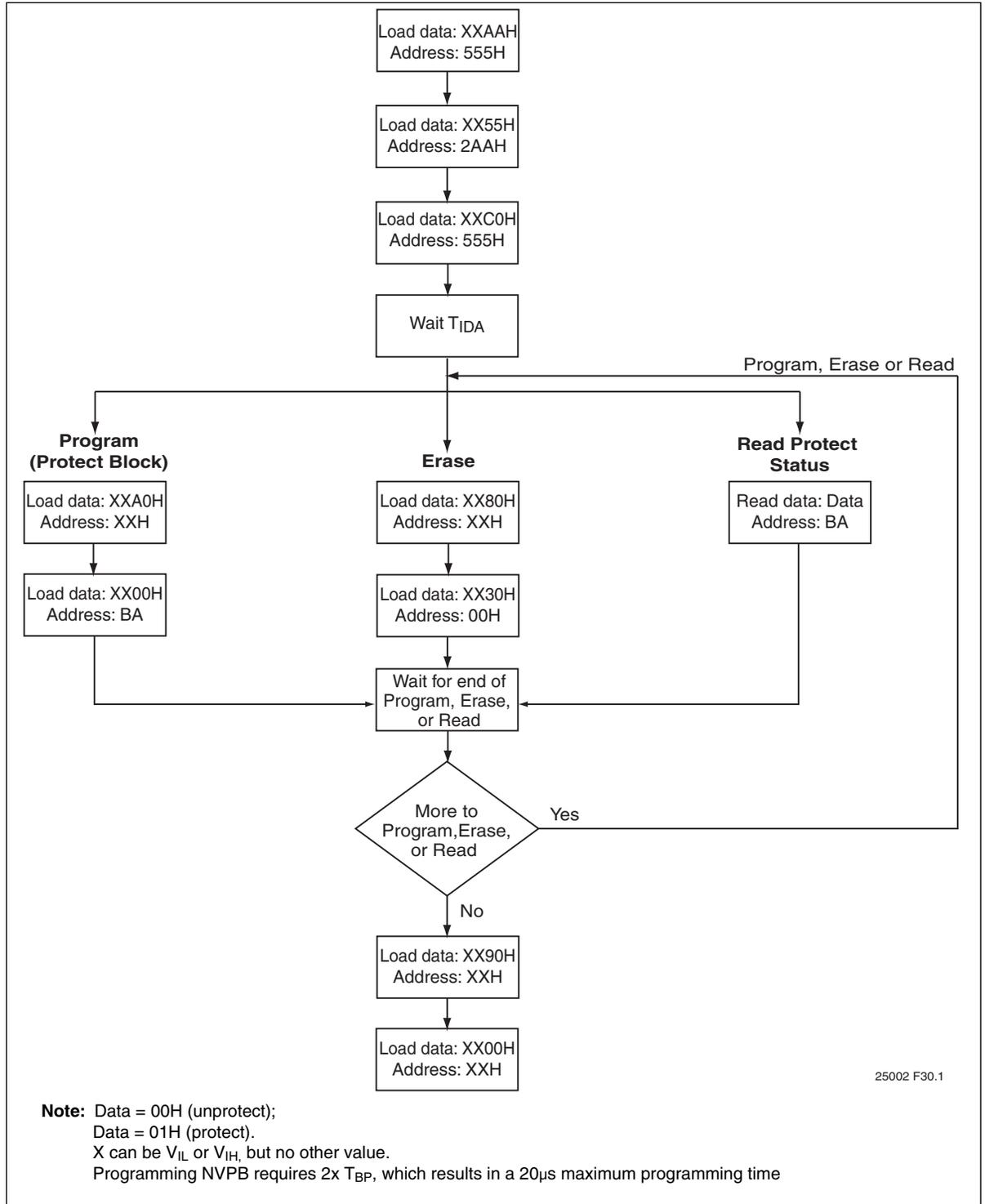


Figure 31: Non-Volatile Block Protect Mode



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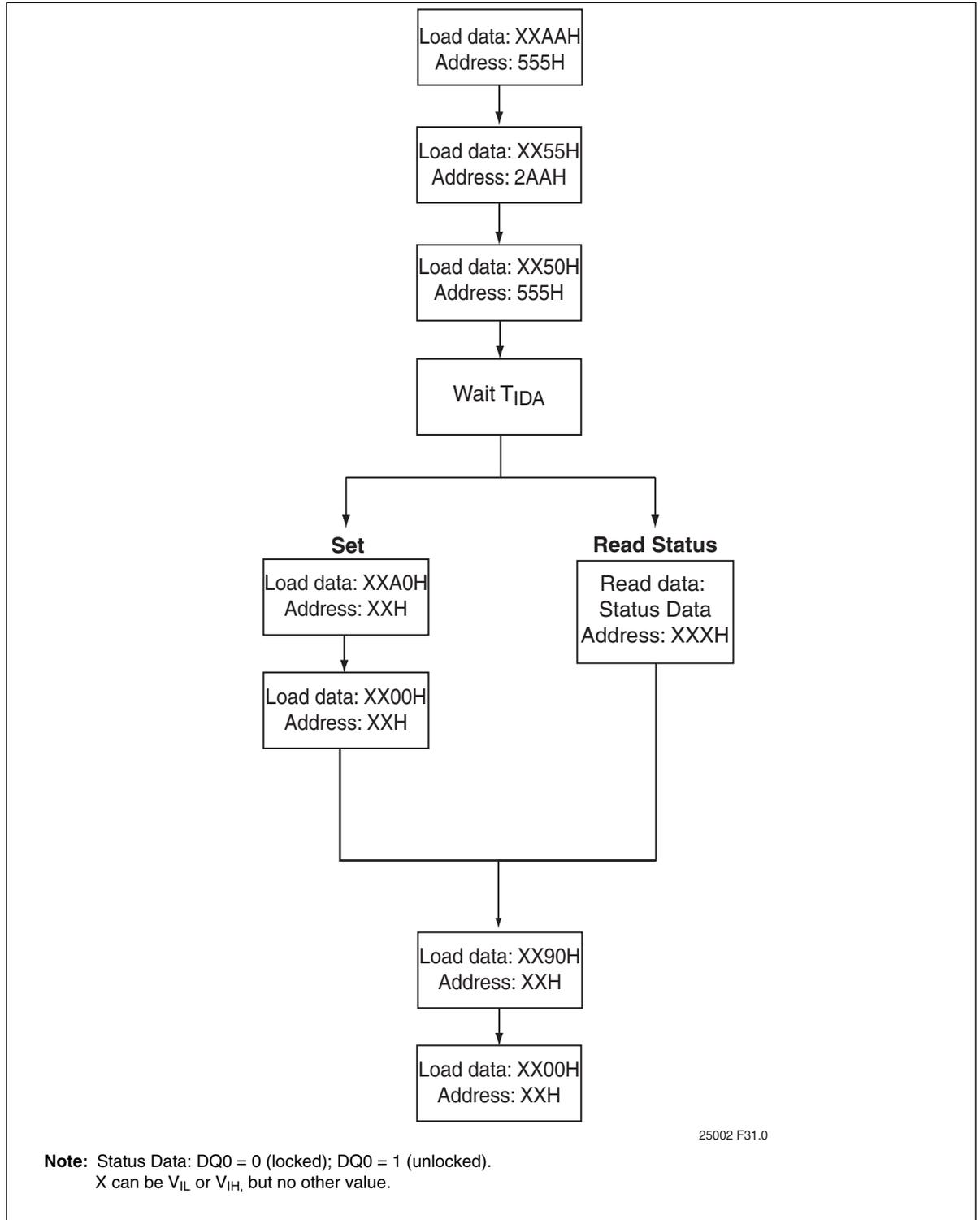


Figure 32: Global Lock of NVPBs



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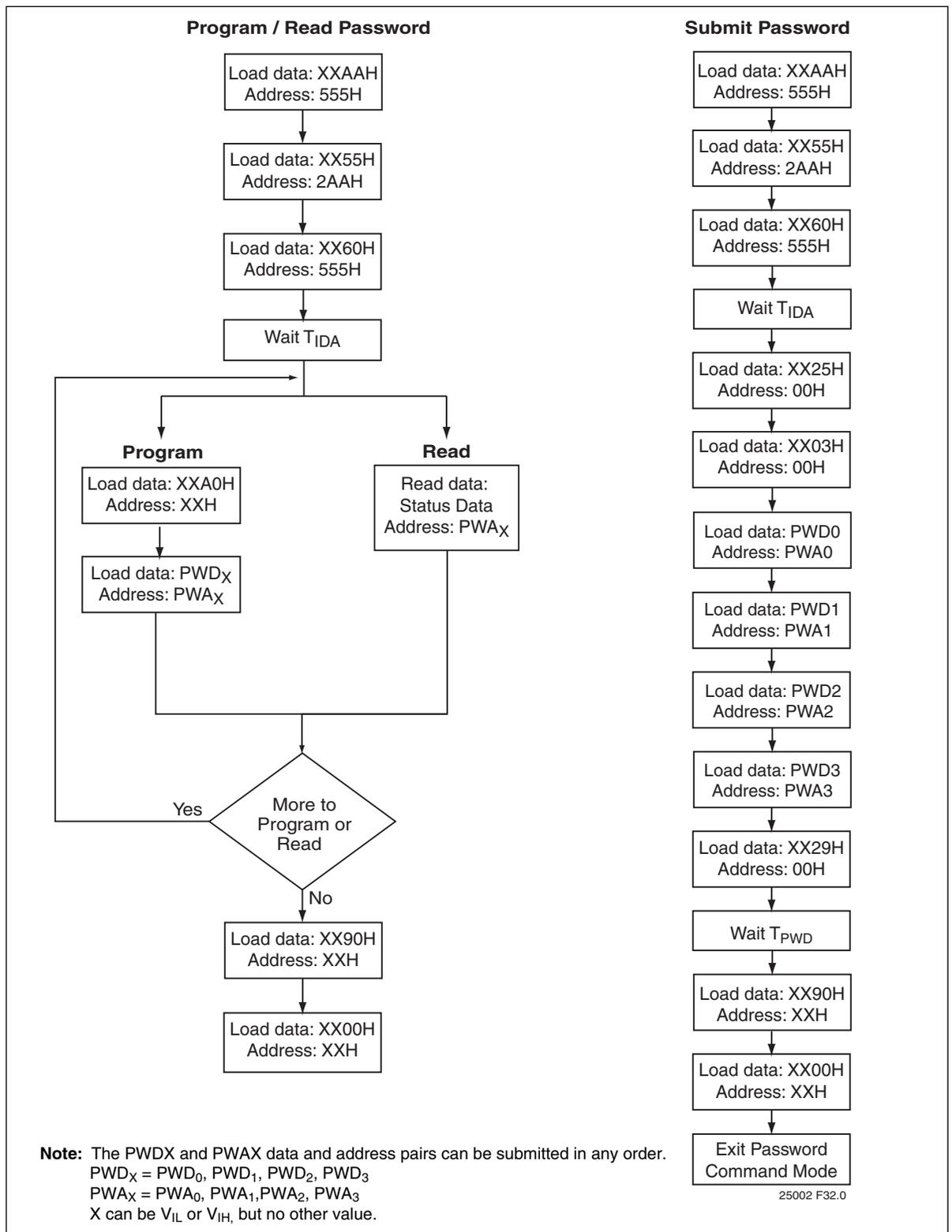


Figure 33: Password Operations (Program, Read, Submit)



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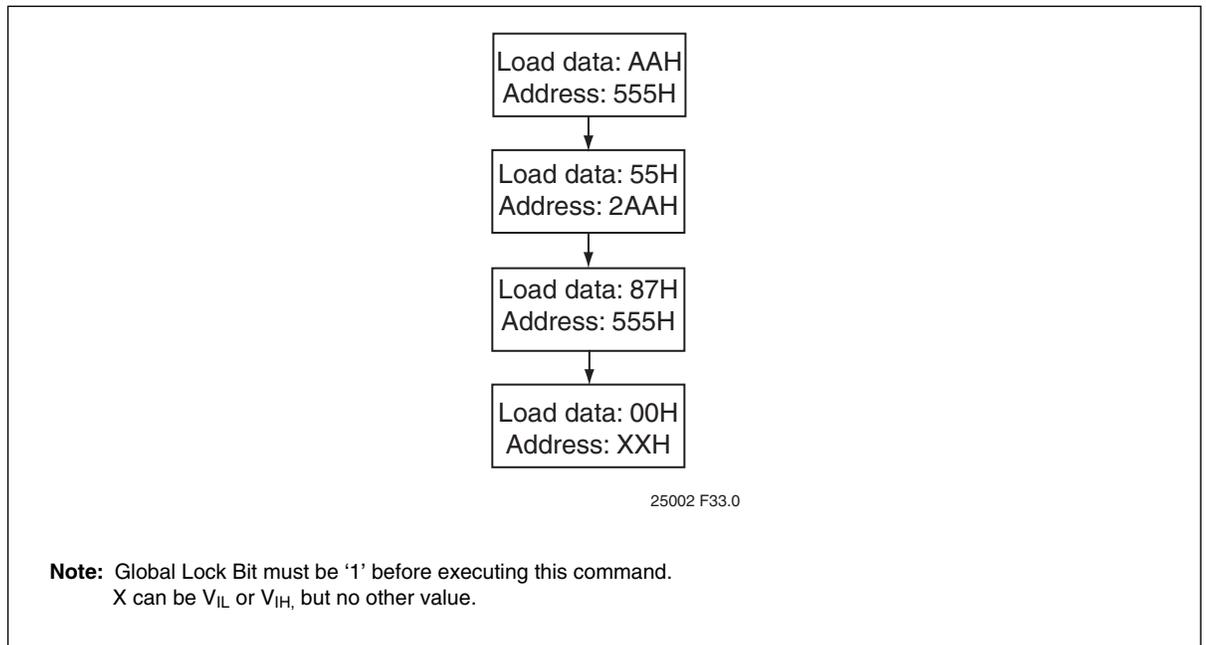


Figure 34: Irreversible Block Lock in Main Array



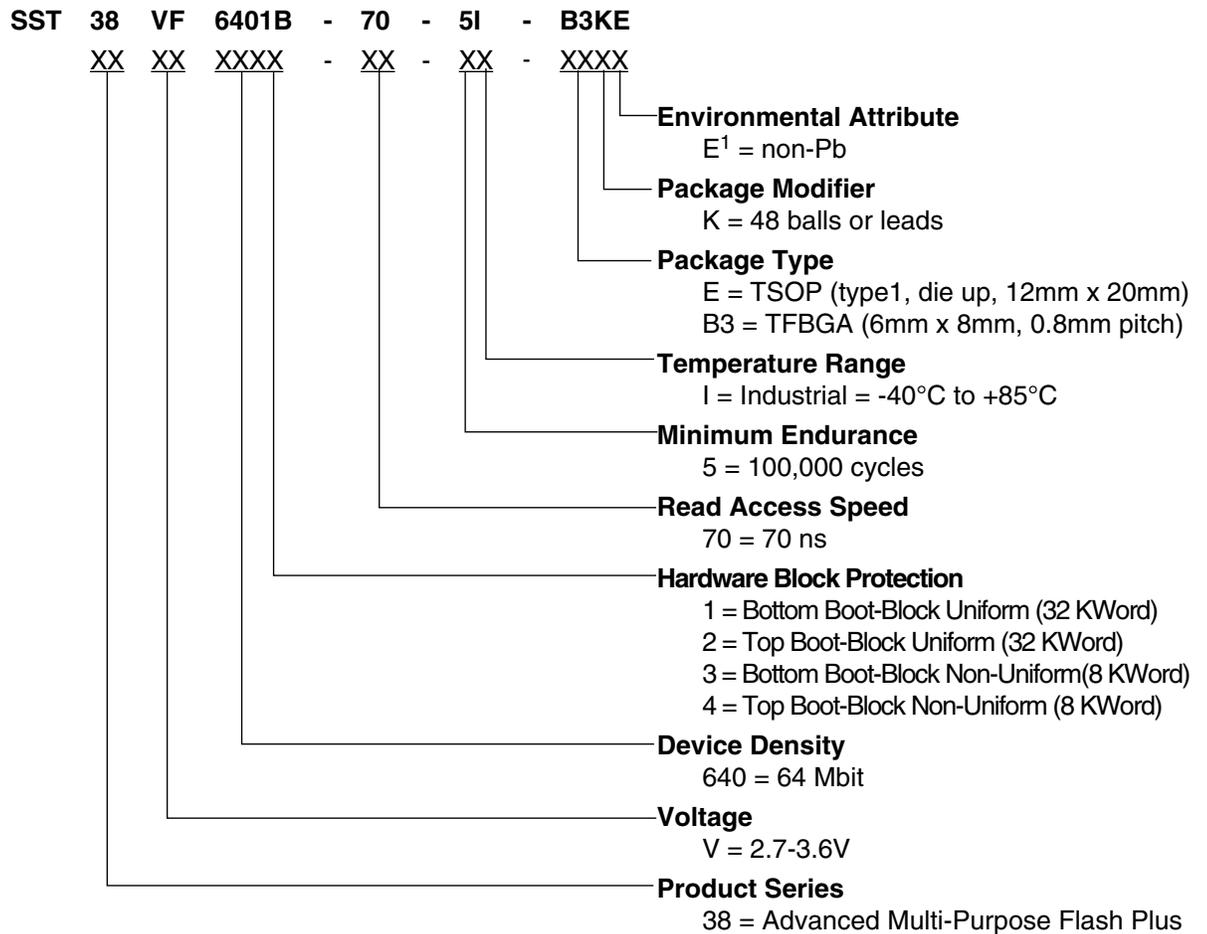
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Product Ordering Information



1. Environmental suffix "E" denotes non-Pb solder.
SST non-Pb solder devices are "RoHS Compliant".



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Valid Combinations

Valid Combinations for SST38VF6401B

SST38VF6401B-70-5I-EKE SST38VF6401B-70-5I-B3KE

Valid Combinations for SST38VF6402B

SST38VF6402B-70-5I-EKE SST38VF6402B-70-5I-B3KE

Valid Combinations for SST38VF6403B

SST38VF6403B-70-5I-EKE SST38VF6403B-70-5I-B3KE

Valid Combinations for SST38VF6404B

SST38VF6404B-70-5I-EKE SST38VF6404B-70-5I-B3KE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



Packaging Diagrams

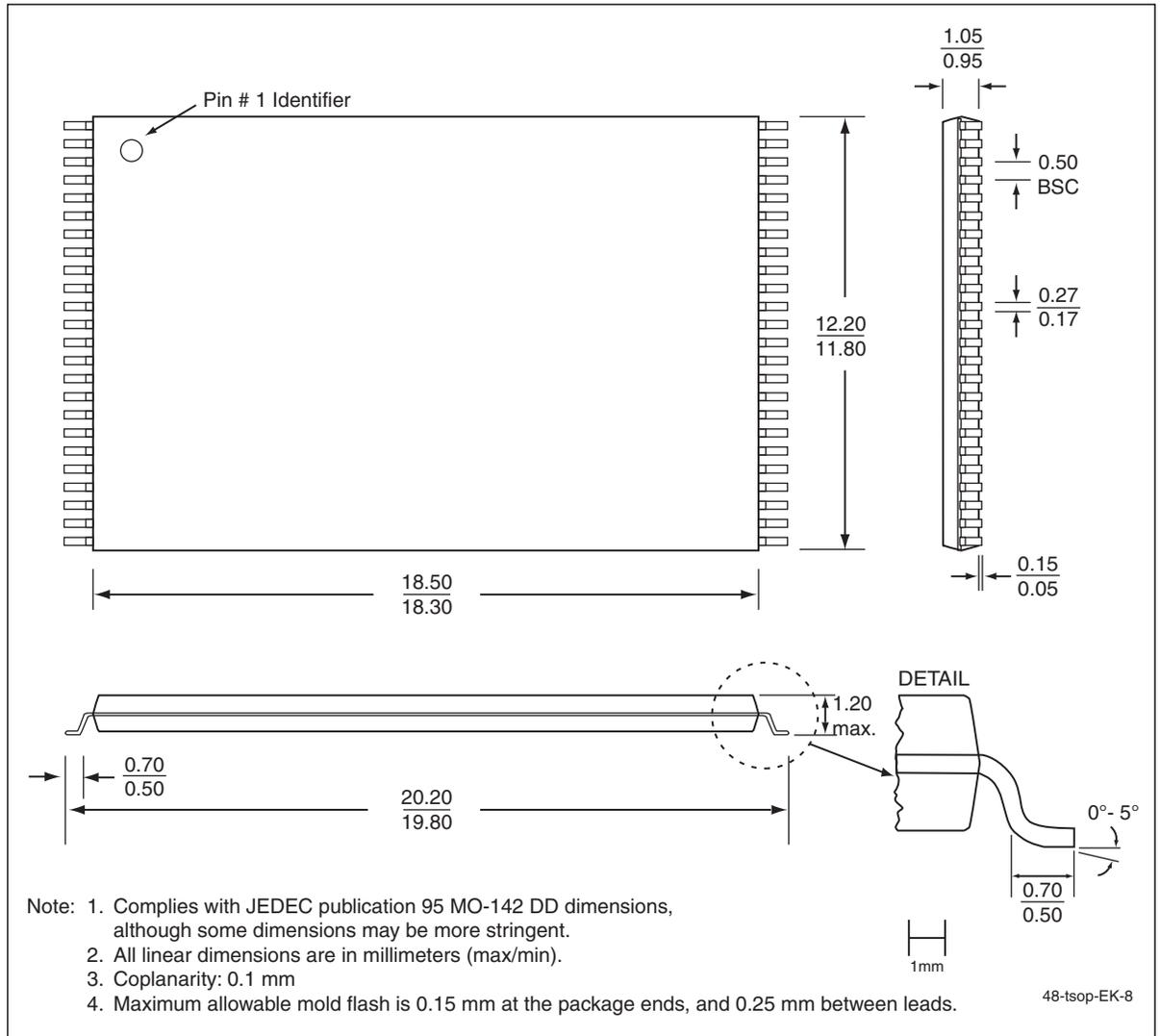


Figure 35:48-lead Thin Small Outline Package (TSOP) 12mm x 20mm
SST Package Code: EKE



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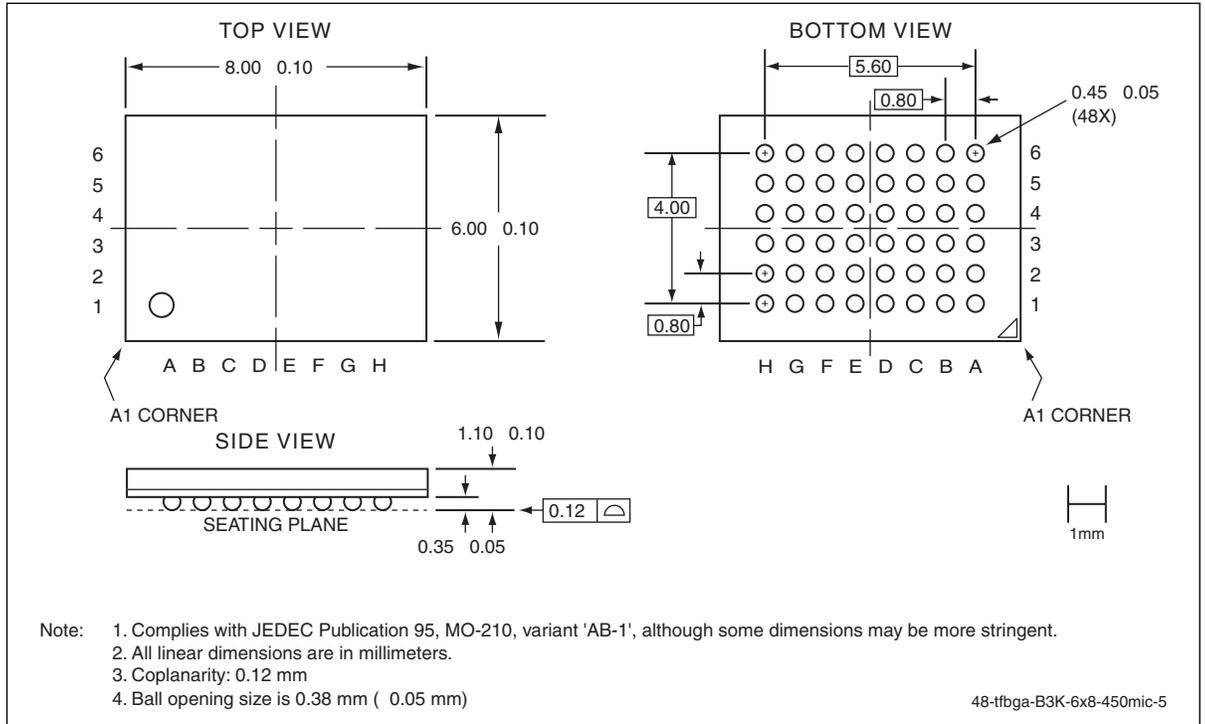


Figure 36: 48-ball Thin-profile, Fine-pitch Ball Grid Array (TFBGA) 6mm x 8mm
SST Package Code: B3KE



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SST38VF6403B / SST38VF6404B

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Table 25:Revision History

| Number | Description | Date |
|--------|---|----------|
| A | <ul style="list-style-type: none"> • Initial release | Aug 2011 |

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