IS31FL3726A

16-CHANNEL LED DRIVER

November 2022

GENERAL DESCRIPTION

The IS31FL3726A is an industry standard serial shift-register-plus latch-type LED driver operating from a 3V to 5V supply. It is comprised of 16 constant-current open drain sinks designed for driving common anode LEDs. The output current value can be set from 5mA to 60mA by using an external resistor. As a result, all outputs will have virtually the same current levels. This driver uses a high-speed 4-wire serial interface of up to 30MHz to drive 16 constant current outputs, a 16-bit shift register, a 16-bit latch and a 16-bit AND-gate circuit. Serial input data appears at the output $\overline{OUTn}$ channels after 16 clock cycles. Driving the Latch pin will load the 16-bit of shift-register data into the 16-bit output latch to drive the LEDs ON or OFF. The Enable pin can be used as a PWM input to adjust the LED brightness. The IS31FL3726A operates from a 3V to 5.5V supply, and is specified over the -40°C to +125°C temperature range.

APPLICATIONS

- Video display panel LED driver
- Point of sale signs
- Variable LED signboards

FEATURES

- Output current capability and number of outputs: 60mA × 16 outputs
- Current set with external resistor
- Constant current range: 5mA to 60mA
  I_{OUT_MAX}= 45mA @ V_{CC}= 3V
  I_{OUT_MAX}= 60mA @ V_{CC}= 5V
- Current accuracy (All output on, I_{OUT} = 25.2mA)
  - Bit to bit: < ±4%
  - Device to device: < ±2%
- 200mV LED Dropout at 25mA
- For common-anode LEDs
- Power supply voltage range, V_{CC}= 3.0V to 5.5V
- Serial and parallel data transfer rate: 30MHz (Max. cascade connection)
- Operating temperature range, T_A= -40°C ~ +125°C
- Package: QFN-24 (4mm×4mm), SSOP-24 and eTSSOP-24

TYPICAL APPLICATION CIRCUIT

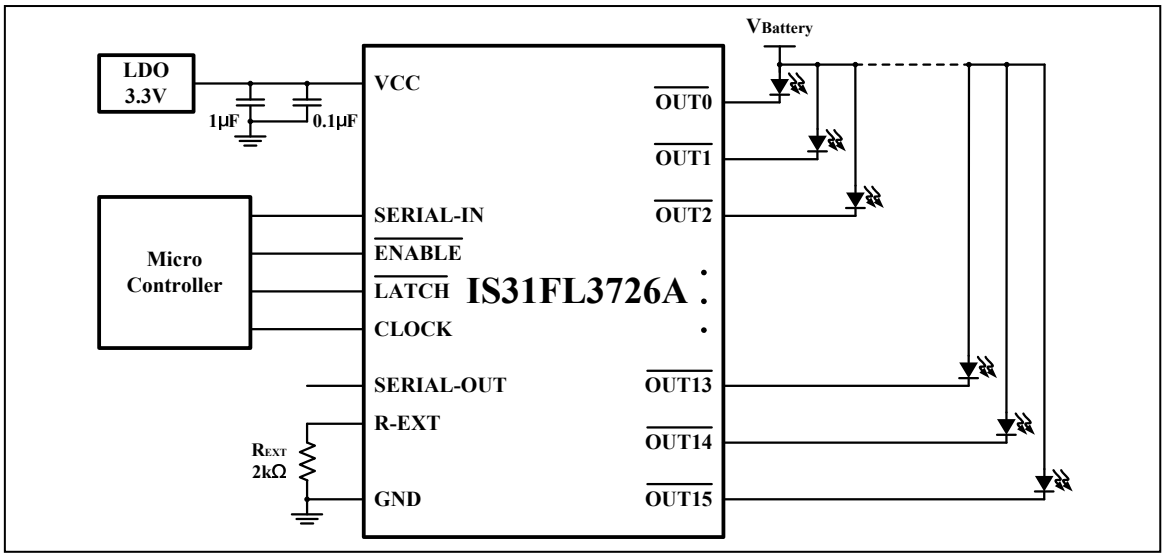


Figure 1 Typical Application Circuit

TYPICAL APPLICATION CIRCUIT (CONTINUE)

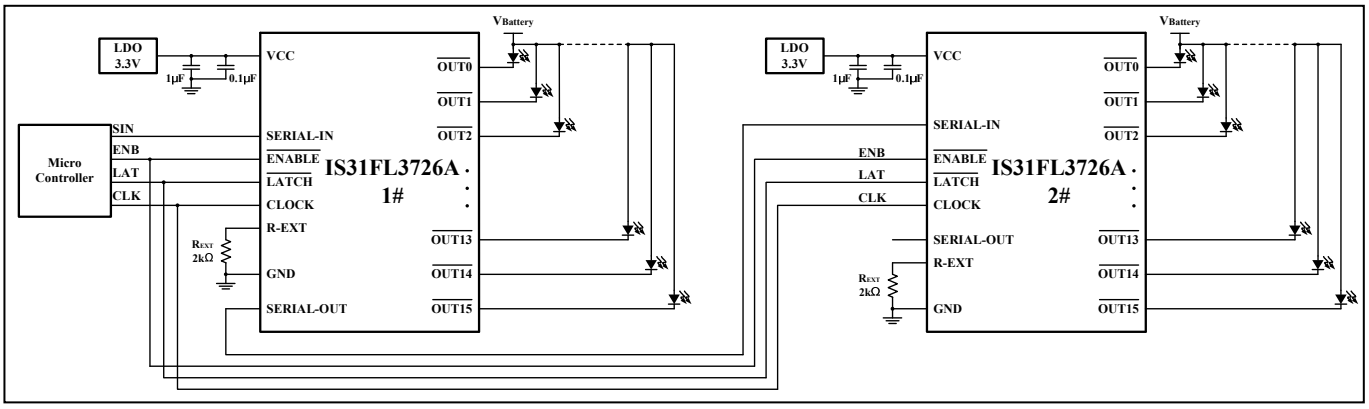
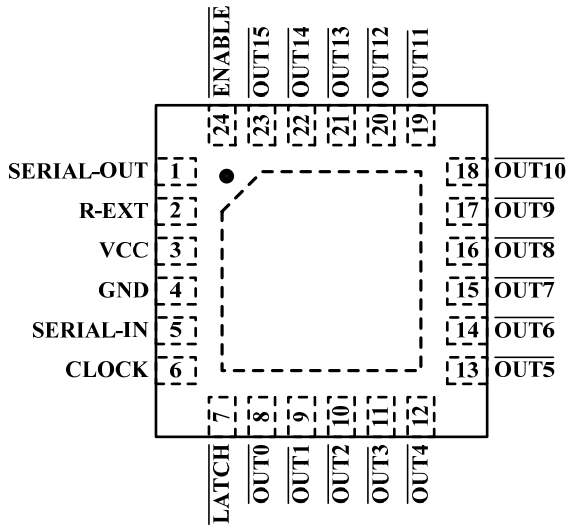
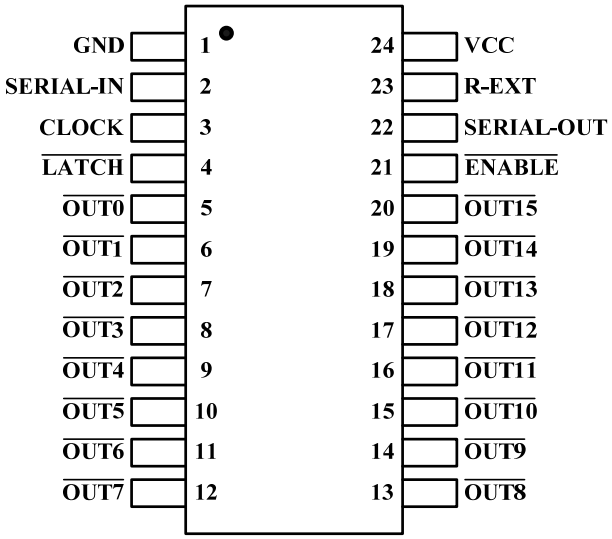
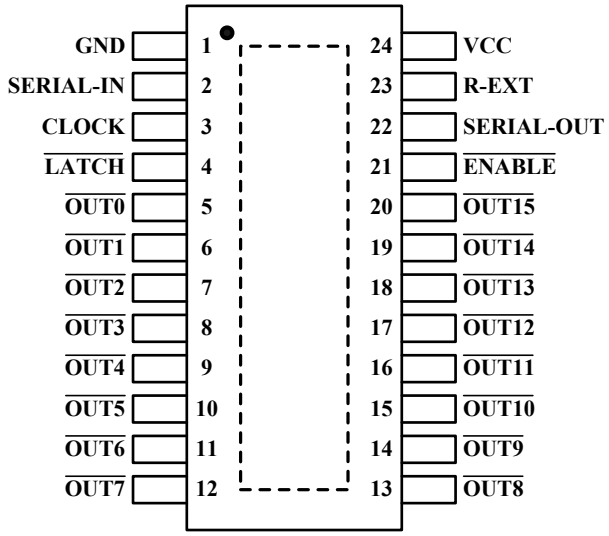


Figure 2 Typical Application Circuit (Serial Synchronization)

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-24	
SSOP-24	
eTSSOP-24	

PIN DESCRIPTION

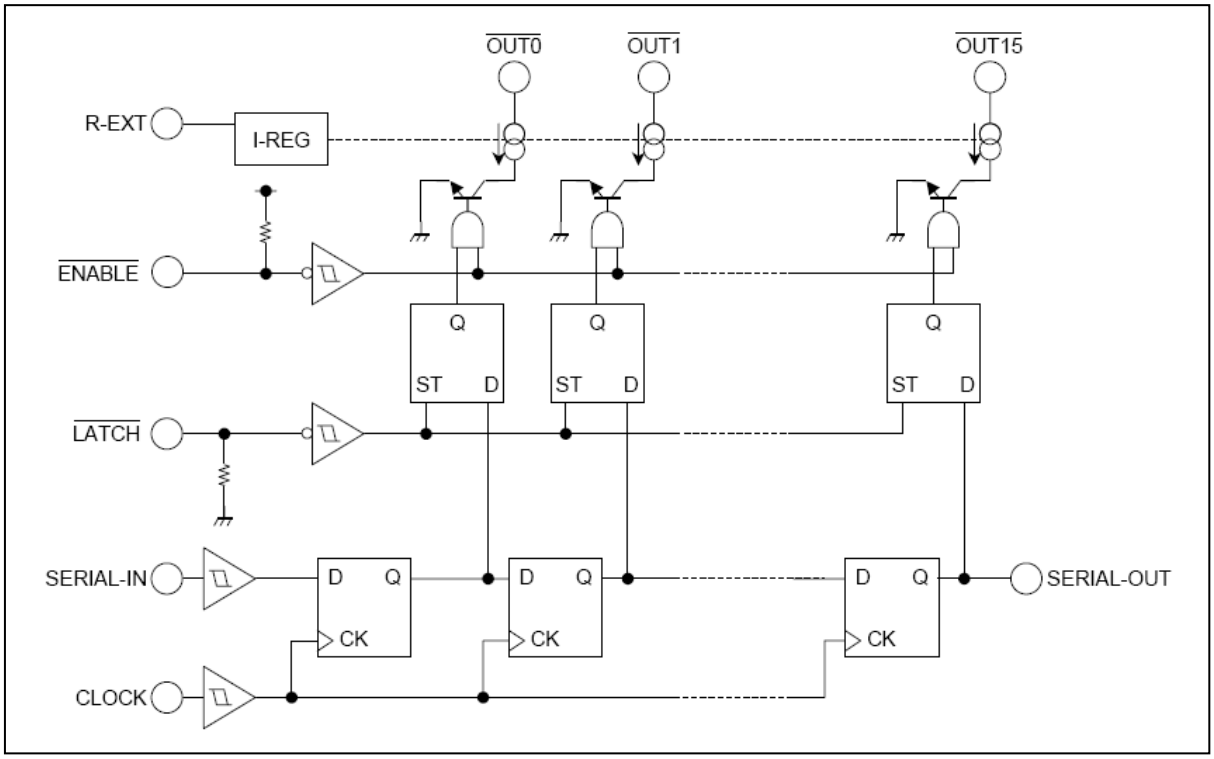
No.		Pin	Description
QFN	SSOP/eTSSOP		
1	22	SERIAL-OUT	Output pin for serial data input on SERIAL-IN terminal.
2	23	R-EXT	Input pin connect to an external resistor to regulate the output current.
3	24	VCC	Supply voltage pin.
4	1	GND	GND pin for control logic.
5	2	SERIAL-IN	Input pin for serial data for data shift register.
6	3	CLOCK	Input pin for clock for data shift on rising edge.
7	4	$\overline{\text{LATCH}}$	Input pin for data strobe when the $\overline{\text{LATCH}}$ input is driven low, data is not latched. When it is pulled high, data is latched.
8 ~ 23	5~20	$\overline{\text{OUT0}}$~$\overline{\text{OUT15}}$	Constant-current sinks.
24	21	$\overline{\text{ENABLE}}$	Input pin for output enable. All current sinks ($\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$) are turned off, when the $\overline{\text{ENABLE}}$ pin is driven High and are turned on, when this pin is driven Low.
		Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
IS31FL3726A-QFLS4-TR	QFN-24, Lead-free	2500/Reel
IS31FL3726A-SALS4-TR IS31FL3726A-SALS4	SSOP-24, Lead-free	2000/Reel 58/Tube
IS31FL3726A-ZLS4-TR	eTSSOP-24, Lead-free	2500/Reel

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply voltage, VCC	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.2V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Junction package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	29.1°C/W (QFN) 70.3°C/W (SSOP) 28.1°C/W (eTSSOP)
Maximum power dissipation, P_{DMAX}	3.44W (QFN) 1.42W (SSOP) 3.56W (eTSSOP)
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

T_A = 25°C, unless otherwise specified.

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
V_{OUT}	Output (headroom) voltage			0.7	5	V
f_{CLK}	Clock frequency (Note 2)	Cascade connected			30	MHz
t_{wLAT}	$\overline{LATCH}$ pulse width		20			ns
t_{wCLK}	CLOCK pulse width		20			ns
t_{wENA}	$\overline{ENABLE}$ pulse width (Note 2, 3)		70			ns
t_{SETUP1}	SERIAL-IN set-up time for CLOCK pin		8			ns
t_{HOLD1}	SERIAL-IN Hold time for CLOCK pin		8			ns
t_{SETUP2}	Set-up time for $\overline{LATCH}$ pin		8			ns
t_{HOLD2}	Hold time for $\overline{LATCH}$ pin		8			ns

Note 2: Guaranteed by design.

Note 3: When the pulse of the Low level is input to the $\overline{ENABLE}$ pin held in the High level.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC}= 3.3V ~ 5.5V, unless otherwise specified.

Symbol	Characteristic	Condition		Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	Normal operation		3.0		5.5	V
I_{OUT}		V_{OUT}= 1V,V_{CC}= 3.3V	R_{EXT} = 750Ω	23.9	25.2	26.5	mA
		V_{OUT}= 1V,V_{CC}= 5V	R_{EXT} = 750Ω	23.9	25.2	26.5	
$\triangle I_{MAT}$	Output current error between bits (Note 5)	V_{OUT} = 1V, V_{CC} = 3.3V	R_{EXT} = 750Ω I_{OUT}=25.2mA	-4		4	%
		V_{OUT} = 1V, V_{CC} = 5V	R_{EXT} = 750Ω I_{OUT}=25.2mA	-4		4	%
$\triangle I_{OUT}$	Output current error between ICs (Note 6)	V_{OUT} = 1V, V_{CC} = 3.3V	R_{EXT} = 750Ω I_{OUT}=25.2mA	-2		2	%
		V_{OUT} = 1V, V_{CC} = 5V	R_{EXT} = 750Ω I_{OUT}=25.2mA	-2		2	%
V_{HR}	Headroom voltage	R_{EXT} = 750Ω, I_{OUT}= 25.2mA			0.4	0.5	V
I_{OZ}	Output leakage current input voltage	V_{OUT} = 5.5V				1	μA
V_{IH}	Input voltage	Logic high level		0.7V_{CC}			V
V_{IL}		Logic low level				0.3V_{CC}	
V_{OL}	SERIAL-OUT pin voltage	I_{OL} = 1.0mA, V_{CC} = 3.3V				0.4	V
		I_{OL} = 1.0mA, V_{CC} = 5V				0.4	
V_{OH}		I_{OH} = -1.0mA, V_{CC} = 3.3V		2.9			
		I_{OH} = -1.0mA, V_{CC} = 5V		4.6			
%/V_{CC}	Output current supply voltage regulation	When V_{CC} is changed 3.3V to 5.5V, I_{OUT}= 25.2mA				1	%
$R_{(UP)}$	Pull-up resistor	$\overline{ENABLE}$ pin		250	500	750	kΩ
$R_{(DOWN)}$	Pull-down resistor	$\overline{LATCH}$ pin					
$I_{DD(OFF)1}$	Supply current	V_{OUT} = 5V	R_{EXT} = OPEN		0.3	0.6	mA
$I_{DD(OFF)2}$		V_{OUT} = 5V All outputs off	R_{EXT} = 0.75kΩ		2.1	2.5	
			R_{EXT} = 1.8kΩ		1	1.2	
$I_{DD(ON)1}$		V_{OUT} = 0.7V All outputs on	R_{EXT} = 0.75kΩ		8.6	10	
			R_{EXT} = 1.8kΩ		4.5	6	

SWITCHING CHARACTERISTICS (NOTE 4)

T_A= 25°C, unless otherwise specified

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
t_{pLH1}	Propagation delay	CLOCK - $\overline{OUTn}$, $\overline{LATCH}$= "H" $\overline{ENABLE}$= "L"		30	50	ns
t_{pLH2}		$\overline{LATCH}$ - $\overline{OUTn}$, $\overline{ENABLE}$= "L"		30	50	
t_{pLH3}		$\overline{ENABLE}$ - $\overline{OUTn}$, $\overline{LATCH}$= "H"		50	70	
t_{pLH}		CLOCK - SERIAL-OUT		20	40	
t_{pHL1}		CLOCK - $\overline{OUTn}$, $\overline{LATCH}$= "H" $\overline{ENABLE}$= "L"		60	100	
t_{pHL2}		$\overline{LATCH}$ - $\overline{OUTn}$, $\overline{ENABLE}$= "L"		60	100	
t_{pHL3}		$\overline{ENABLE}$ - $\overline{OUTn}$, $\overline{LATCH}$= "H"		70	100	
t_{pHL}		CLOCK - SERIAL-OUT		20	40	
t_{or}	Output rise time	10%~90% of voltage waveform		30	50	ns
t_{of}	Output fall time	90%~10% of voltage waveform		52	80	ns
t_r	Maximum CLOCK rise time	When not on PCB (Note 7)			500	ns
t_f	Maximum CLOCK fall time				500	ns

Conditions: (Refer to test circuit.)

T_A = 25°C, V_{CC}=V_{IH} =3.3V and 5V, V_{IL} =0V, R_{EXT} =750Ω, V_L =3.0V, R_L=60Ω, C_L=10.5pF

Note 4: Guaranteed by design.

Note 5: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn}(n=0\sim15)}{\left(\frac{I_{OUT0}+I_{OUT1}+...+I_{OUT15}}{16}\right)} - 1 \right) \times 100\%$$

Note 6: I_{OUT} accuracy (device to device) $\triangle I_{OUT}$ is calculated:

$$\Delta I_{OUT} = \left(\frac{\left(\frac{I_{OUT0}+I_{OUT1}+...+I_{OUT15}}{16} - I_{OUT(IDEAL)}\right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 10.5mA when R_{EXT}= 1800Ω, $I_{OUT(IDEAL)}$= 25.2mA when R_{EXT}= 750Ω.

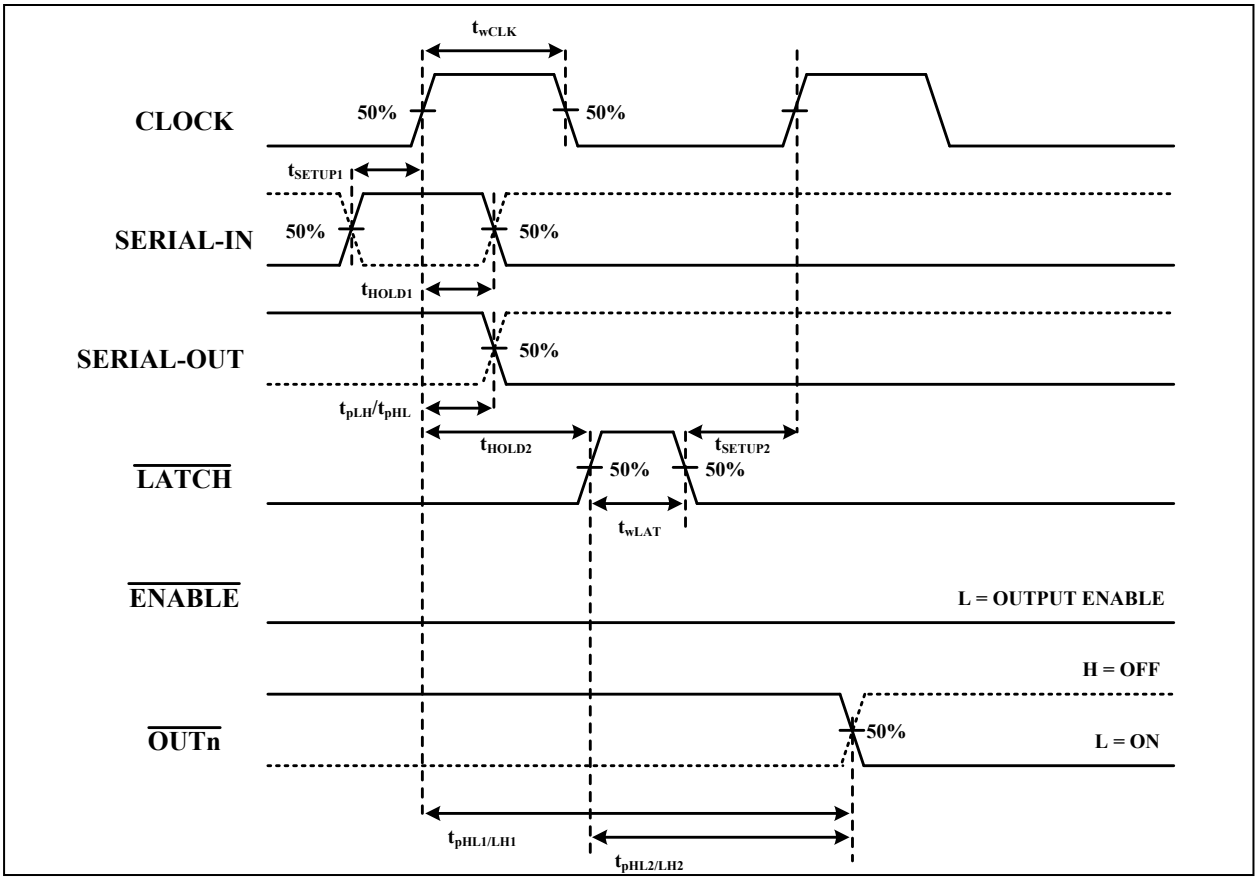
Note 7:

1. If the device is connected in a cascade and tr/tf for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

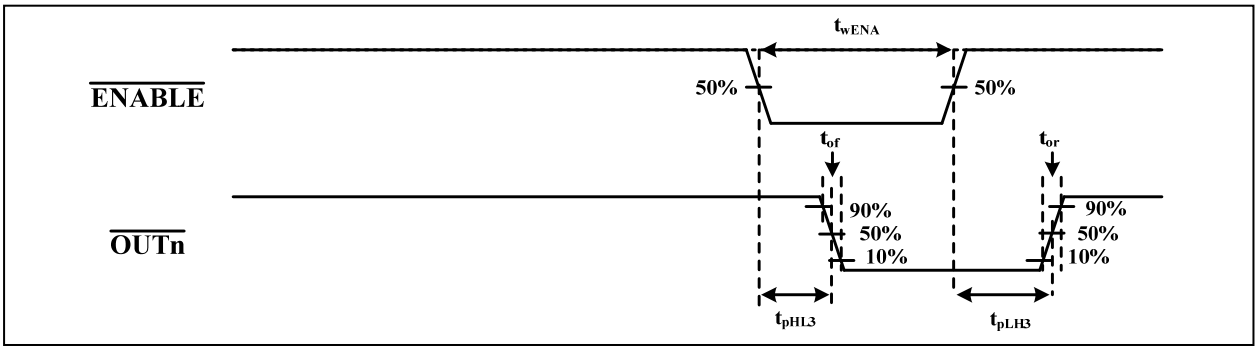
2. Delay between outputs. The IS31FL3726A has graduated delay circuits between outputs. The fixed delay time is 5ns (typical), $\overline{OUT1}$ has 5ns delay, $\overline{OUT2}$ has 10ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on. The delay works during switch on and switch off of each output channel. LEDs that have not turned on before $\overline{ENABLE}$ is low will still turn on and off at the determined delayed time regardless of the state of $\overline{ENABLE}$. Therefore, every LED will be illuminated for the amount of time $\overline{ENABLE}$ is pulled high.

TIMING WAVEFORM

1. CLOCK, SERIAL-IN, SERIAL-OUT, $\overline{\text{LATCH}}$, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$



2. $\overline{\text{OUTn}}$



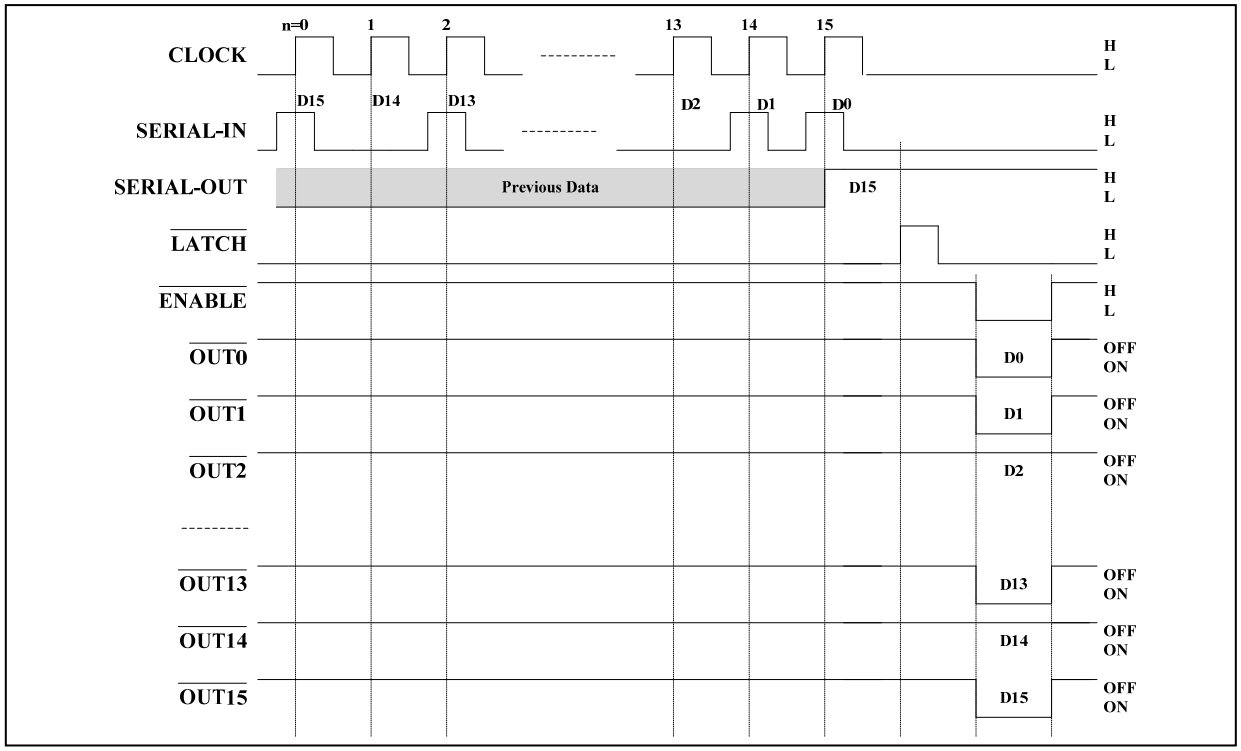


Figure 3 Timing Diagram

Warning: The Latch input is a logic levelit is not an edge triggered latch circuit.

Note 8: The serial-in data (SERIAL-IN) will be clocked into an 16-bit shift register synchronized on the rising edge of the clock (CLOCK). The data "1" means the corresponding current output "ON" for output, the data '0' represents for "OFF". The data will be transferred into the 16 bit latch register when the signal ($\overline{LATCH}$) is 'H' (level trigger); otherwise, the data will be latched. The trigger timing of the serial-out data (SERIAL-OUT) will be shifted out on synchronization to the rising edge of the clock. All outputs are turned off while enable terminal ($\overline{ENABLE}$) is kept at high level. And they are active when $\overline{ENABLE}$ turns to low.

Truth Table

CLOCK	$\overline{LATCH}$	$\overline{ENABLE}$	SERIAL-IN	$\overline{OUT0}$ …$\overline{OUT7}$ … $\overline{OUT15}$	SERIAL-OUT
↑	H	L	Dn	Dn …Dn-7 …Dn-15	Dn-15
↑	L	L	Dn+1	No change	Dn-14
↑	H	L	Dn+2	Dn+2 …Dn-5 …Dn-13	Dn-13
↓	X	L	Dn+3	Dn+2 …Dn-5 …Dn-13	Dn-13
↓	X	H	Dn+3	OFF	Dn-13

Warning: The following conditions, $\overline{ENABLE}$=0, $\overline{LATCH}$=1, SERIAL-IN=1, cannot be configured at the same time when power is on, or IS31FL3726A will behave unpredictably.

Note 9: $\overline{OUT0}$ to $\overline{OUT15}$ =On when Dn = H; $\overline{OUT0}$ to $\overline{OUT15}$ =Off when Dn = L. In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between R-EXT and GND.

TYPICAL TEST CHARACTERISTICS

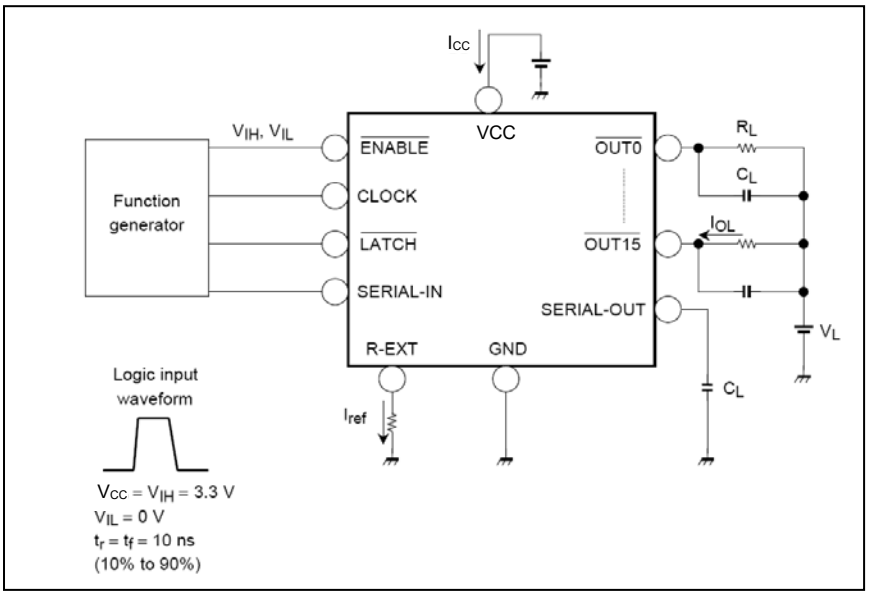


Figure 4 Test Diagram

APPLICATION INFORMATION

ADJUSTING OUTPUT CURRENT

The output current of each channel is set by an external resistor R_{EXT}, the relationship between I_{OUT} and R_{EXT} is:

$$I_{OUT} = k \times \frac{V_{REXT}}{R_{EXT}}$$

Where V_{REXT} is 1.26V, k is 15, so I_{OUT} is calculated by Equation (1):

$$I_{OUT} = 15 \times \frac{1.26V}{R_{EXT}} \qquad (1)$$

As show in the figure below:

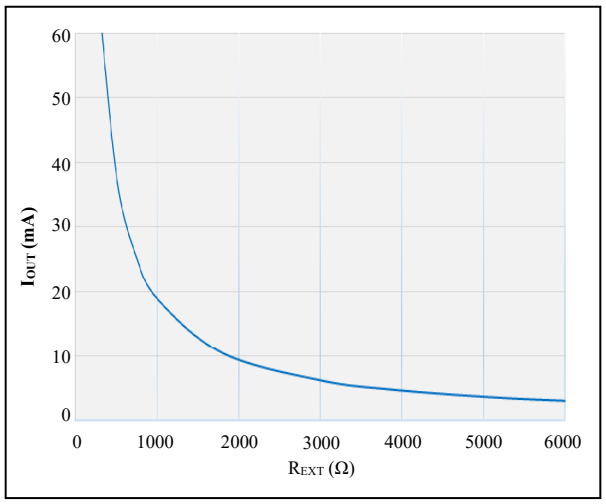


Figure 5 I_{OUT} vs. R_{EXT}

CONSTANT CURRENT OUTPUT

In order to obtain a good performance of constant-current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage below.

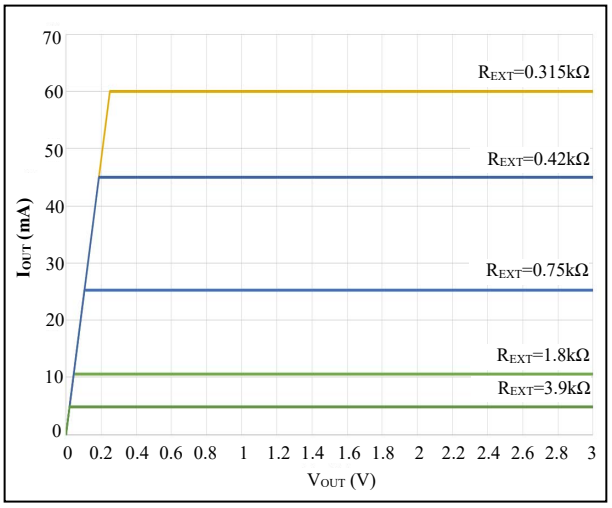


Figure 6 I_{OUT} vs. V_{OUT}

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (2):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad (2)$$

So, $P_{D(MAX)} = \frac{125°C - 25°C}{29.1°C/W} \approx 3.44W$ (QFN)

$$P_{D(MAX)} = \frac{125°C - 25°C}{70.3°C/W} \approx 1.42W \text{ (SSOP)}$$

$$P_{D(MAX)} = \frac{125°C - 25°C}{28.1°C/W} \approx 3.56W \text{ (eTSSOP)}$$

Figure 7 shows the power derating of the IS31FL3726A on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

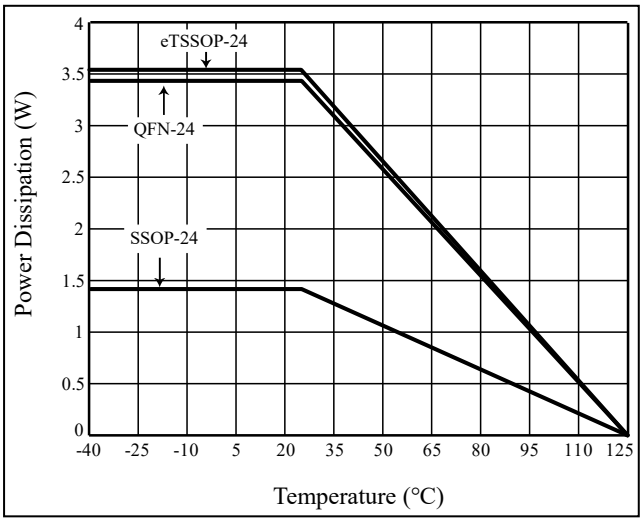


Figure 7 Dissipation Curve

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

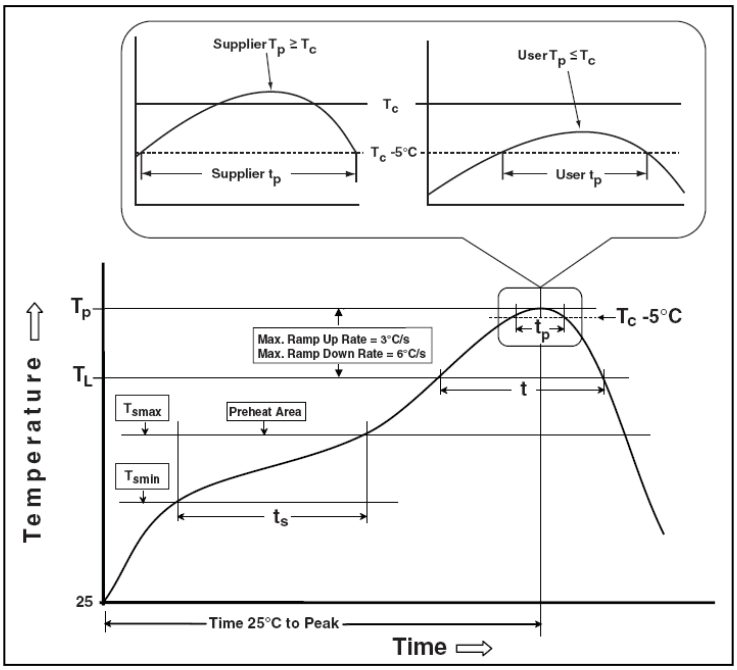
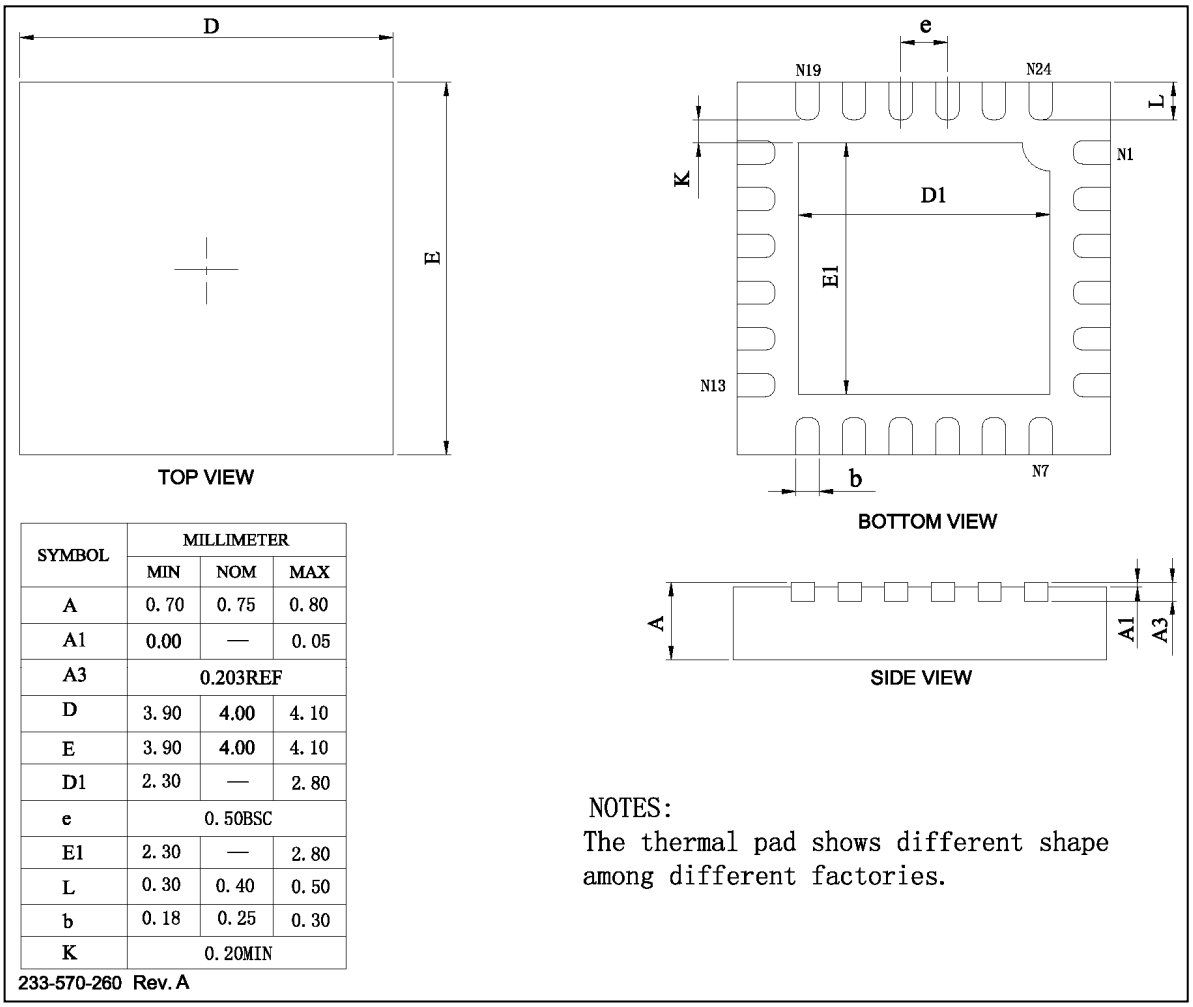


Figure 8 Classification Profile

PACKAGE INFORMATION

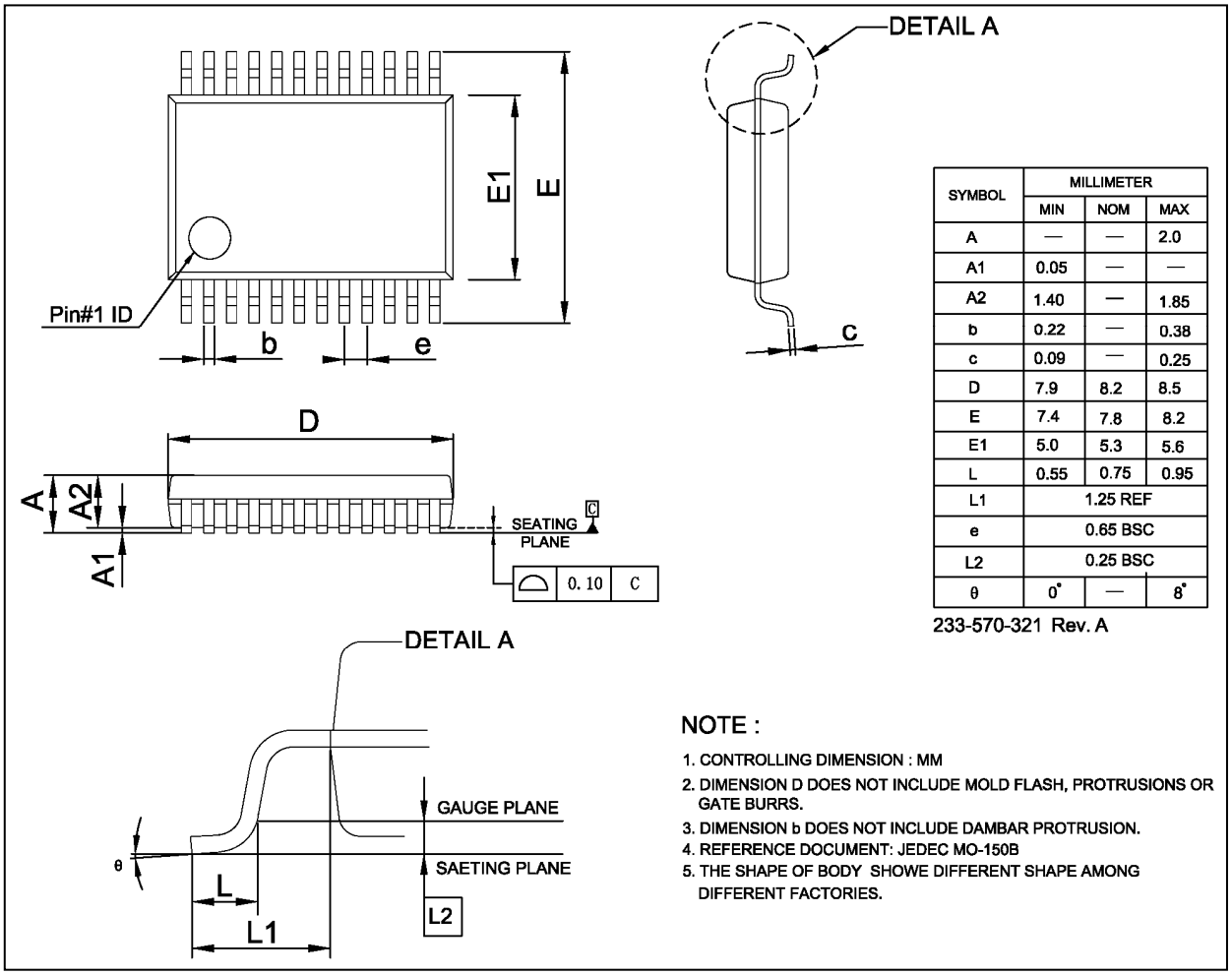
QFN-24



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.30	—	2.80
e	0.50BSC		
E1	2.30	—	2.80
L	0.30	0.40	0.50
b	0.18	0.25	0.30
K	0.20MIN		

233-570-260 Rev. A

SSOP-24



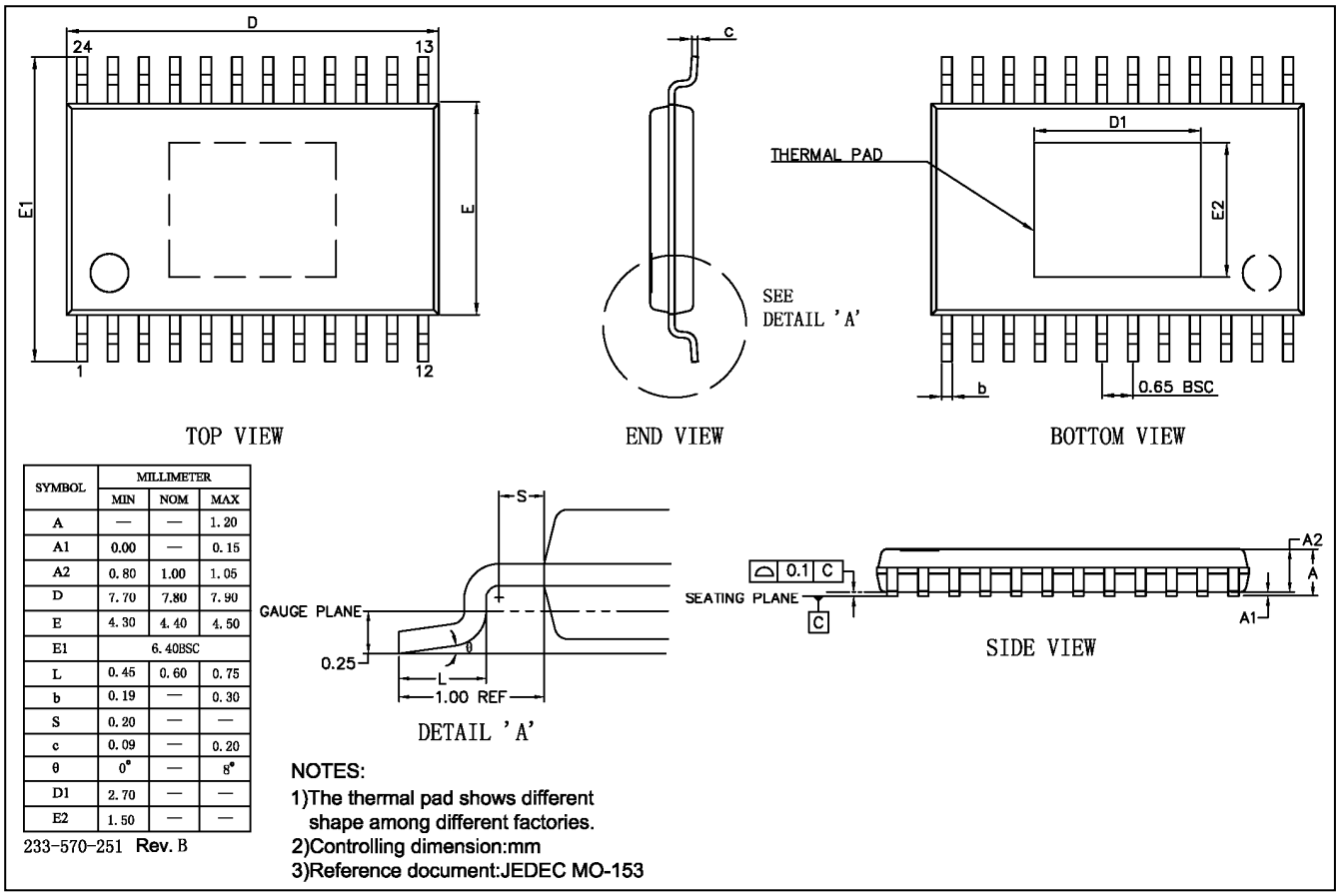
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.0
A1	0.05	—	—
A2	1.40	—	1.85
b	0.22	—	0.38
c	0.09	—	0.25
D	7.9	8.2	8.5
E	7.4	7.8	8.2
E1	5.0	5.3	5.6
L	0.55	0.75	0.95
L1	1.25 REF		
e	0.65 BSC		
L2	0.25 BSC		
θ	0°	—	8°

233-570-321 Rev. A

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MO-150B
5. THE SHAPE OF BODY SHOWE DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

eTSSOP-24



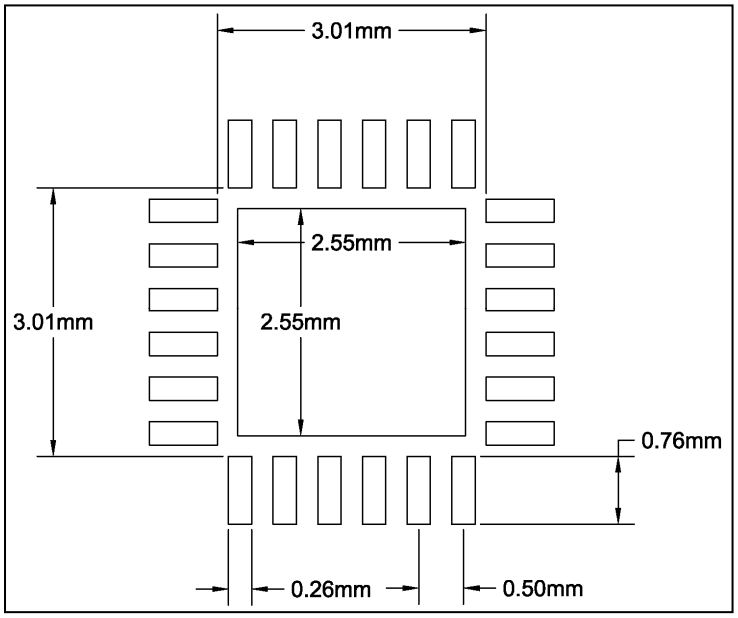
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	1.00	1.05
D	7.70	7.80	7.90
E	4.30	4.40	4.50
E1	6.40BSC		
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°
D1	2.70	—	—
E2	1.50	—	—

233-570-251 Rev. B

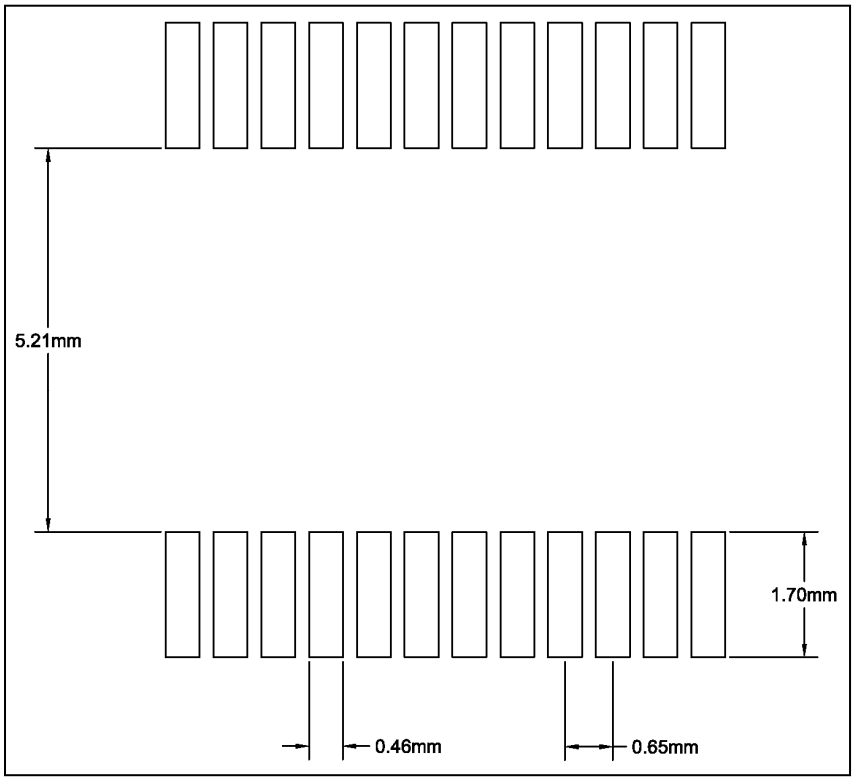
NOTES:
1)The thermal pad shows different shape among different factories.
2)Controlling dimension:mm
3)Reference document:JEDEC MO-153

RECOMMENDED LAND PATTERN

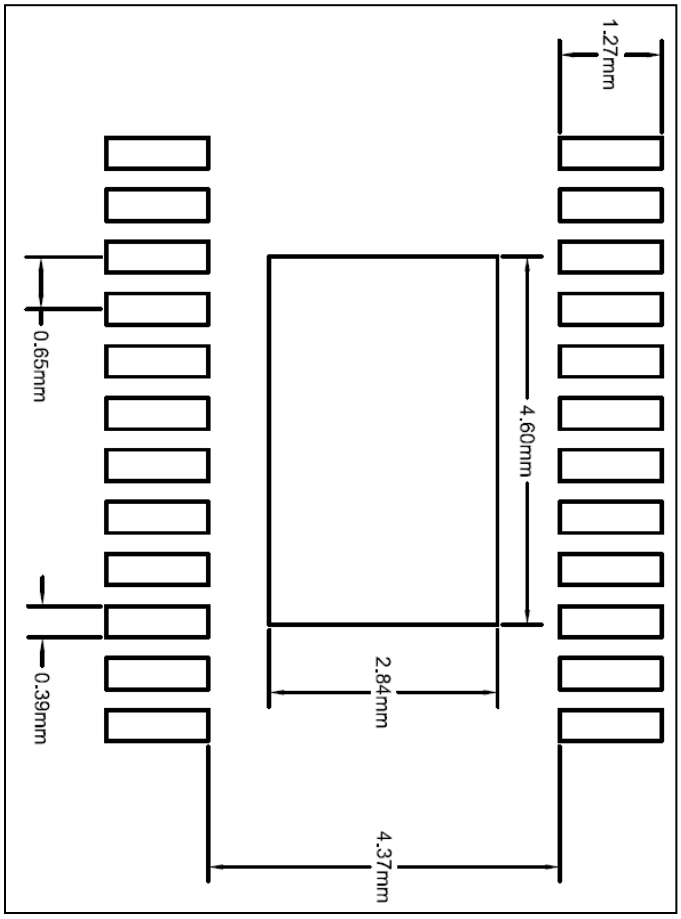
QFN-24



SSOP-24



eTSSOP-24



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Update to Lumissil Logo	2020.01.22
0B	Update typical application circuit, EC table and application information	2020.06.04
A	Release to mass production	2020.06.23
B	Change SSOP-24 package QTY to 2000/Reel	2022.11.10