CIPOS™ Mini

IM512-L6A

Description

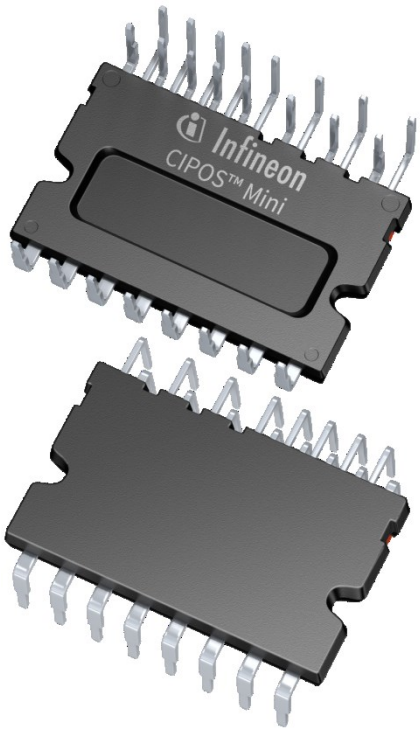
The CIPOS™ Mini family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs.

It is designed to control two phase AC motors for applications like refrigerator with linear compressor. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also EMI-save control and overload protection.

2Φ-bridges with CoolMOS™ CFD2 Power MOSFETs are combined with an optimized SOI gate driver for excellent electrical performance.

Features

- Fully isolated Dual In-Line molded module
- 650V CoolMOS™ CFD2 Power MOSFETs
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative VS potential up to -11V for signal transmission at VBS=15V
- Integrated bootstrap functionality
- Over-current shutdown
- Built-in NTC thermistor for temperature monitor
- Under-voltage lockout at all channels
- Low-side source pins accessible for all phase current monitoring (open source)
- Cross-conduction prevention
- All of 4 switches turn off during protection
- Lead-free terminal plating; RoHS compliant



Potential applications

- Two phase linear compressor for Refrigerators and single phase low power motor drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Product Information

Base Part Number	Package Type	Standard Pack		Remark
		Form	Quantity	
IM512-L6A	DIP 36x21	20 tubes	280 pcs	

Table of Contents

1 Internal Electrical Schematic

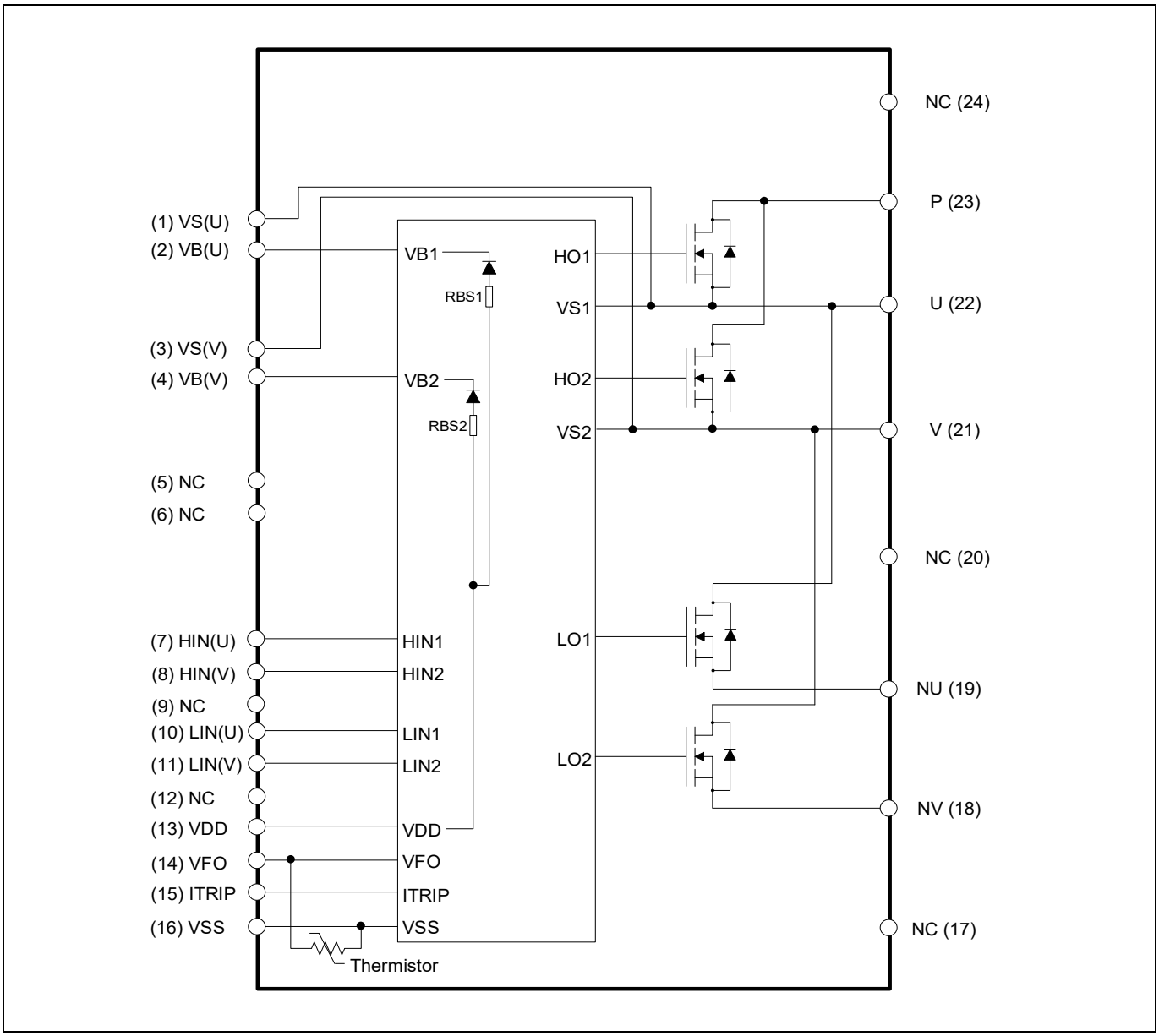


Figure 1 Internal electrical schematic

2 Pin Description

2.1 Pin Assignment

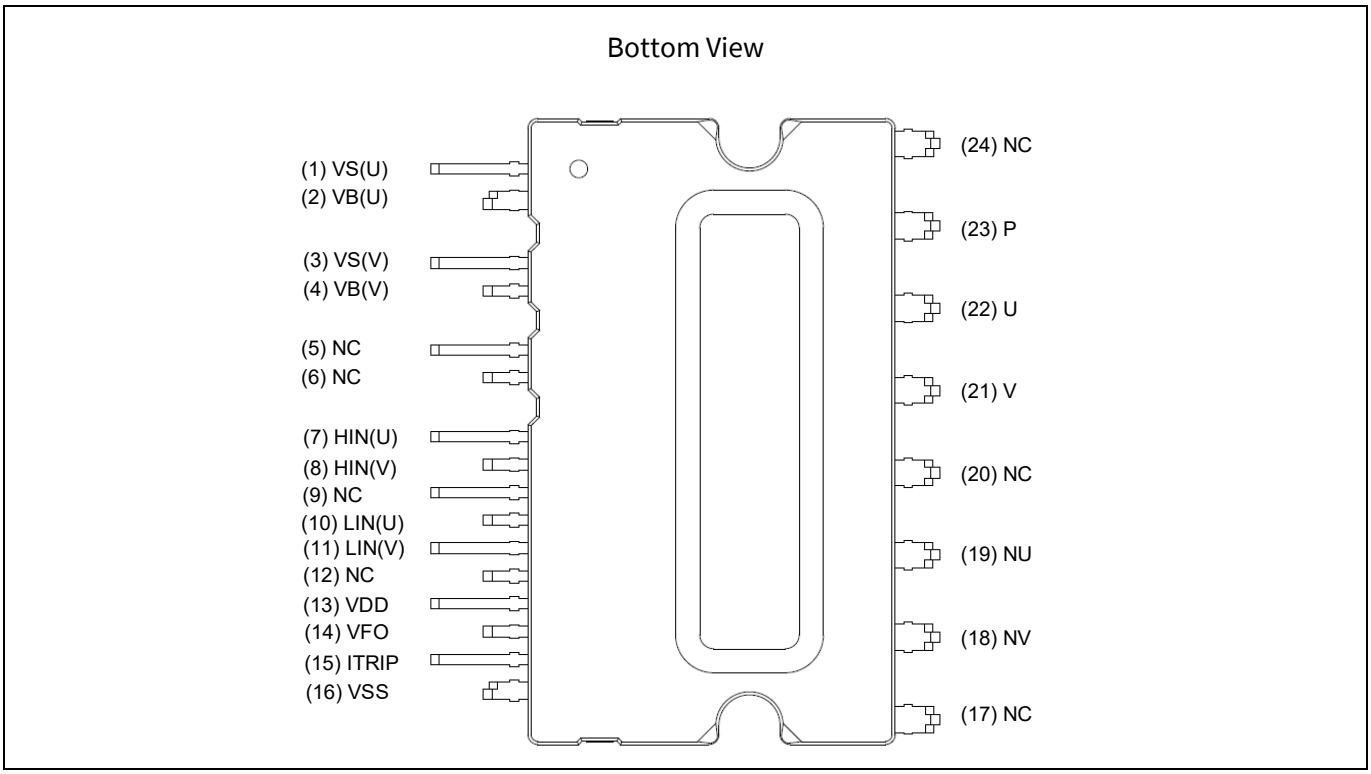


Figure 2 Pin configuration

Table 2 Pin assignment

Pin Number	Pin name	Pin Description
1	VS(U)	U-phase high-side floating IC supply offset voltage
2	VB(U)	U-phase high-side floating IC supply voltage
3	VS(V)	V-phase high-side floating IC supply offset voltage
4	VB(V)	V-phase high-side floating IC supply voltage
5	NC	No connection
6	NC	No connection
7	HIN(U)	U-phase high-side gate driver input
8	HIN(V)	V-phase high-side gate driver input
9	NC	No connection
10	LIN(U)	U-phase low-side gate driver input
11	LIN(V)	V-phase low-side gate driver input
12	NC	No connection
13	VDD	Low-side control supply
14	VFO	Fault output / Temperature monitor
15	ITRIP	Over-current shutdown input

Pin Description

Pin Number	Pin name	Pin Description
16	VSS	Low-side control negative supply
17	NC	No connection
18	NV	V-phase low-side source
19	NU	U-phase low-side source
20	NC	No connection
21	V	Motor V-phase output
22	U	Motor U-phase output
23	P	Positive bus input voltage
24	NC	No connection

2.2 Pin Description

HIN(U, V) and LIN(U, V) (Low-side and high-side control pins, Pin 7, 8, 10 and 11)

These pins are positive logic and they are responsible for the control of the integrated MOSFET. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Pull-down resistor of about 5 kΩ is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input Schmitt-trigger and noise filter provide noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time t_{FILIN}. The filter acts according to Figure 4.

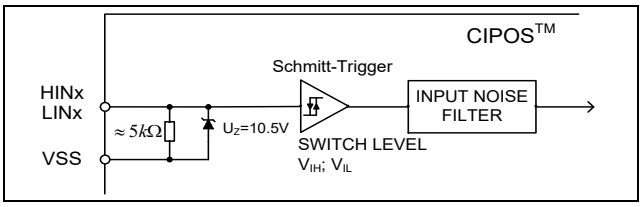


Figure 3 Input pin structure

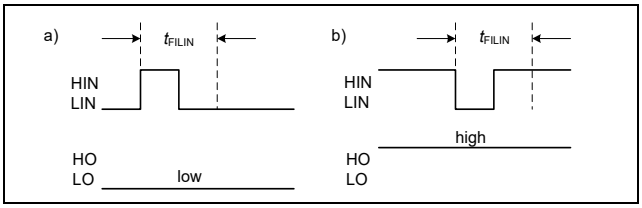


Figure 4 Input filter timing diagram

It is not recommended for proper work to provide input pulse-width lower than 1µs.

The integrated gate drive provides additionally a shoot-through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2). When two inputs of a same leg are activated, only former activated one is activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 380ns is also provided by driver IC, in order to reduce cross-conduction of the power switches.

VFO (Fault-output and NTC, Pin 14)

The VFO pin indicates a module failure in case of under voltage at pin VDD or in case of triggered over-current detection at ITRIP. A pull-up resistor is externally required.

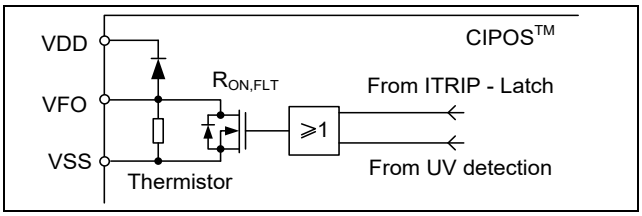


Figure 5 Internal circuit at pin VFO

The same pin provides direct access to the NTC, which is referenced to VSS. An external pull-up resistor connected to +5 V ensures that the resulting voltage can be directly connected to the microcontroller.

ITRIP (Over-current detection function, Pin 15)

CIPOS™ Mini provides an over-current detection function by connecting the ITRIP input with the

MOSFET drain current feedback. The ITRIP comparator threshold (typ. 0.47 V) is referenced to VSS ground. An input noise filter (typ.: $t_{ITRIPMIN}$ = 530 ns) prevents the driver to detect false over-current events.

Over-current detection generates a shutdown of all outputs of the gate driver after the shutdown propagation delay of typically 1000 ns.

The fault-clear time is set to minimum 40 µs.

VDD, VSS (Low-side control supply and reference, Pin 13, 16)

VDD is the control supply and it provides power both to input logic and to output power stage. Input logic is referenced to VSS ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 12.1 V is present.

The IC shuts down all the gate drivers power outputs, when the VDD supply voltage is below V_{DDUV-} = 10.4 V. This prevents the power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB(U, V) and VS(U, V) (High-side supplies, Pin 1 - 4)

VB to VS is the high-side supply voltage. The high-side circuit can float with respect to VSS following the high-side power device source voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 12.1 V and a falling threshold of V_{BSUV-} = 10.4 V.

VS(U, V) provide a high robustness against negative voltage in respect of VSS of -50 V transiently. This ensures very stable designs even under rough conditions.

NV, NU (Low-side source, Pin 18 and 19)

The low-side sources are available for current measurements of each phase leg. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

V, U (High-side source and low-side drain, Pin 21 and 22)

These pins are connected to U, V input of a motor.

P (Positive bus input voltage, Pin 23)

The high-side MOSFETs are connected to the bus voltage. It is noted that the bus voltage does not exceed 450V.

3 Absolute Maximum Ratings

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

3.1 Module Section

Description	Symbol	Condition	Value	Unit
Storage temperature range	T_{STG}		-40 ~ 125	°C
Operating case temperature	T_C	Refer to Figure 7	-40 ~ 125	°C
Operating junction temperature	T_J		-40 ~ 150	°C
Isolation test voltage	V_{ISO}	1min, RMS, f = 60 Hz	2000	V

3.2 Inverter Section

Description	Symbol	Condition	Value	Unit
Max. blocking voltage	V_{DSS}	I_D = 250 µA	650	V
DC link supply voltage of P-N	V_{PN}	Applied between P-N	450	V
DC link supply voltage (surge) of P-N	$V_{PN(surge)}$	Applied between P-N	500	V
Output current	I_O	T_C = 25°C, T_J < 150°C	±10	A
Peak output current	$I_{O(peak)}$	less than 1 ms	±12	A
Power dissipation per MOSFET	P_{tot}		29.7	W
Short circuit withstand time[1]	t_{SC}	V_{DC} ≤ 400 V, T_J = 150°C	5	µs

3.3 Control Section

Description	Symbol	Condition	Value	Unit
High-side offset voltage	V_S		600	V
Repetitive peak reverse voltage of bootstrap diode	V_{RRM}		600	V
Module supply voltage	V_{DD}		20	V
High-side floating supply voltage (V_B reference to V_S)	V_{BS}		20	V
Input voltage	V_{IN}	LIN, HIN, ITRIP	10	V

[1] Allowed number of short circuits: <1000; time between short circuits: >1s.

4 Thermal Characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Single MOSFET thermal resistance, junction-case	R_{thJC}				4.21	K/W

5 Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

Description	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P-N	V_{PN}	0	-	450	V
Low-side supply voltage	V_{DD}	14.0	15	18.5	V
High-side floating supply voltage (V_B vs. V_S)	V_{BS}	13.5	-	18.5	V
Logic input voltages LIN, HIN, ITRIP	V_{IN}	0	-	5	V
PWM carrier frequency	f_{PWM}	-	-	20	kHz
External deadtime between HIN and LIN	DT	1.5	-	-	µs
Voltage between VSS - N (including surge)	V_{COMP}	-5	-	5	V
Minimum input pulse width	$PW_{IN(ON)}$ $PW_{IN(OFF)}$	1.2	-	-	µs
Control supply variation	$\Delta V_{BS,}$ ΔV_{DD}	-1 -1	- -	1 1	V/µs

6 Static Parameters

(V_{DD} = 15V and T_J = 25°C, if not stated otherwise)

6.1 Inverter Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Drain-Source on-state resistance	$R_{DS(on)}$	I_D = 4.4 A T_J = 25°C 150°C	 - -	 0.28 0.73	 0.33 -	Ω
Drain-Source leakage current	I_{DSS}	V_{DS} = 600 V	-	-	1	mA
Diode forward voltage	V_F	I_F = 4.4 A T_J = 25°C	-	0.9	-	V

6.2 Control Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Logic "1" input voltage (LIN, HIN)	V_{IH}		-	2.1	2.5	V
Logic "0" input voltage (LIN, HIN)	V_{IL}		0.7	0.9	-	V
ITRIP positive going threshold	$V_{IT,TH+}$		400	470	540	mV
ITRIP input hysteresis	$V_{IT,HYS}$		-	70	-	mV
VDD and VBS supply under voltage positive going threshold	V_{DDUV+} V_{BSUV+}		10.8	12.1	13.0	V
VDD and VBS supply under voltage negative going threshold	V_{DDUV-} V_{BSUV-}		9.5	10.4	11.2	V
VDD and VBS supply under voltage lockout hysteresis	V_{DDUVH} V_{BSUVH}		1.0	1.7	-	V
Quiescent VB_x supply current (V_{Bx} only)	I_{QBS}	H_{IN} = 0 V	-	-	500	µA
Quiescent VDD supply current (V_{DD} only)	I_{QDD}	L_{IN} = 0 V, H_{INX} = 5 V	-	-	900	µA
Input bias current for LIN, HIN	I_{IN+}	V_{IN} = 5 V	-	1	1.5	mA
Input bias current for ITRIP	I_{ITRIP+}	V_{ITRIP} = 5 V	-	65	150	µA
Input bias current for VFO	I_{FO}	VFO = 5 V, V_{ITRIP} = 0 V	-	60	-	µA
VFO output voltage	V_{FO}	I_{FO} = 10 mA, V_{ITRIP} = 1 V	-	0.5	-	V
Bootstrap diode forward voltage	V_{F_BSD}	IF = 20 mA, VS2 and VS3 = 0 V	-	2.6	-	V
Bootstrap resistance	R_{BSD}	Between V_{F1} = 4 V and V_{F2} = 5 V	-	40	-	Ω

7 Dynamic Parameters

(V_{DD} = 15V and T_J = 25°C, if not stated otherwise)

7.1 Inverter Section

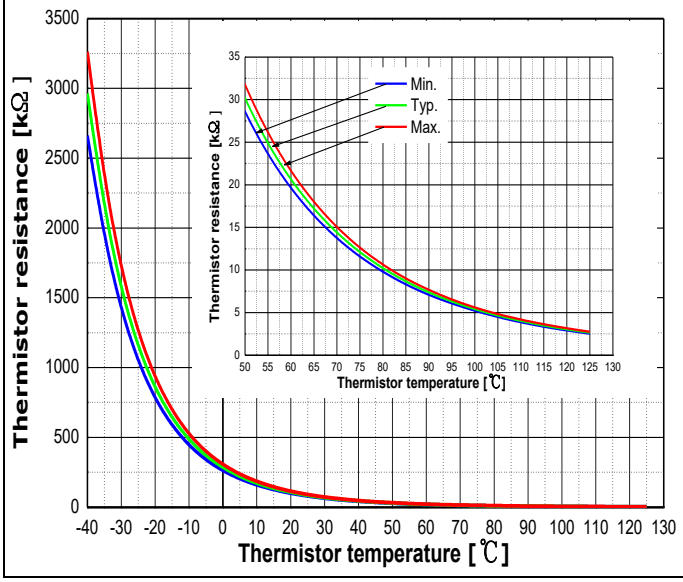
Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Turn-on propagation delay time	t_{on}	$V_{LIN, HIN}$ = 5 V, I_D = 6 A, V_{DC} = 300 V	-	875	-	ns
Turn-on rise time	t_r		-	85	-	ns
Turn-on switching time	$t_{c(on)}$		-	200	-	ns
Reverse recovery time	t_{rr}		-	115	-	ns
Turn-off propagation delay time	t_{off}	$V_{LIN, HIN}$ = 0 V, I_D = 6 A, V_{DC} = 300 V	-	810	-	ns
Turn-off fall time	t_f		-	10	-	ns
Turn-off switching time	$t_{c(off)}$		-	20	-	ns
Short circuit propagation delay time	t_{SCP}	From $V_{IT,TH+}$ to 10% I_{SC}	-	1300	-	ns
MOSFET turn-on energy (includes reverse recovery of diode)	E_{on}	V_{DC} = 300 V, I_D = 6 A T_J = 25°C 150°C	- -	360 660	- -	µJ
MOSFET turn-off energy	E_{off}	V_{DC} = 300 V, I_D = 6 A T_J = 25°C 150°C	- -	15 25	- -	µJ
Diode recovery energy	E_{rec}	V_{DC} = 300 V, I_D = 6 A T_J = 25°C 150°C	- -	55 125	- -	µJ

Control Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Bootstrap diode reverse recovery time	t_{rr_BS}	I_F = 0.6 A, di/dt = 80 A/µs	-	50	-	ns
Input filter time ITRIP	$t_{ITRIPmin}$	V_{ITRIP} = 1 V	-	530	-	ns
Input filter time at LIN, HIN for turn on and off	t_{FILIN}	$V_{LIN, HIN}$ = 0 V & 5 V	-	290	-	ns
Fault clear time after ITRIP-fault	t_{FLTCLR}	V_{ITRIP} = 1 V	40	65	200	µs
ITRIP to Fault propagation delay	t_{FLT}	$V_{LIN, HIN}$ = 0 or $V_{LIN, HIN}$ = 5 V, V_{ITRIP} = 1 V	-	730	1000	ns
Internal deadtime	DT_{IC}		-	380	-	ns
Matching propagation delay time (On and Off) all channels	M_T	External dead time >500 ns	-	20	100	ns

8 Thermistor

Description	Condition	Symbol	Value			Unit
			Min.	Typ.	Max.	
Resistance	T_{NTC} = 25°C	R_{NTC}	-	85	-	kΩ
B-constant of NTC (Negative Temperature Coefficient)		B(25/100)	-	4092	-	K



T [°C]	Rmin. [kΩ]	Rtyp. [kΩ]	Rmax. [kΩ]
50	28.400	29.972	31.545
60	19.517	20.515	21.514
70	13.670	14.315	14.960
80	9.745	10.169	10.593
90	7.062	7.345	7.628
100	5.199	5.388	5.576
110	3.856	4.009	4.163
120	2.900	3.024	3.149
125	2.527	2.639	2.751

Figure 6 Thermistor resistance – temperature curve and table
(For more information, please refer to the application note 'AN2016-10 CIPOS Mini Technical description')

9 Mechanical Characteristics and Ratings

Description	Condition	Value			Unit
		Min.	Typ.	Max.	
Comparative Tracking Index (CTI)		550	-	-	V
Mounting torque	M3 screw and washer	0.59	0.69	0.78	Nm
Backside Curvature	Refer to Figure 8	-50	-	100	µm
Weight		-	6.12	-	g

10 Qualification Information

UL Certification	File number: E314539	
Moisture sensitivity level (SOP23 only)	-	
RoHS Compliant	Yes (Lead-free terminal plating)	
ESD	HBM(Human Body Model)	Class 2
	CDM(Charged Device Model)	Class C3

11 Diagrams and Tables

11.1 T_C Measurement Point

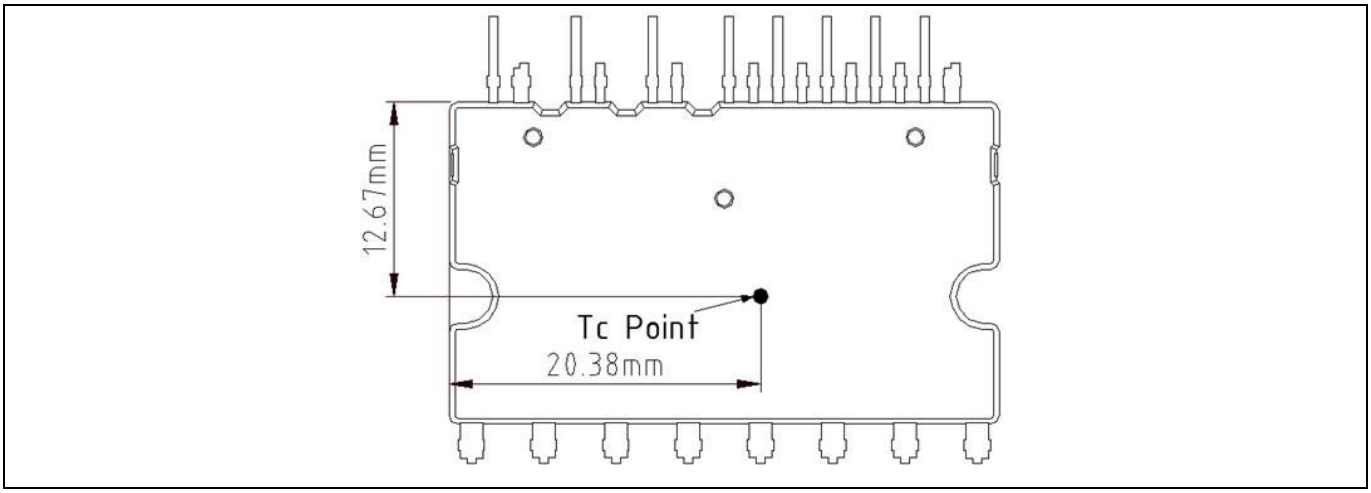


Figure 7 T_C measurement point[1]

11.2 Backside Curvature Measurment Point

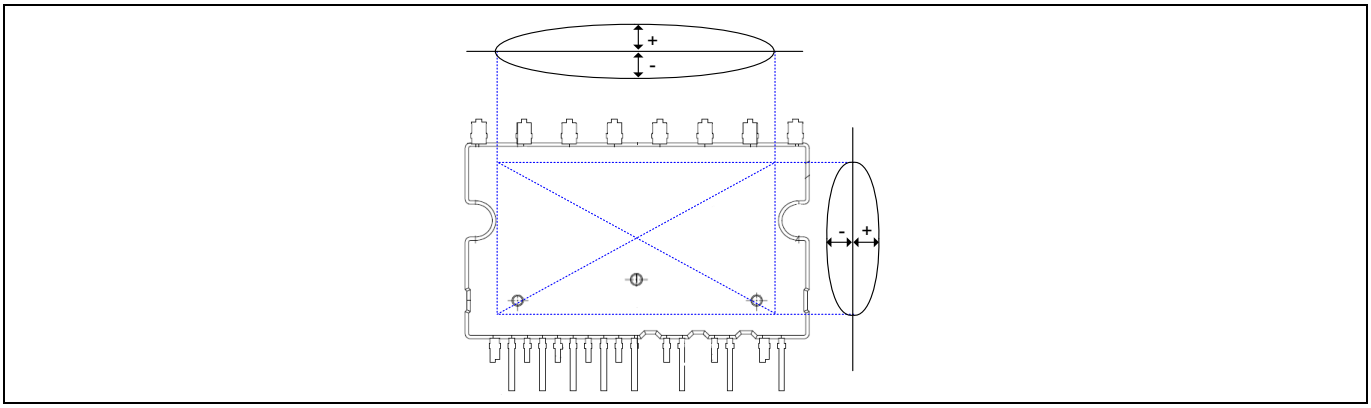
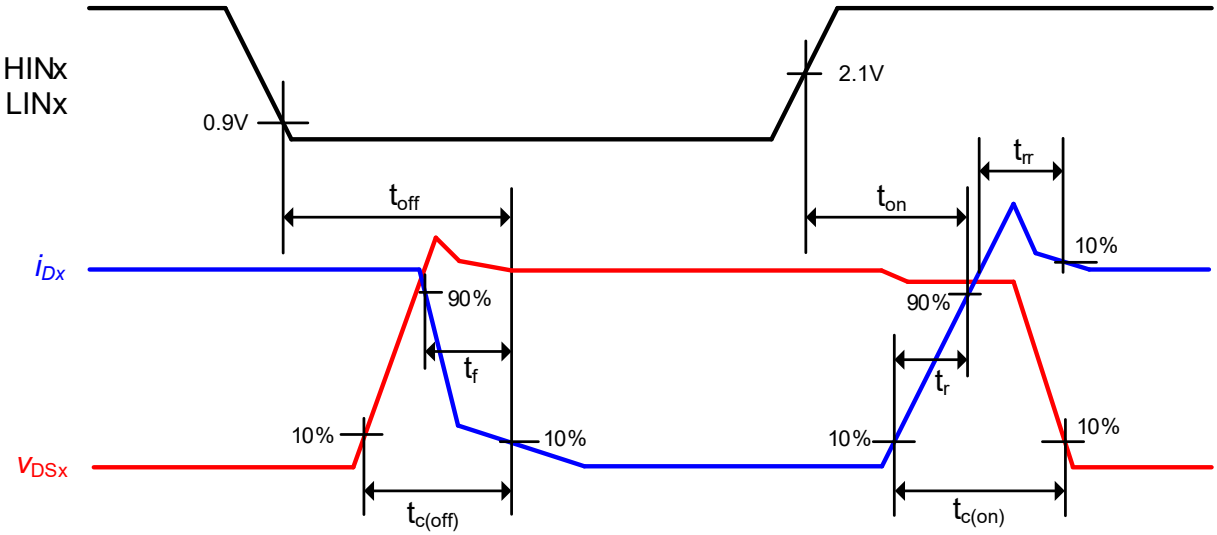


Figure 8 Backside curvature measurement position

[1]Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.

11.3 Switching Time Definition



12 Application Guide

12.1 Typical Application Schematic

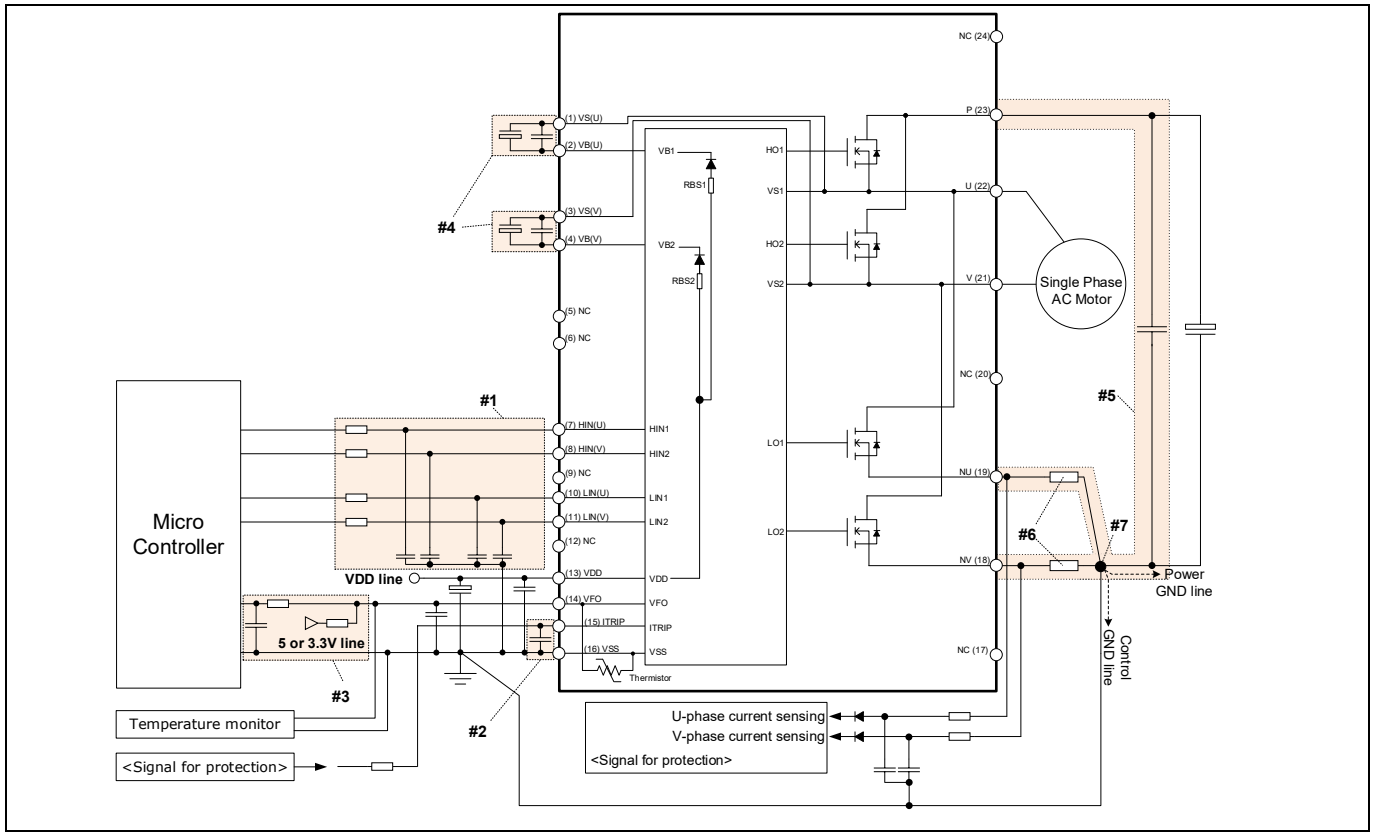


Figure 9 Typical application circuit

- #1 Input circuit
  - RC filter can be used to reduce input signal noise. (100 Ω, 1 nF)
  - The capacitors should be located close to the IPM (to V_{SS} terminal especially).
- #2 Itrip circuit
  - To prevent a mis operation of protection function, RC filter is recommended.
  - The capacitor should be located close to Itrip and VSS terminals.
- #3 VFO circuit
  - VFO pin is open drain configuration. This terminal should be pulled up to the bias voltage of the 5 V/3.3 V through a proper resistor.
  - It is recommended that RC filter is placed close to the controller.
- #4 VB-VS circuit
  - Capacitors for high-side floating supply voltage should be placed close to VB and VS terminals.
- #5 Snubber capacitor
  - The wiring among CIPOS™ Mini, snubber capacitor and shunt resistors should be short as possible.
- #6 Shunt resistor
  - SMD type shunt resistors are strongly recommended to minimize its internal stray inductance.
- #7 Ground pattern
  - Pattern overlap of power ground and signal ground should be minimized. The patterns should be connected at one end of shunt resistor only for the same potential.

12.2 Performance Chart

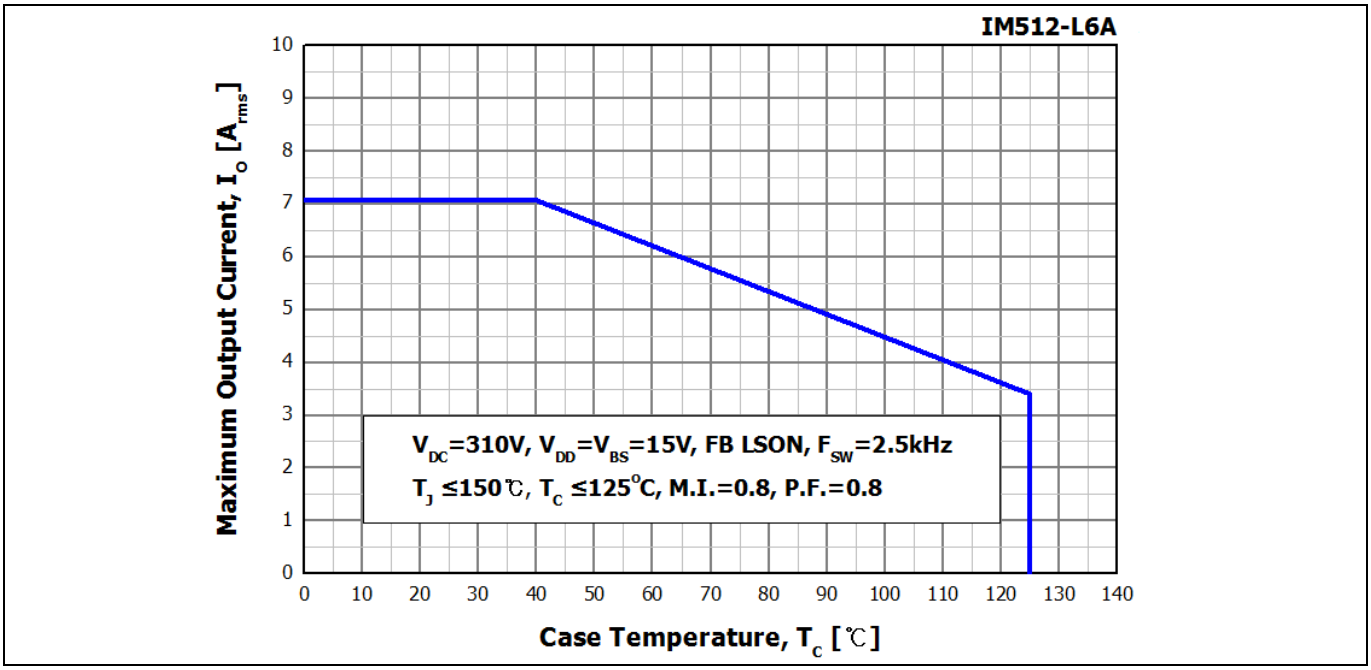
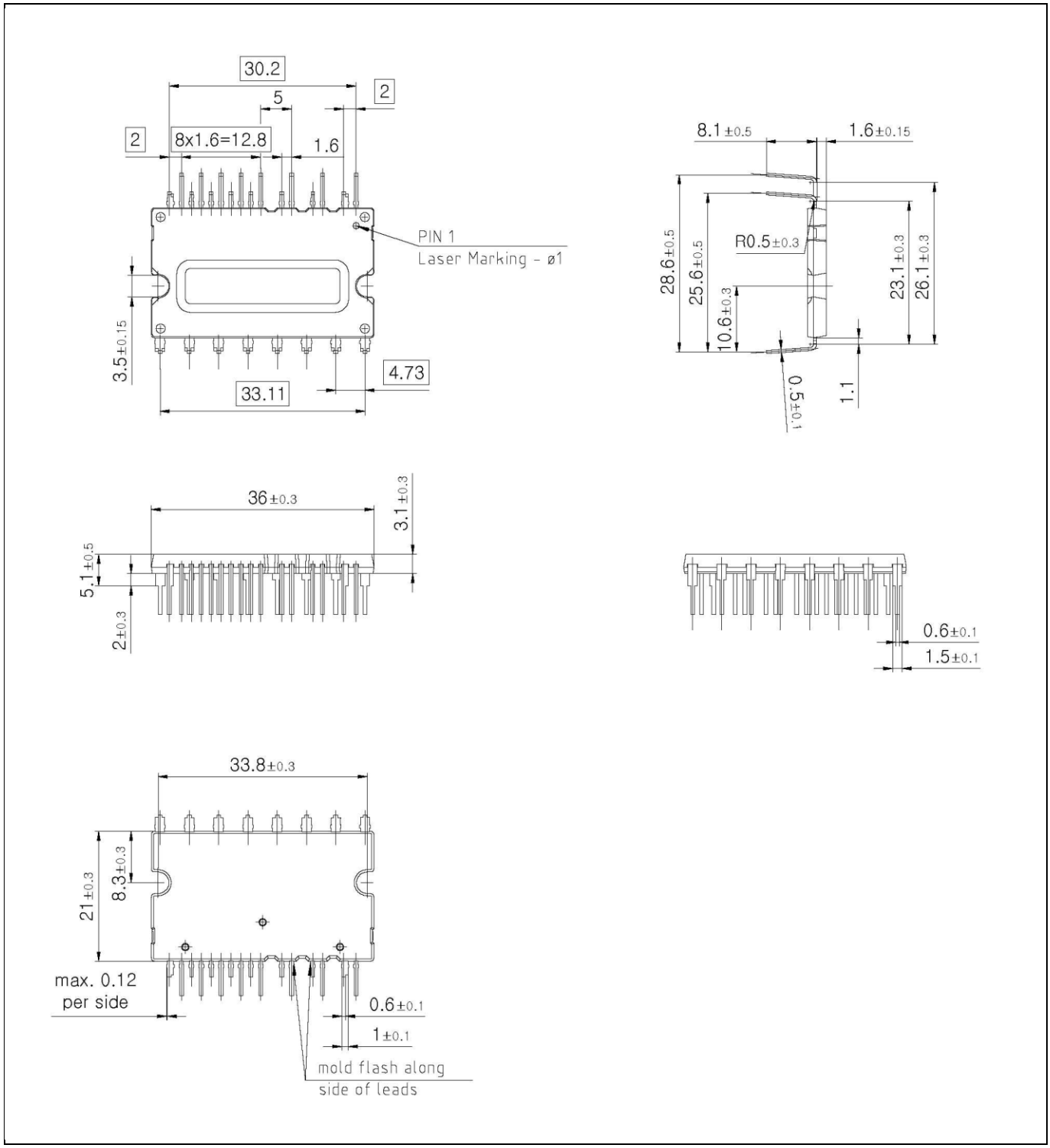


Figure 10 Maximum operating current SOA[1]

[1]This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

13 Package Outline



Revision history

Document version	Date of release	Description of changes
V 2.0	2017-12-07	Initial release
V 2.1	2020-04-24	Updated Table 1, Figure 1, and Figure 9

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