PIC18F25/45/55Q43

PIC18F25/45/55Q43 Silicon Errata and Data Sheet Clarifications

The PIC18F25/45/55Q43 devices you have received conform functionally to the current device data sheet (DS40002170E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F25/45/55Q43 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID			
		B0	B2	B3	D2
PIC18F25Q43	0x73C0	0xA040	0xA042	0xA043	0xA0C2
PIC18F45Q43	0x73E0	0xA040	0xA042	0xA043	0xA0C2
PIC18F55Q43	0x7400	0xA040	0xA042	0xA043	0xA0C2

> **Important:** Refer to the **Device/Revision ID** section in the current **"PIC18FXXQ43 Family Programming Specification"** (DS40002079) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions			
				B0	B2	B3	D2
ADCC	Capacitive Voltage Divider	1.1.1	CVD is only functional on PORTA[2:0] and PORTB[4:0]	X			
Oscillator	XT mode	1.2.1	Maximum clock frequency limited to 2 MHz for XT mode	X	X		
I2C	I2C	1.3.1	I2CxADR0/1/2/3 registers have incorrect Reset value	X	X	X	
I2C	I2C	1.3.2	I2C Start and/or Stop flags may be set when I2C is enabled	X	X	X	X
SRAM	SRAM read-back	1.4.1	SRAM read-back can be incorrect	X			
In-Circuit Debug	Software breakpoints	1.5.1	Software breakpoints are not available	X	X	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

> **CAUTION**
>
> **Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

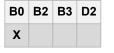## 1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 Capacitive Voltage Divider (CVD)

The CVD feature is only functional on PORTA[2:0] and PORTB[4:0]. This feature is not recommended for use on any other pins.

Work around
None.

Affected Silicon Revisions

B0	B2	B3	D2
X			

1.2 Module: Oscillator

1.2.1 Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around
For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

B0	B2	B3	D2
X	X		

1.3 Module: I²C

1.3.1 I2CxADR0/1/2/3 Registers Have Incorrect Reset Value

The I2CxADR0/2 registers reset to `0xFF` when the I2CxMD is enabled instead of `0x00`. The I2CxADR1/3 registers reset to `0xFE` when the I2CxMD is enabled instead of `0x00`.

Work around
None.

Affected Silicon Revisions

B0	B2	B3	D2
X	X	X	

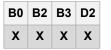### 1.3.2   I²C Start and/or Stop Flags May be Set When I²C is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts if enabled.

Work around

1. Disable the Start and Stop conditions interrupt functions
2. Enable the I²C module
3. Wait 250 nS + six instructions cycles (F_{OSC}/4)
4. Clear the Start and Stop conditions interrupt flags
5. Enable the Start and Stop conditions interrupt functions if used

```
I2CxPIEbits.SCIE = 0;        // Disable Start conditoin interrupt
I2CxPIEbits.PCIE = 0;        // Disable Stop condition interrupt
I2CxCON0bits.EN = 1;         // Enable I2C
Delay();                     // Wait for 250nS + 6 instruction cycles (FOSC/4)
I2CxPIRbits.SCIF = 0;        // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0;        // Clear the Stop condition interrupt flags
I2CxPIEbits.SCIE = 1;        // Enable Start condition interrupt if used
I2CxPIEbits.PCIE = 1;        // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

B0	B2	B3	D2
X	X	X	X

1.4   Module: SRAM

1.4.1   SRAM Read-Back

Following a device power-up sequence, there is a possibility that some SRAM locations will not return the expected written value but will read back '00' instead.
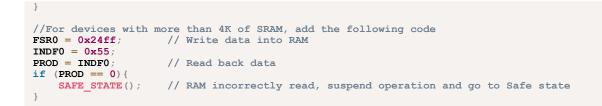
Work around

None. The device can only recover by power cycling.

This erroneous condition can be detected by running the following code that writes non-zero values to SRAM and then verifies that the returned read values are not '00'. If a returned value is '00', the application code has to be put into a safe state until a POR event occurs. This code has to be executed immediately after power-up. If the test passes, the device operation will be normal.

```
// SRAM test

FSR0 = 0xcff;        // Write data into RAM address for devices up to 2K RAM
INDF0 = 0x55;
PROD = INDF0;        // Read back data
if (PROD == 0){
    SAFE_STATE();    // RAM incorrectly read, suspend operation and go to Safe state
}

//For devices with more than 2K of SRAM, add the following code
FSR0 = 0x14ff;       // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;        // Read back data
if (PROD == 0){
    SAFE_STATE();    // RAM incorrectly read, suspend operation and go to Safe state
```

```
}

//For devices with more than 4K of SRAM, add the following code
FSR0 = 0x24ff;         // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;          // Read back data
if (PROD == 0){
    SAFE_STATE();      // RAM incorrectly read, suspend operation and go to Safe state
}
```

Affected Silicon Revisions

B0	B2	B3	D2
X			

1.5   Module: In-Circuit Debug

1.5.1   Software Breakpoints Are Not Available

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

B0	B2	B3	D2
X	X	X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002170E):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
K	07/2021	Added silicon erratum item 1.3.2
J	03/2021	Added silicon erratum item 1.5.1
H	12/2020	Added silicon revision D2; Deleted clarification 2.1.
G	10/2020	Added silicon revision B3 and UART Transmit Collision Interrupt data sheet clarification; Updated silicon erratum item 1.3.1.
F	08/2020	Added silicon revision B2
E	06/2020	Added silicon erratum item 1.4.1
D	06/2020	Added silicon erratum item 1.3.1
C	04/2020	Added XT mode erratum and Temperature Indicator data sheet clarification
B	02/2020	Added working pins for CVD
A	12/2019	Initial document release

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