UCS2113

USB Dual-Port Power Switch and Current Monitor

Features

- Dual-Port Power Switches:
  - 2.9V to 5.5V source voltage range
  - 3.0A continuous current per V_{BUS} port with 40 mΩ On resistance per switch
  - Independent port power switch enable pins
  - DUAL fault ALERT# active drain output pins
  - Constant Current or Trip mode current limiting behaviors
  - Undervoltage and overvoltage lockout
  - Back-drive, back-voltage protection
  - Auto-recovery fault handling with low test current
  - BOOST# logic output to increase DC-DC converter output under large load conditions
- SMBus 2.0/I^2C Mode Features:
  - Eight programmable current limits assignable to each power switch
  - Other SMBus addresses available upon request
  - Block read and block write
- Self-Contained Current Monitoring (No External Sense Resistor Required)
- Fully Programmable Per-Port Charge Rationing and Behaviors
- Configurable Per-Port BC1.2 V_{BUS} Discharge Function
- Wide Operating Temperature Range:
  - -40°C to +105°C
- UL Recognized and EN/IEC 60950-1 (CB) Certified

Description

The UCS2113 is a dual USB port power switch configuration which can provide 3.0A continuous current (3.4A maximum) per V_{BUS} port with precision overcurrent limiting (OCL), port power switch enables, auto-recovery fault handling, undervoltage and overvoltage lockout, back-drive protection and back-voltage protection, and thermal protection.

The UCS2113 is well suited for both stand-alone and applications having SMBus/I^2C communications.

For applications with SMBus, the UCS2113 provides per-port current monitoring and eight programmable current limits per switch, ranging from 0.53A to 3.0A continuous current (3.4A maximum). Per-port charge rationing is also provided ranging from 3.8 mAh to 246.3 Ah.

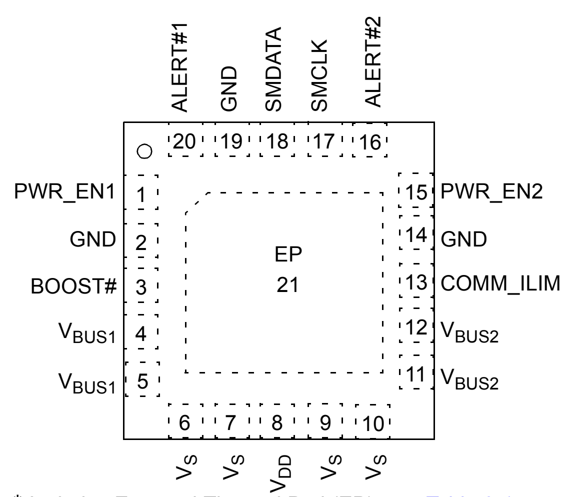
In stand-alone mode, the UCS2113 provides eight current limits for both switches, ranging from 0.53A + 0.53A to 3A + 3A total continuous current (see Table 1-1).

Both power switches include an independent V_{BUS} discharge function and constant current mode current limiting for BC1.2 applications.

The UCS2113 is available in a 4x4 mm 20-pin QFN package.

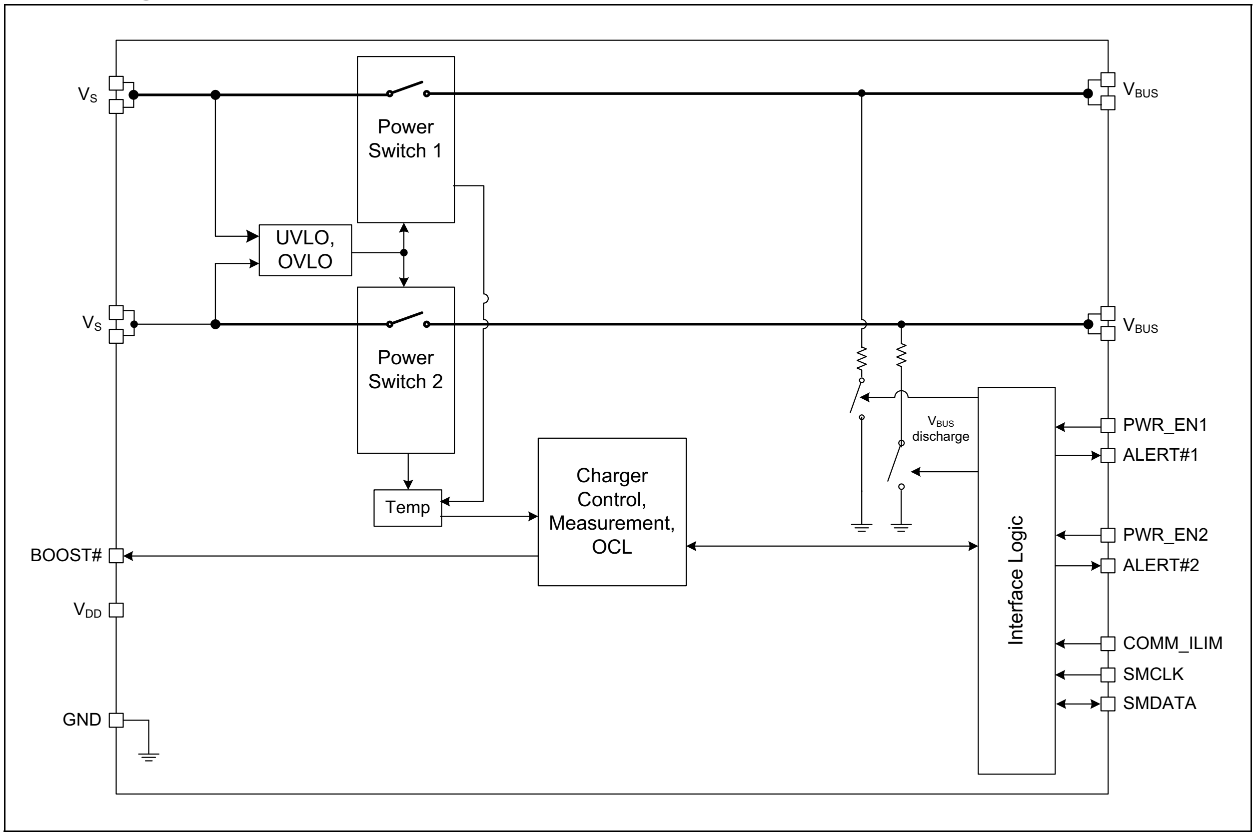
Package Type

UCS2113
4 x 4 QFN*



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD}, V_S, and V_{BUS} pins .... -0.3 to 6V
Pull-Up Voltage (V_{PULLUP}) .... -0.3 to V_{DD} + 0.3
Port Power Switch Current .... Internally limited
Voltage on any Other Pin to Ground .... -0.3 to V_{DD} + 0.3V
Current on any Other Pin .... ±10 mA
Package Power Dissipation .... See Table 1-1
Operating Ambient Temperature Range .... -40°C to +105°C
Storage Temperature Range .... -55°C to +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: POWER DISSIPATION SUMMARY

Board	Package	θ_{JC}	θ_{JA}	Derating Factor Above +25°C	T_A < +25°C Power Rating	T_A = +70°C Power Rating	T_A = +85°C Power Rating
High K (Note)	**20-pin QFN 4x4 mm**	6 °C/W	41 °C/W	24.4 mW/°C	2193 mW	1095 mW	729 mW
Low K (Note)	**20-pin QFN 4x4 mm**	6 °C/W	60 °C/W	16.67 mW/°C	1498 mW	748 mW	498 mW

Note: A High-K board uses a thermal via design with the thermal landing soldered to the PCB ground plane with 0.3 mm (12 mil) diameter vias in a 3x3 matrix (9 total) at 0.5 mm (20 mil) pitch. The board is multilayer with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom. A Low-K board is a two-layer board without thermal via design with 2-ounce copper traces on the top and bottom.

TABLE 1-2: ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 105°C. All typical values at V_{DD} = V_S = 5V, T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power and Interrupts - DC						
Supply Voltage	V_{DD}	4.5	5	5.5	V	
Supply Current in Active ($I_{DD\_ACT} + I_{S1\_ACT} + I_{S2\_ACT}$)	I_{ACTIVE}	—	700	—	µA	Average current I_{BUS} = 0 mA
Supply Current in Sleep ($I_{DD\_SLEEP} + I_{S1\_SLEEP} + I_{S2\_SLEEP}$)	I_{SLEEP}	—	6	20	µA	Average current $V_{PULLUP} \leq V_{DD}$
Power-On Reset						
V_{DD} Low Threshold	V_{DD_TH}	—	4	4.3	V	V_{DD} voltage increasing (Note 1)
V_{DD} Low Hysteresis	$V_{DD\_TH\_HYST}$	—	500	600	mV	V_{DD} voltage decreasing (Note 1)

Note 1: This parameter is characterized, not 100% tested.
2: This parameter is ensured by design and not 100% tested.
3: The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \leq 1.6A$).

TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 105°C. All typical values at V_{DD} = V_S = 5V, T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
I/O Pins - SMCLK, SMDATA, PWR_EN, ALERT#, BOOST# - DC Parameters						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{SINK_IO} = 8 mA SMDATA, ALERT#, BOOST#
Input High Voltage	V_{IH}	2.0	—	—	V	PWR_EN, SMDATA, SMCLK
Input Low Voltage	V_{IL}	—	—	0.8	V	PWR_EN, SMDATA, SMCLK
Leakage Current	I_{LEAK}	—	—	±5	µA	Powered or unpowered $V_{PULLUP} \leq V_{DD}$ T_A < 85°C (**Note 1**)
Interrupt Pins - AC Parameters						
ALERT# Pin Blanking Time	t_{BLANK}	—	25	—	ms	Blanking time, coming out of reset
ALERT# Pin Interrupt Masking Time	t_{MASK}	—	5	—	ms	
BOOST# Pin Minimum Assertion Time	t_{BOOST_MAT}	—	1	—	s	
BOOST# Pin Assertion Current	I_{BOOST}	—	1.9	—	A	
SMBus/I²C Timing						
Input Capacitance	C_{IN}	—	5	—	pF	
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}	—	—	50	ns	
Bus Free Time Stop to Start	t_{BUF}	1.3	—	—	µs	
Start Setup Time	$t_{SU:STA}$	0.6	—	—	µs	
Start Hold Time	$t_{HD:STA}$	0.6	—	—	µs	
Stop Setup Time	$t_{SU:STO}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6	—	—	µs	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Min. = 20+0.1C_{LOAD} ns (Note 1)
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Min. = 20+0.1C_{LOAD} ns (Note 1)
Capacitive Load	C_{LOAD}	—	—	400	pF	Per bus line (Note 1)
Timeout	$t_{TIMEOUT}$	25	—	35	ms	Disabled by default (Note 1)
Idle Reset	t_{IDLE_RESET}	350	—	—	µs	Disabled by default (Note 1)

Note 1: This parameter is characterized, not 100% tested.

2: This parameter is ensured by design and not 100% tested.

3: The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \leq$ 1.6A).

TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 105°C. All typical values at V_{DD} = V_S = 5V, T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Port Power Switch						
Port Power Switch - DC Parameter						
Overvoltage Lockout	V_{S_OV}	—	6	—	V	Note 2
V_S Low Threshold	V_{S_UVLO}	—	2.5	—	V	Note 2
V_S Low Hysteresis	$V_{S\_UVLO\_HYST}$	—	100	—	mV	Note 2
On Resistance	R_{ON_PSW}	—	40	—	mΩ	4.75V < V_S < 5.25V
V_S Leakage Current	I_{LEAK_VS}	—	—	5	µA	Sleep state into V_S pin on one channel (Note 1)
Back-Voltage Protection Threshold	V_{BV_TH}	—	150	—	mV	V_{BUS} > V_S V_S > V_{S_UVLO}
Leakage Current	I_{LKG_1}	—	0	3	µA	V_{DD} < V_{DD_TH}, Leakage current from V_{BUS} pins to the V_{DD} and the V_S pins (Note 1)
	I_{LKG_2}	—	0	2	µA	V_{DD} > V_{DD_TH}, Leakage current from V_{BUS} pins to the V_S pins, when the power switch is open
Selectable Current Limits	I_{LIM1}	—	530	—	mA	I_{LIM} Resistor = 0 or 47 kΩ (530 mA setting)
	I_{LIM2}	—	960	—	mA	I_{LIM} Resistor = 10 kΩ or 56 kΩ (960 mA setting)
	I_{LIM3}	—	1070	—	mA	I_{LIM} Resistor = 12 kΩ or 68 kΩ (1070 mA setting)
	I_{LIM4}	—	1280	—	mA	I_{LIM} Resistor = 15 kΩ or 82 kΩ (1280 mA setting)
	I_{LIM5}	—	1600	—	mA	I_{LIM} Resistor = 18 kΩ or 100 kΩ (1600 mA setting)
	I_{LIM6}	—	2130	—	mA	I_{LIM} Resistor = 22 kΩ or 120 kΩ (2130 mA setting)
	I_{LIM7}	2500	2670	2900	mA	I_{LIM} Resistor = 27 kΩ or 150 kΩ (2670 mA setting)
	I_{LIM8}	3000	3200	3400	mA	I_{LIM} Resistor = 33 kΩ or V_{DD} (3200 mA setting)
Pin Wake Time	t_{PIN_WAKE}	—	3	—	ms	
SMBus Wake Time	t_{SMB_WAKE}	—	4	—	ms	
Idle Sleep Time	t_{IDLE_SLEEP}	—	200	—	ms	
First Thermal Shutdown Stage Threshold	T_{TSD_LOW}	—	120	—	°C	Die Temperature at which the power switch will open if it is in constant current mode
First Thermal Shutdown Stage Hysteresis	$T_{TSD\_LOW\_HYST}$	—	10	—	°C	Hysteresis for T_{TSD_LOW} functionality. Temperature must drop by this value before any of the power switches can be closed.

Note 1: This parameter is characterized, not 100% tested.

2: This parameter is ensured by design and not 100% tested.

3: The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \le I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \le$ 1.6A).

TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 105°C. All typical values at V_{DD} = V_S = 5V, T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Second Thermal Shutdown Stage Threshold	T_{TSD_HIGH}	—	135	—	°C	Die Temperature at which both power switches will open
Second Thermal Shutdown Stage Hysteresis	$T_{TSD\_HIGH\_HYST}$	—	25	—	°C	Hysteresis for T_{TSD_HIGH} functionality. Temperature must drop by this value before any of the power switches can be closed.
Auto-Recovery Test Current	I_{TEST}	—	190	—	mA	Portable device attached, V_{BUS}= 0 V, Die temp < T_{TSD}
Auto-Recovery Test Voltage	V_{TEST}	—	750	—	mV	Portable device attached, V_{BUS} = 0 V before application, Die temp < T_{TSD} Programmable, 250 - 1000 mV, default listed
Discharge Impedance	$R_{DISCHARGE}$	—	100	—	Ω	
Port Power Switch - AC Parameters						
Turn-On Delay	t_{ON_PSW}	—	0.9	—	ms	PWR_EN active toggle to switch on time, V_{BUS} discharge not active
Turn-Off Time	$t_{OFF\_PSW\_INA}$	—	0.75	—	ms	PWR_EN inactive toggle to switch off time C_{BUS} = 120 µF
Turn-Off Time	$t_{OFF\_PSW\_ERR}$	—	1	—	ms	Over-current Error, V_{BUS} Min Error, or Discharge Error to switch off C_{BUS} = 120 µF
Turn-Off Time	$t_{OFF\_PSW\_ERR1}$	—	100	—	ns	TSD or Back-drive Error to switch off C_{BUS} = 120 µF
V_{BUS} Output Rise Time	t_{R_BUS}	—	1.1	—	ms	Measured from 10% to 90% of V_{BUS}, C_{LOAD} = 220 µF I_{LIM} = 1.0A
Soft Turn-On Rate	$\Delta I_{BUS}/\Delta_t$	—	100	—	mA/µs	
Temperature Update Time	t_{DC_TEMP}	—	200	—	ms	
Short-Circuit Response Time	t_{SHORT_LIM}	—	1.5	—	µs	Time from detection of short to current limit applied. No C_{BUS} applied
Short-Circuit Detection Time	t_{SHORT}	—	6	—	ms	Time from detection of short to port power switch disconnect and ALERT# pin assertion
Latched Mode Cycle Time	t_{UL}	—	7	—	ms	From PWR_EN edge transition from inactive to active to begin error recovery

Note 1: This parameter is characterized, not 100% tested.

2: This parameter is ensured by design and not 100% tested.

3: The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \leq 1.6A$).

TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 105°C. All typical values at V_{DD} = V_S = 5V, T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Auto-Recovery Mode Cycle Time	t_{CYCLE}	—	25	—	ms	Time delay before error condition check. Programmable 15-50 ms, default listed
Auto-Recovery Delay	t_{TST}	—	20	—	ms	Portable device attached, V_{BUS} must be $\geq V_{TEST}$ after this time. Programmable 10-25 ms, default listed
Discharge Time	$t_{DISCHARGE}$	—	200	—	ms	Amount of time discharge resistor applied. Programmable 100-400 ms, default listed
Port Power Switch Operation With Trip Mode Current Limiting						
Region 2 Current Keep-Out	$I_{BUS\_R2MIN\_1}$	—	—	0.1	A	Note 2
Minimum V_{BUS} Allowed at Output	$V_{BUS\_MIN\_1}$	2.0	—	—	V	Note 2
Port Power Switch Operation With Constant Current Limiting (Variable Slope)						
Region 2 Current Keep-Out	I_{BUS_R2MIN}	—	—	2.13	A	Note 2
Minimum V_{BUS} Allowed at Output	V_{BUS_MIN}	2.0	—	—	V	Note 2
Current Measurement - DC						
Current Measurement Range	I_{BUS_M}	0	—	3400	mA	Range (Note 2 and Note 3)
Reported Current Measurement Resolution	ΔI_{BUS_M}	—	13.3	—	mA	1 LSB
Current Measurement Accuracy		—	±2	—	%	200 mA < I_{BUS} < I_{LIM}
		—	±2	—	LSB	I_{BUS} < 200 mA
Current Measurement - AC						
Sampling Rate	—	—	1.1	—	ms	Note 2
Conversion Time Both Channels	t_{CONV}	—	2.2	—	ms	All registers updated in digital (Note 2)
Charge Rationing - DC						
Accumulated Current Measurement Accuracy	—	—	±4.5	—	%	
Charge Rationing - AC						
Current Measurement Update Time	t_{PCYCLE}	—	1	—	s	

Note 1: This parameter is characterized, not 100% tested.
2: This parameter is ensured by design and not 100% tested.
3: The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \leq$ 1.6A).

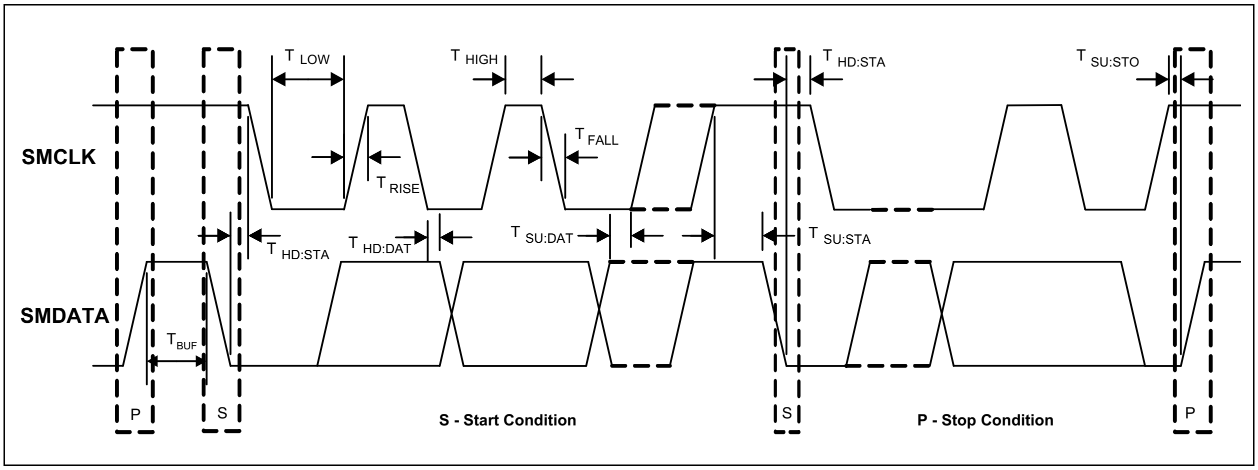


FIGURE 1-1: SMBus Timing.

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+105	°C	
Operating Junction Temperature	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	
Thermal Package Resistances - see Table 1-1						

1.1 ESD and Transient Performance

TABLE 1-4: ESD RATINGS

ESD Specification	Rating or Value
Human Body Model (JEDEC JESD22-A114) - All pins	8 kV
Charged Device Model (JEDEC JESD22-C101) - All pins	500V

1.1.1 HUMAN BODY MODEL (HBM) PERFORMANCE

HBM testing verifies the ability to withstand ESD strikes, like those that occur during handling and manufacturing, and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

1.1.2 CHARGED DEVICE MODEL (CDM) PERFORMANCE

CDM testing verifies the ability to withstand ESD strikes, like those that occur during handling and assembly, with pick-and-place-style machinery and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = V_S = 5V, T_A = +27°C.

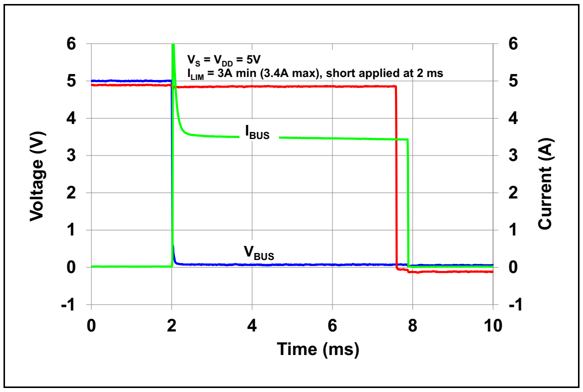


FIGURE 2-1: Short Applied After Power-Up.

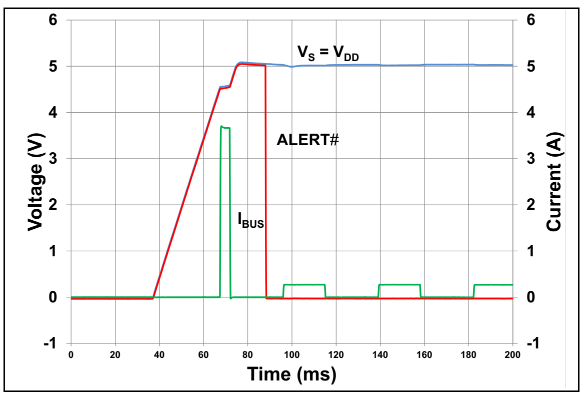


FIGURE 2-2: Power-Up Into a Short.

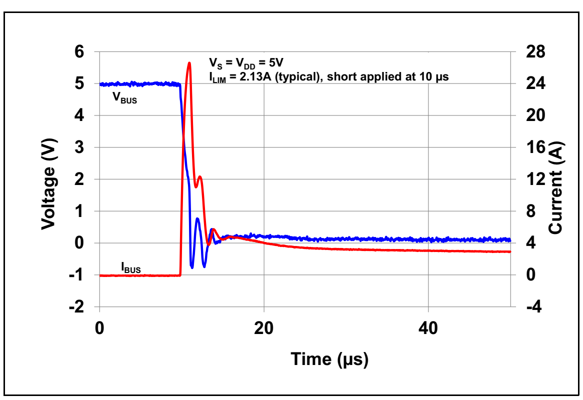


FIGURE 2-3: Internal Power Switch Short Response.

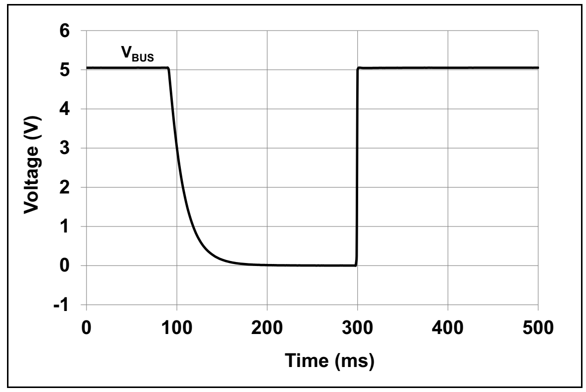


FIGURE 2-4: V_{BUS} Discharge Behavior.

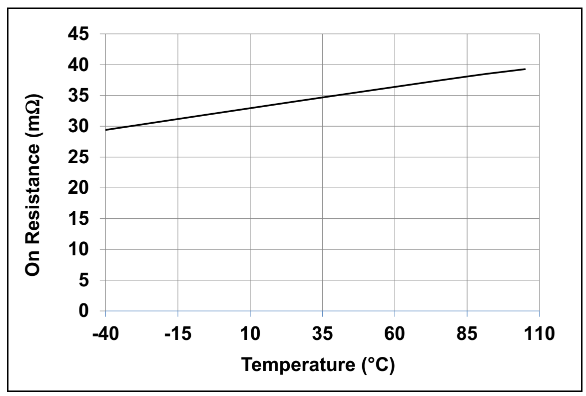


FIGURE 2-5: Power Switch On Resistance vs. Temperature.

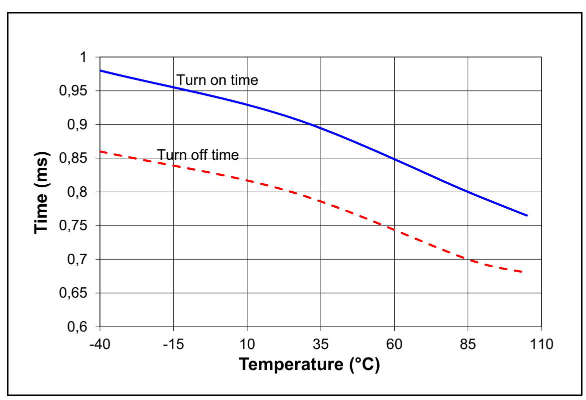


FIGURE 2-6: Power Switch On/Off Time vs. Temperature.

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_A = +27°C$.

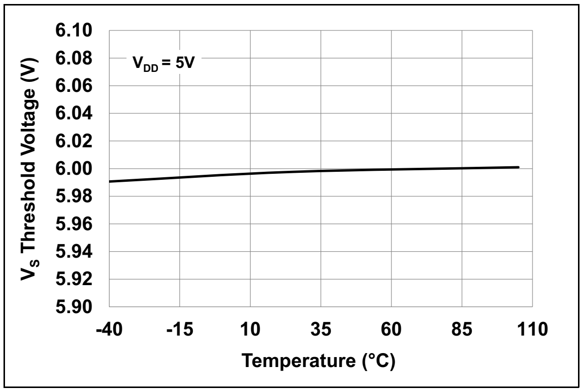


FIGURE 2-7: *V_S Overvoltage Threshold vs. Temperature.*

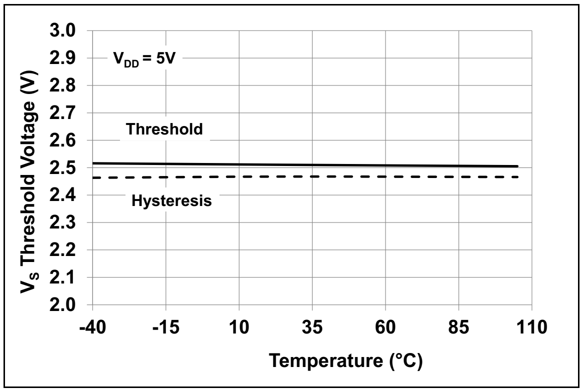


FIGURE 2-8: *V_S Undervoltage Threshold vs. Temperature.*

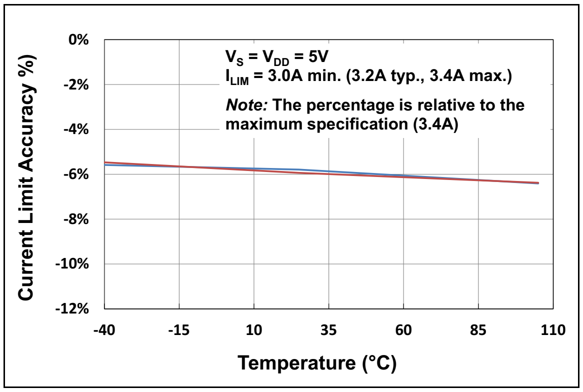


FIGURE 2-9: *Trip Current Limit Operation vs. Temperature.*

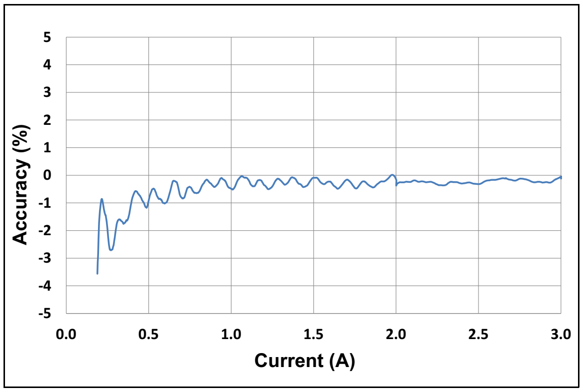


FIGURE 2-10: *I_{BUS} Measurement Accuracy.*

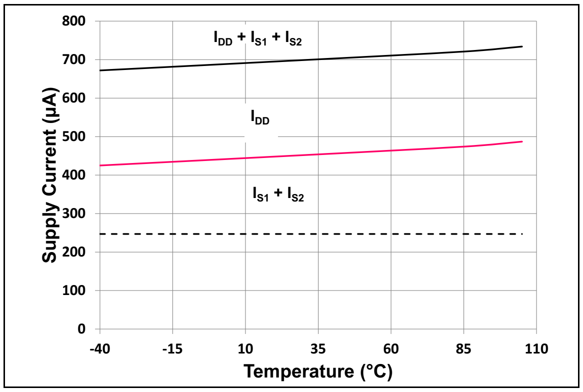


FIGURE 2-11: *Active State Current vs. Temperature (both channels on, PWR_EN1 = PWR_EN2 = 1).*

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_A = +27°C$.

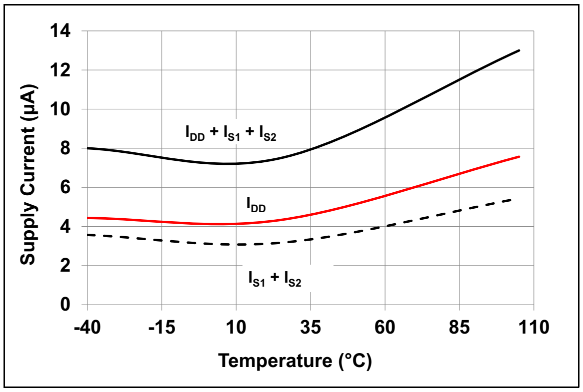


FIGURE 2-12: *Sleep State Current vs. Temperature.*

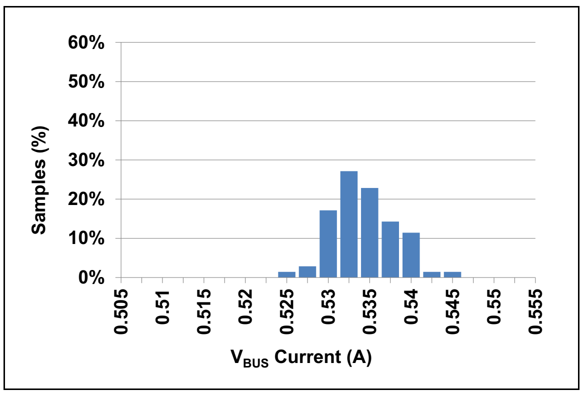


FIGURE 2-13: *ILIM1 Trip Current Distribution.*

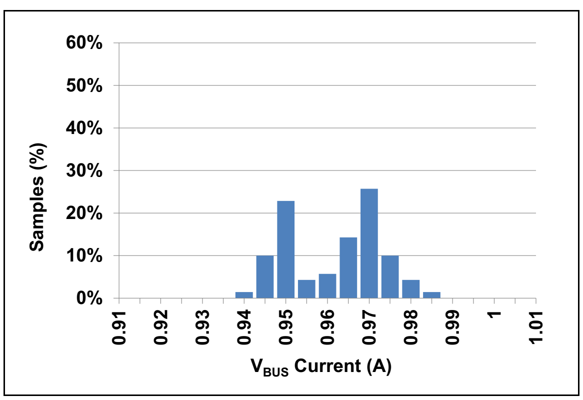


FIGURE 2-14: *ILIM2 Trip Current Distribution*[(1)]*.*

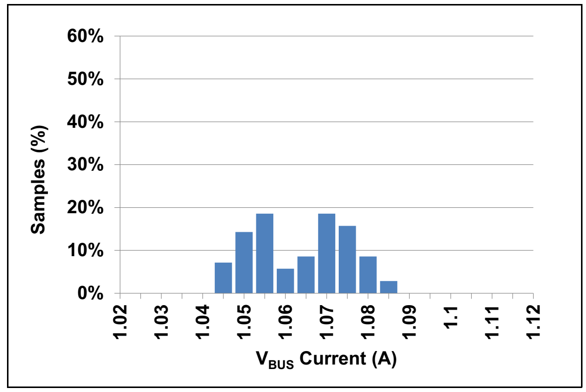


FIGURE 2-15: *ILIM3 Trip Current Distribution*[(1)]*.*

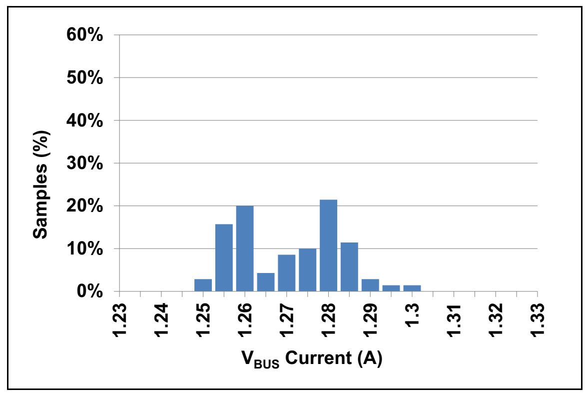


FIGURE 2-16: *ILIM4 Trip Current Distribution*[(1)]*.*

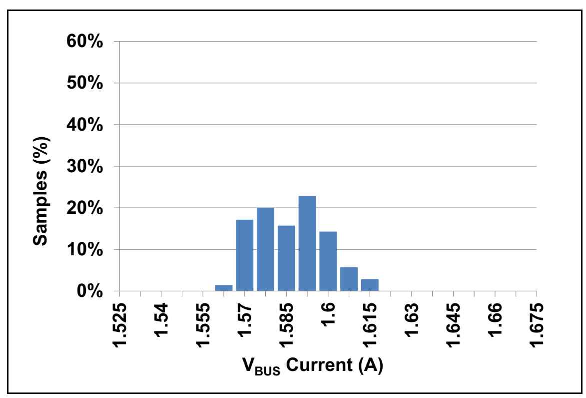


FIGURE 2-17: *ILIM5 Trip Current Distribution*[(1)]*.*

Note 1: The histogram aspect is caused by a mixture of two normal distributions, corresponding to the two V_{BUS} channels.

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_A = +27°C$.

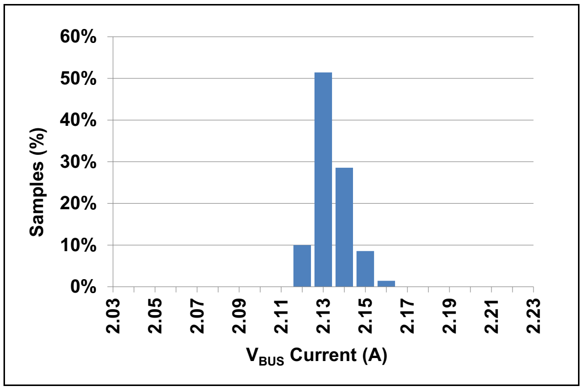


FIGURE 2-18: *ILIM6 Trip Current Distribution.*

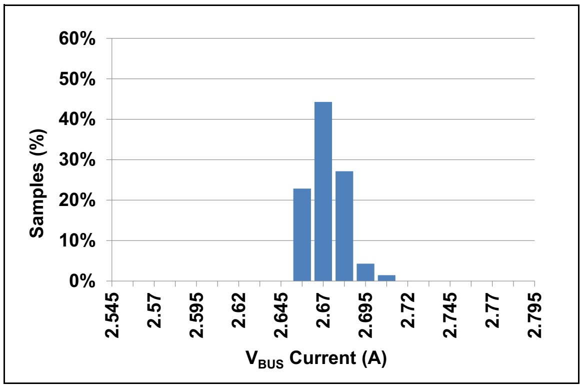


FIGURE 2-19: *ILIM7 Trip Current Distribution.*

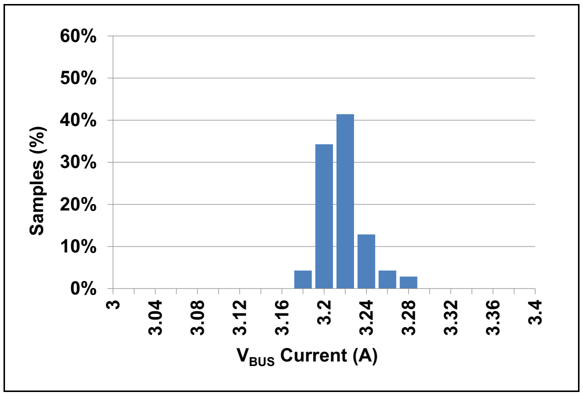


FIGURE 2-20: *ILIM8 Trip Current Distribution.*

Note 1: The histogram aspect is caused by a mixture of two normal distributions, corresponding to the two V_{BUS} channels.

3.0 PIN DESCRIPTION

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

UCS2113 4x4 QFN	Symbol	Function	Pin Type	Connection Type if Pin Not Used
1	PWR_EN1	Port power switch enable #1	DI	Connect to ground or V_{DD} (depending on the polarity decoded via COMM_ILIM pin)
2	GND	Ground	Power	N/A
3	BOOST#	Logic output for DC-DC converter voltage increase (requires pull-up resistor)	OD	Connect to ground
4, 5	V_{BUS1}	Port power switch #1 output (requires both pins tied together)	High Power, AIO	Leave open
6, 7	V_S	Voltage input to port power switch V_{BUS1} (requires both pins tied together)	High Power, AIO	Connect to ground
8	V_{DD}	Common supply voltage	Power	N/A
9, 10	V_S	Voltage input to port power switch V_{BUS2} (requires both pins tied together)	High Power, AIO	Connect to ground
11, 12	V_{BUS2}	Port power switch #2 output (requires both pins tied together)	High Power, AIO	Leave open
13	COMM_ILIM	Enables SMBus or Stand-Alone mode at power-up. Hardware strap for maximum current limit.	AIO	N/A
14	GND	Ground	Power	N/A
15	PWR_EN2	Port power switch enable #2	DI	Connect to ground or V_{DD} (depending on the polarity decoded via COMM_ILIM pin)
16	ALERT#2	Output fault ALERT for V_{BUS2} (requires pull-up resistor)	OD	Connect to ground
17	SMCLK	SMCLK - SMBus clock input (requires pull-up resistor)	DI	Connect to V_{PULLUP}(or to ground in Stand-Alone mode)
18	SMDATA	SMDATA - SMBus data input/output (requires pull-up resistor)	DIOD	Connect to V_{PULLUP} (or to ground in Stand-Alone mode)
19	GND	Ground	Power	N/A
20	ALERT#1	Output fault ALERT for V_{BUS1} (requires pull-up resistor)	OD	Connect to ground
21	EP	Exposed thermal pad. Must be connected to electrical ground.	EP	N/A

TABLE 3-2: PIN TYPES

Pin Type	Description
Power	This pin is used to supply power or ground to the device
Hi-Power	This pin is a high-current pin
AIO	Analog Input/Output - this pin is used as an I/O for analog signals
DI	Digital Input - this pin is used as a digital input
DIOD	Open-Drain Digital Input/Output - this pin is bidirectional. It is open-drain and requires a pull-up resistor.
OD	Open-Drain Digital Output - used as a digital output. It is open-drain and requires a pull-up resistor.
EP	Exposed thermal pad

4.0 TERMS AND ABBREVIATIONS

Note: The PWR_EN1 and PWR_EN2 pins each have configuration bits (“<pin name>_S” in General Configuration 1 register (Address 11h) and General Configuration 2 register (Address 12h)) that may be used to perform the same function as the external pin state. These bits are accessed via the SMBus/I²C and are OR’d with the respective pin. This OR’d combination of pin state and register bit is referenced as the <pin name> control.

TABLE 4-1: TERMS AND ABBREVIATIONS

Term/Abbreviation	Description
CC	Constant Current
Current Limiting Mode	Determines the action that is performed when the I_{BUS} current reaches the I_{LIM} threshold. Trip opens the port power switch. Constant Current (variable slope) allows V_{BUS} to be dropped by the portable device.
I_{BUS_R2MIN}	Current limiter mode boundary
I_{LIM}	The I_{BUS} current threshold used in current limiting. In Trip mode, when I_{LIM} is reached, the port power switch is opened. In Constant Current mode, when the current exceeds I_{LIM}, operation continues at a reduced voltage and increased current; if V_{BUS} voltage drops below V_{BUS_MIN}, the port power switch is opened.
OCL	Overcurrent limit
POR	Power-on Reset
Portable Device	USB device attached to the USB port
Stand-Alone Mode	Indicates that the communications protocol is not active and all communications between the UCS2113 and a controller are done via the external pins only (PWR_EN1 and PWR_EN2 as inputs, and ALERT1# and ALERT2# as outputs)

NOTES:

5.0 GENERAL DESCRIPTION

The UCS2113 is a dual-port power switch. Two USB power ports are supported with current limits up to 3.0A continuous current (3.4A maximum) each. Selectable and programmable current limiting configurations are also available to the application. A typical block diagram is shown in Figure 5-1.

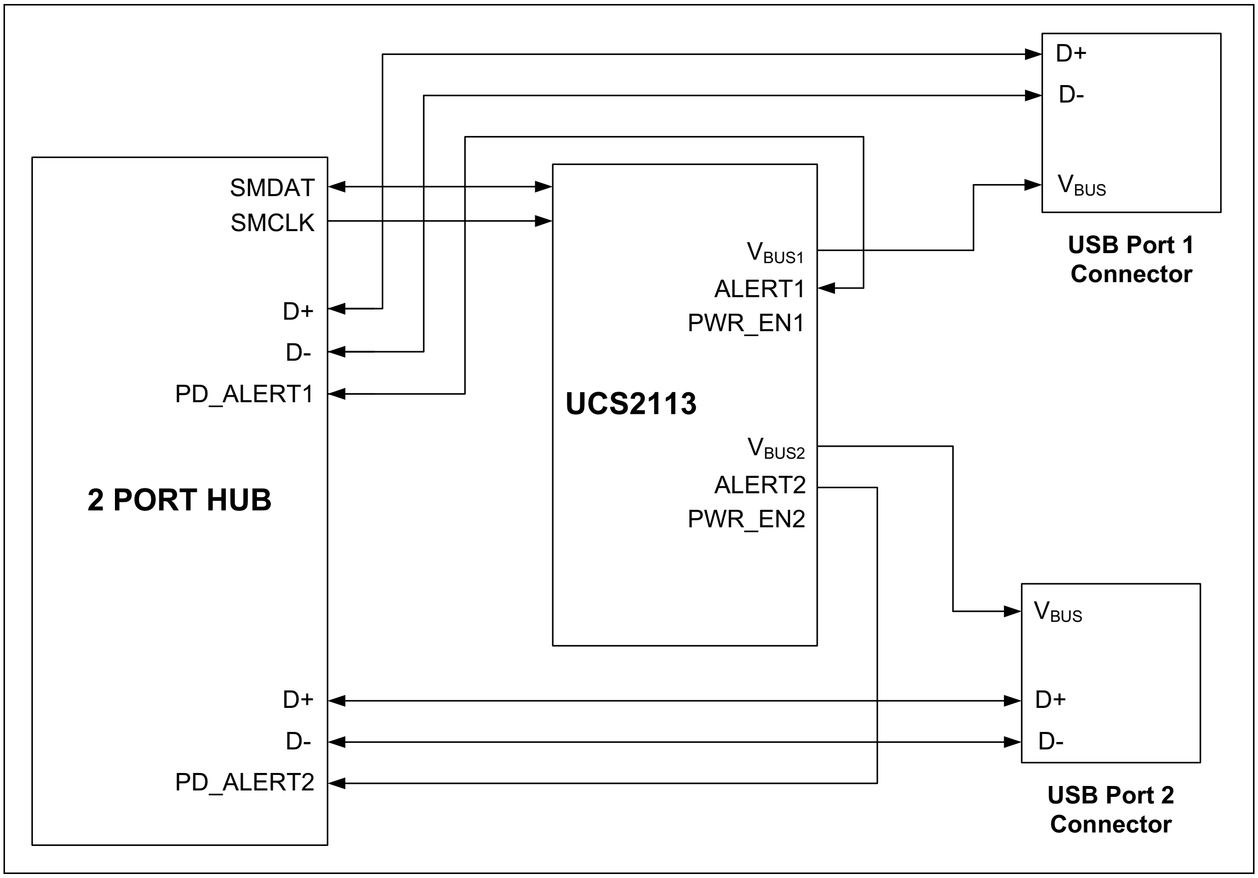


FIGURE 5-1: *Typical USB Application.*

5.1 UCS2113 Power States

Power states are indicators of the device's current consumption in the system and the functionality of the digital logic. Table 5-1 details the UCS2113 power states.

TABLE 5-1: POWER STATES DESCRIPTION

State	Description
Off	This power state is entered when the voltage at the V_{DD} pin voltage is < V_{DD_TH}. In this state, the device is considered "off". The UCS2113 will not retain its digital states and register contents nor respond to SMBus/I^{2}C communications. The port power switch will be off. See **Section 5.1.1 "Off State Operation"**.
Sleep	This is the lowest power state available. While in this state, the UCS2113 will retain digital functionality and wake to respond to SMBus/I^{2}C communications. See **Section 5.1.2 "Sleep State Operation"**.
Error	This power state is entered when a fault condition exists. Error power state is one or both channels in Fault Handling. This state is updated as Priority One. The Interrupt Status Registers for each channel will update the fault detected per channel. Only the channel that has detected a Fault will be affected since the other channel can remain active if no fault is detected. See **Section 5.1.4 "Error State Operation"**.
Active	Active power State is one, or both channels active and sourcing current to the V_{BUS} Port. This state is updated as Priority Two. None of the channels have detected Fault. This power state provides full functionality. While in this state, operations include activation of the port power switch, current limiting, and charge rationing. See **Section 5.1.3 "Active State Operation"**.

Table 5-2 shows the settings for the various power states, except Off and Error. If V_{DD} < V_{DD_TH}, the UCS2113 is in the Off state.

TABLE 5-2: POWER STATES CONTROL SETTINGS

Power State	PWR_EN1	PWR_EN2	Behavior
Sleep	disabled	disabled	• All switches disabled • V_{BUS} will be near ground potential • The UCS2113 wakes to respond to SMBus communications
Active	enabled	disabled	• Port power switch is on for V_{BUS1} • V_{BUS2} pins are near ground potential or floating (Note 1)
	disabled	enabled	• Port power switch is on for V_{BUS2} • V_{BUS1} pins are near ground potential or floating (Note 1)
	enabled	enabled	• Port power switch is on for V_{BUS1} and V_{BUS2}

Note 1: If the bit EN_VBUS_DISCHG is '1', the V_{BUS} is discharged automatically and V_{BUS} is near ground potential. If the bit EN_VBUS_DISCHG is '0' then the corresponding VBUS pins are floating (V_{BUS} discharge is controlled by the SMBus master).

5.1.1 OFF STATE OPERATION

The device will be in the Off state if V_{DD} is less than V_{DD_TH}. When the UCS2113 is in the Off state, it will do nothing and all circuitry will be disabled. Digital register values are not stored and the device will not respond to SMBus commands.

5.1.2 SLEEP STATE OPERATION

The PWR_EN1 and PWR_EN2 pins may be used to cause the UCS2113 to enter/exit Sleep. These pins are AND'ed for Sleep mode.

When the UCS2113 is in the Sleep state, the device will be in its lowest power state. The port power switch will be disabled. V_{BUS1} and V_{BUS2} will be near ground potential. The ALERT#1 and ALERT#2 pins will not be asserted. If asserted prior to entering the Sleep state, the ALERT# pin will be released. SMBus activity is limited to single byte read or write.

The first data byte read from the UCS2113 when it is in the Sleep state will wake it; however, the data to be read will return all 0's and should be considered invalid. This is a "dummy" read byte meant to wake the UCS2113. Subsequent read or write bytes will be accepted normally. After the dummy read, the UCS2113 will be in a higher power state (see Figure 5-2). After communication has not occurred for t_{IDLE_SLEEP}, the UCS2113 will return to Sleep.

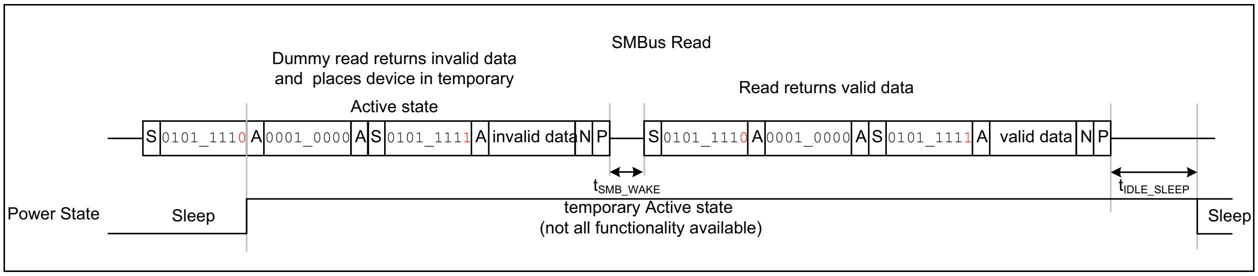


FIGURE 5-2: *Wake from Sleep using SMBus Read.*

5.1.3 ACTIVE STATE OPERATION

Every time the UCS2113 enters the Active state, the port power switches are closed. The UCS2113 cannot be in the Active state (and therefore, the port power switch cannot be turned on) if any of the following conditions exist:

- $V_S < V_{S\_UVLO}$
- PWR_EN1 and PWR_EN2 are disabled.

5.1.4 ERROR STATE OPERATION

The UCS2113 will enter the Error state from the Active state when any of the following events are detected:

- The maximum allowable internal die temperature (T_{TSD_HIGH}) has been exceeded.
- The T_{TSD_LOW} die temperature has been exceeded and any of the following conditions is met:
  - a power switch operates in constant current mode
  - PWR_EN1 and/or PWR_EN2 controls transition from inactive to active.
  - it is a power up situation and PWR_EN1 and/or PWR_EN2 pins are active.
- An overcurrent condition has been detected.
- An undervoltage condition on either V_{BUS} pin has been detected (see **Section 5.3.4 "Undervoltage Lockout on VS"**).
- A back-voltage condition has been detected (see **Section 5.3.2 "Back-voltage Detection"**).
- A discharge error has been detected.
- An overvoltage condition on the V_S pin.

When the UCS2113 enters the Error state, the port power switch will be disabled while the ALERT# pin is asserted. It will remain off while in this power state. The UCS2113 will leave this state as determined by the fault handling selection.

With the Auto-recovery fault handler, after the t_{CYCLE} time period, the UCS2113 will check that all of the error conditions have been removed.

If all of the error conditions have been removed, the UCS2113 will return to the Active state.

If both PWR_EN1 and PWR_EN2 controls transition from active to inactive while the UCS2113 is in the Error state, the device will not enter the Sleep state. After the fault has been removed, the UCS2113 will not automatically enter the Sleep state if the EN_VBUS_DISCHG bit from the General Configuration 2 Register is not set (default setting). To enter the Sleep state, the PWR_EN pins must be toggled or an SMBus read register command must be sent.

5.2 Communication

The UCS2113 can operate in SMBus mode (see **Section 7.0 "System Management Bus Protocol"**) or Stand-Alone mode. The resistor connected to the COMM_ILIM pin determines the operating mode and the hardware-set I_{LIM} setting, as shown in Table 5-3. Unless connected to GND or V_{DD}, the resistors in Table 5-3 are external pull-down resistors.

The SMBus address is specified in **Section 7.2 "SMBus Address and RD/WR Bit"**.

TABLE 5-3: COMMUNICATION DECODE

COMM_ILIM Pull Down Resistor (±1%)	PWR_EN1 and PWR_EN2 Polarity	I_{LIM} (A)	Total I_{LIM} (A) (Note 1)	Communication Mode
GND	Active-High	0.53	0.53 + 0.53	SMBUS
10 kΩ	Active-High	0.96	0.96 + 0.96	SMBUS
12 kΩ	Active-High	1.07	1.07 + 1.07	SMBUS
15 kΩ	Active-High	1.28	1.28 + 1.28	SMBUS
18 kΩ	Active-High	1.6	1.6 + 1.6	SMBUS

TABLE 5-3: COMMUNICATION DECODE (CONTINUED)

COMM_ILIM Pull Down Resistor (±1%)	PWR_EN1 and PWR_EN2 Polarity	I_{LIM} (A)	Total I_{LIM} (A) (Note 1)	Communication Mode
22 kΩ	Active-High	2.13	2.13 + 2.13	SMBUS
27 kΩ	Active-High	2.67	2.67 + 2.67	SMBUS
33 kΩ	Active-High	3.2	3.2 + 3.2	SMBUS
47 kΩ	Active-Low	0.53	0.53 + 0.53	Stand-Alone
56 kΩ	Active-Low	0.96	0.96 + 0.96	Stand-Alone
68 kΩ	Active-Low	1.07	1.07 + 1.07	Stand-Alone
82 kΩ	Active-Low	1.28	1.28 + 1.28	Stand-Alone
100 kΩ	Active-Low	1.6	1.6 + 1.6	Stand-Alone
120 kΩ	Active-Low	2.13	2.13 + 2.13	Stand-Alone
150 kΩ	Active-Low	2.67	2.67 + 2.67	Stand-Alone
V_{DD}	Active-Low	3.2	3.2 + 3.2	Stand-Alone

Note 1: The total maximum current depends on power dissipation characteristics of the design (see Table 1-1).

5.3 Supply Voltages

5.3.1 V_{DD} SUPPLY VOLTAGE

The UCS2113 requires 4.5V to 5.5V to be present on the V_{DD} pin for core device functionality. Core device functionality consists of maintaining register states and wake-up upon SMBus/I^2C query.

5.3.2 BACK-VOLTAGE DETECTION

The back-voltage detector is functional in all power states (Sleep and Active).

When in Sleep, the UCS2113 will enter the Error state from Sleep if a back-voltage condition was detected.

Whenever the following condition is true for either port, the port power switch will be disabled and a back-voltage event will be flagged. This will cause the UCS2113 to enter the Error power state (see **Section 5.1.4 "Error State Operation"**).

Note: The V_{BUS} voltage exceeds the V_S and/or the V_{DD} pin voltage by V_{BV_TH} and the port power switch is closed. The port power switch will be opened immediately. If the condition lasts for longer than t_{MASK}, then the UCS2113 will enter the Error state. Otherwise, the port power switch will be turned on as soon as the condition is removed.

5.3.3 BACK-DRIVE CURRENT PROTECTION

If a portable device is attached that is self-powered, it may drive the V_{BUS} port to its power supply voltage level; however, the UCS2113 is designed such that leakage current from the V_{BUS} pins to the V_{DD} and/or the V_S pin shall not exceed I_{LKG_1} (if the V_{DD} and/or V_S voltage is zero) or I_{LKG_2} (if the V_{DD} and/or V_S voltage exceeds V_{DD_TH} and the power switch is open).

5.3.4 UNDERVOLTAGE LOCKOUT ON V_S

The UCS2113 requires a minimum voltage (V_{S_UVLO}) be present on the V_S pin for Active power state.

5.3.5 OVERVOLTAGE DETECTION AND LOCKOUT ON VS

Both power switches will be disabled if the voltage on any V_S pin exceeds a voltage (V_{S_OV}) for longer than the specified time (t_{MASK}). This will cause the device to enter the Error state and both ALERT#1 and ALERT#2 pins will be asserted.

5.3.6 PWR_EN1 AND PWR_EN2 INPUT

The PWR_EN control affects the power state and enables the port power switch to be turned on if conditions are met (see Table 5-2). The port power switch cannot be closed if PWR_EN is disabled. However, if PWR_EN is enabled, the port power switch is not necessarily closed (see **Section 5.1.3 "Active State Operation"**). In SMBus mode, the PWR_EN1 and PWR_EN2 pins states will be ignored by the UCS2113 if the PIN_IGN configuration bit is set; otherwise, the PWR_EN1S and PWR_EN2S configuration bits are checked along with the pins.

5.4 Discrete Output Pins

5.4.1 ALERT#1 AND ALERT#2 OUTPUT PINS

The UCS2113 has two independent ALERT# out pins. ALERT#1 is tied to the status of the V_{BUS1} pin. ALERT#2 is tied to the status of the V_{BUS2} pin.

The ALERT# pin is an active-low open-drain interrupt to the host controller. The ALERT# pin is asserted when an error occurs. Also, when charge rationing is enabled, the ALERT# pin is asserted by default when the current rationing threshold is reached (as determined by RATION_BEH<1:0>). The ALERT# pin is released when all error conditions that may assert the ALERT# pin (such as an error condition and charge rationing) have been removed or reset as necessary.

The UCS2113 is compatible with the Microchip hub devices supporting single pin power control feature. These hub devices have a single connection to the PWR_EN and ALERT# pins of the UCS2113, which are tied together in the application.

5.4.2 BOOST# OUTPUT PIN

The UCS2113 provides a BOOST# output pin to compensate for voltage drops during high loads. The BOOST# pin is an active-low, open-drain output that would be connected to a resistor in the DC-DC converter's feedback error voltage loop (see Figure 5-3).

The BOOST# pin is asserted when V_{BUS} Current > I_{BOOST}. I_{BOOST} typical value is 1.9A. The BOOST# is OR'ed for both V_{BUS1} and V_{BUS2} ports. When the BOOST# pin is asserted, it will remain in this state for at least t_{BOOST_MAT} (minimum assertion time).

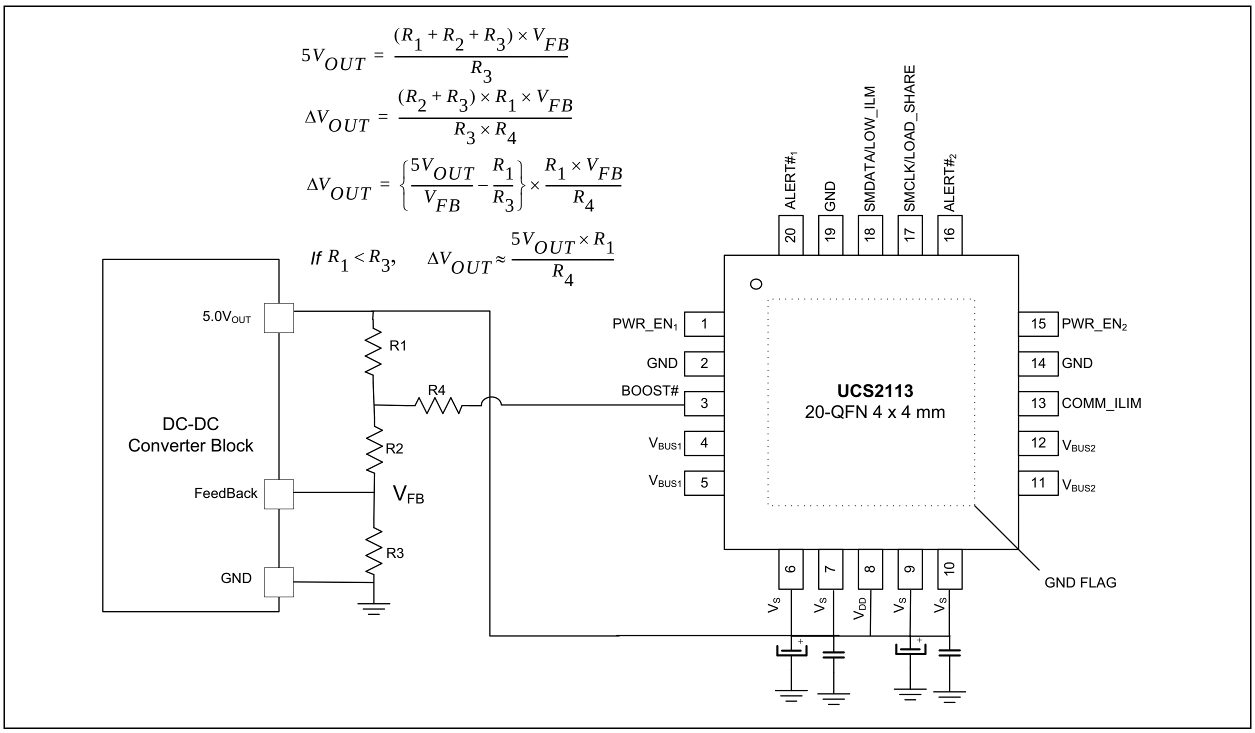


FIGURE 5-3: *Boost# Pin Usage.*

5.5 Discrete Input Pins

5.5.1 COMM_ILIM INPUT

The COMM_ILIM input determines the communications mode, as shown in Table 6-1. This is also the hardware strap for MAX Current Limit.

5.5.2 SMCLK

When operated in Stand-Alone mode, this pin should be tied to ground. When the UCS2113 is configured for SMBus communications, the SMCLK is the clock input.

5.5.3 SMDATA

When used in Stand-Alone, this pin should be tied to ground.

When the UCS2113 is configured for SMBus communications, the SMDATA is the data input/output.

NOTES:

6.0 USB PORT POWER SWITCH

To assure compliance to various charging specifications, the UCS2113 contains a USB port power switch that supports two current-limiting modes: Trip and Constant current (variable slope). The current limit (I_{LIM}) is pin selectable (and may be updated via the register set). The switch also includes soft start circuitry and a separate short circuit current limit.

The port power switch is on in the Active state (except when V_{BUS} is discharging).

6.1 Current Limiting

6.1.1 CURRENT LIMIT SETTING

The UCS2113 hardware set current limit, I_{LIM}, can be one of eight values. This resistor value is read once upon UCS2113 power-up. The current limit can be changed via the SMBus/I^{2}C after power-up; however, the programmed current limit cannot exceed the hardware set current limit. Unless connected to V_{DD}, the resistors in Table 6-1 are pull-down resistors.

At power-up, the communication mode (Stand-Alone or SMBus/I^{2}C) and hardware current limit (I_{LIM}) are determined via the pull-down resistor (or pull-up resistor if connected to V_{DD}) on the COMM_ILIM pin, as shown in Table 6-1.

6.1.2 SHORT CIRCUIT OUTPUT CURRENT LIMITING

Short circuit current limiting occurs when the output current is above the selectable current limit (I_{LIMx}). This event will be detected and the current will immediately be limited (within t_{SHORT_LIM} time). If the condition remains, the port power switch will flag an Error condition and enter the Error state.

6.1.3 SOFT START

When the PWR_EN control changes states to enable the port power switch, the UCS2113 invokes a soft start routine for the duration of the V_{BUS} rise time (t_{R_BUS}). This soft start routine will limit current flow from V_S into V_{BUS} while it is active. This circuitry will prevent current spikes due to a step in the portable device current draw.

In the case when a portable device is attached while the PWR_EN pin is already enabled, if the bus current exceeds I_{LIM}, the UCS2113 current limiter will respond within a specified time (t_{SHORT_LIM}) and will operate normally at this point. The C_{BUS} capacitor will deliver the extra current, if any, as required by the load change.

TABLE 6-1: I_{LIM} DECODE

COMM_ILIM Pulldown Resistor (±1%)	PWR_EN1 and PWR_EN2 Polarity	I_{LIM} (A)	Total I_{LIM} (A) (Note 1)
GND	Active-High	0.53	0.53+0.53
10 kΩ	Active-High	0.96	0.96+0.96
12 kΩ	Active-High	1.07	1.07+1.07
15 kΩ	Active-High	1.28	1.28+1.28
18 kΩ	Active-High	1.6	1.6+1.6
22 kΩ	Active-High	2.13	2.13+2.13
27 kΩ	Active-High	2.67	2.67+2.67
33 kΩ	Active-High	3.2	3.2+3.2
47 kΩ	Active-Low	0.53	0.53+0.53
56 kΩ	Active-Low	0.96	0.96+0.96
68 kΩ	Active-Low	1.07	1.07+1.07
82 kΩ	Active-Low	1.28	1.28+1.28
100 kΩ	Active-Low	1.6	1.6+1.6
120 kΩ	Active-Low	2.13	2.13+2.13
150 kΩ	Active-Low	2.67	2.67+2.67
V_{DD}	Active-Low	3.2	3.2+3.2

Note 1: The total maximum current depends on power dissipation characteristics of the design (see Table 1-1).

6.1.4 CURRENT LIMITING MODES

The UCS2113 current limiting has two modes: Trip and Constant Current (variable slope). Either mode functions at all times when the port power switch is closed.

6.1.4.1 Trip Mode

When using Trip current limiting, the UCS2113 USB port power switch functions as a low-resistance switch and rapidly turns off if the current limit is exceeded. While operating using Trip current limiting, the V_{BUS} output voltage will be held relatively constant (equal to the V_S voltage minus the R_{ON} x I_{BUS} current) for all current values up to the I_{LIM}.

If the current drawn by a portable device exceeds I_{LIM}, the following occurs:

1. The port power switch will be turned off (Trip action).
2. The UCS2113 will enter the Error state and assert the ALERT# pin.
3. The fault handling circuitry will then determine subsequent actions.

Figure 6-1 shows operation of current limits in Trip mode with the shaded area representing the USB 2.0 specified V_{BUS} range. Dashed lines indicate the port power switch output will go to zero (e.g., Trip) when I_{LIM} is exceeded. Note that operation at all possible values of I_{LIM} are shown in Figure 6-1 for illustrative purposes only; in actual operation only one I_{LIM} can be active at any time.

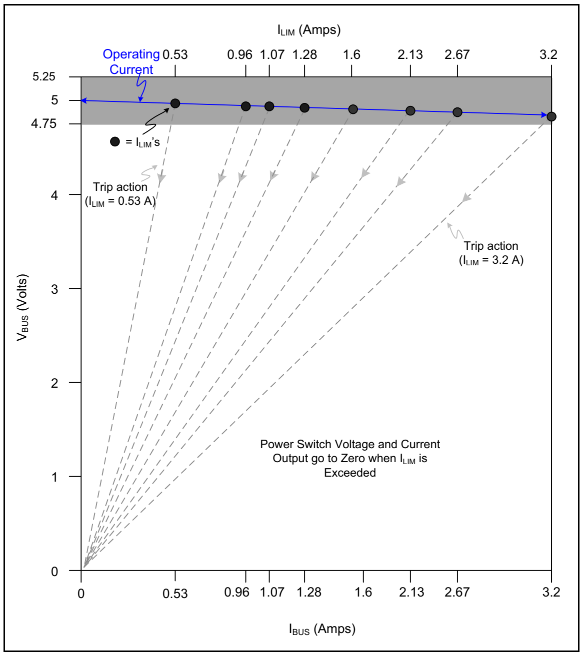


FIGURE 6-1: *Current Limiting in Trip Mode.*

6.1.4.2 Constant Current Limiting (Variable Slope)

Constant current limiting is used when the current drawn is greater than I_{LIM} (and $I_{LIM} \leq 1.6A$). In CC mode, the port power switch allows the attached portable device to reduce V_{BUS} output voltage to less than the input V_S voltage while maintaining current delivery. The V/I slope depends on the user set I_{LIM} value. This slope is held constant for a given I_{LIM} value.

This mode is specifically provided for devices that rely on resistive means to reduce V_{BUS} voltage for direct battery charging or to allow portable devices a means to “test” charger capacity. See Figure 6-2.

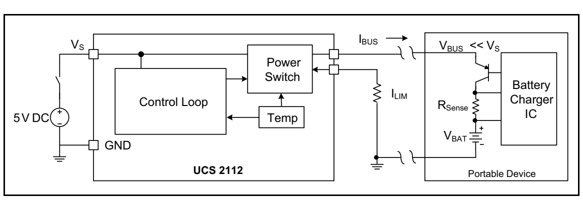


FIGURE 6-2: *Constant Current Example.*

Figure 6-3 shows operation of current limits while using CC mode. Unlike Trip mode, once I_{BUS} current exceeds I_{LIM}, operation continues at a reduced voltage and increased current. Note that the shaded area representing the USB 2.0 specified V_{BUS} range is now restricted to an upper current limit of I_{BUS_R2MIN}. Note that the UCS2113 will heat up along each load line as voltage decreases. If the internal temperature exceeds the T_{TSD_LOW} threshold, the corresponding power switch operating in constant current mode will open. If the internal temperature exceeds the T_{TSD_HIGH} threshold, both power switches will open, regardless of whether the power switch channels are in current limit. Also note that when the V_{BUS} voltage is brought low enough (below V_{BUS_MIN}), the port power switch will open.

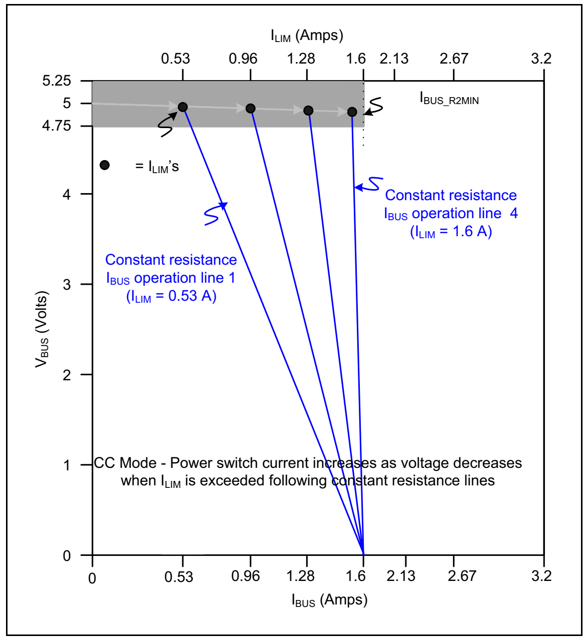


FIGURE 6-3: *Current Limiting in CC Mode.*

6.2 USB Port Power Profiles

The UCS2113 combines the qualities of traditional USB port power switches with USB port power profiles set forth in the USB-IF BC1.2 specification. USB port power profiles consist of distinct voltage-current operation regions defined by “keep-out” and “operation” regions.

While operating in the CC mode of operation, the UCS2113 provides voltage-current output operating profiles that are specified by two keep-out regions.

If the current reaches the I_{BUS_R2MIN} setting for longer than t_{MASK}, the UCS2113 enters the Error state and an Overcurrent event is flagged.

If the V_{BUS} voltage ever goes below the no operation lower-voltage keep-out (V_{BUS_MIN}) value for longer than t_{MASK}, the port power switch is disabled and a keep-out violation is flagged (by setting the MIN_KEEP_OUT status bit). This will cause the device to enter the Error state.

Figure 6-4 illustrates the relationship between these USB port power profile parameters.

6.2.1 OPERATION WITHIN A USB PORT POWER PROFILE

An attached device may be constrained to operate within the boundaries of a USB port power profile by setting the value of I_{LIM} less than the USB port power profile I_{BUS_R2MIN} value. In this case, the port power switch will be in Trip mode up until I_{LIM} is exceeded. At which point, the switch will transition into CC mode. If the attached device reduces the output voltage to less than V_{BUS_MIN}, the switch will trip and terminate charging.

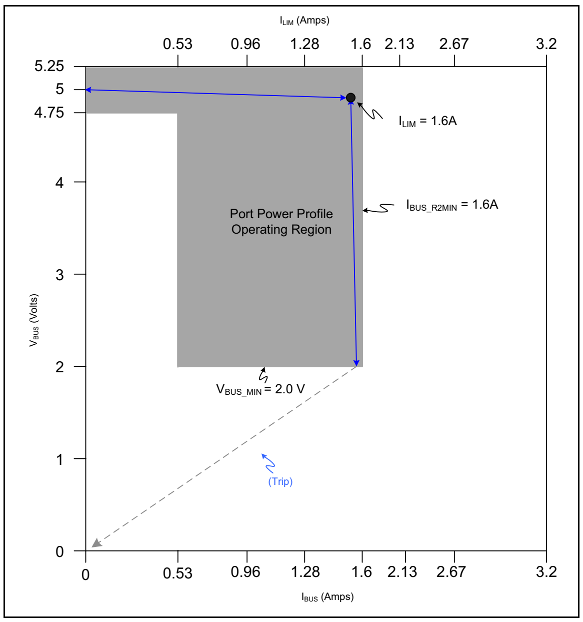


FIGURE 6-4: *$I_{LIM} < I_{BUS\_R2MIN}$ Example.*

Note:	The CC mode of operation is possible only up to 1.6A. As long as the value of I_{LIM} is less than the fixed port power profile I_{BUS_R2MIN} value, CC mode is possible. Otherwise, the USB port power switch will operate in Trip mode operation.

6.2.2 OPERATION OUTSIDE OF A USB PORT POWER PROFILE

An attached device may be allowed to operate outside of the boundaries of a USB port power profile by setting the value of I_{LIM} greater than the USB port power profile I_{BUS_R2MIN} value. This is the default operation for all portable devices. In this case, the USB port power switch will operate in Trip mode until the bus current reaches the I_{LIM} value. Once the I_{LIM} value has been exceeded, the port power switch will open and terminate charging. Figure 6-5 illustrates an example of current limiting in this configuration.

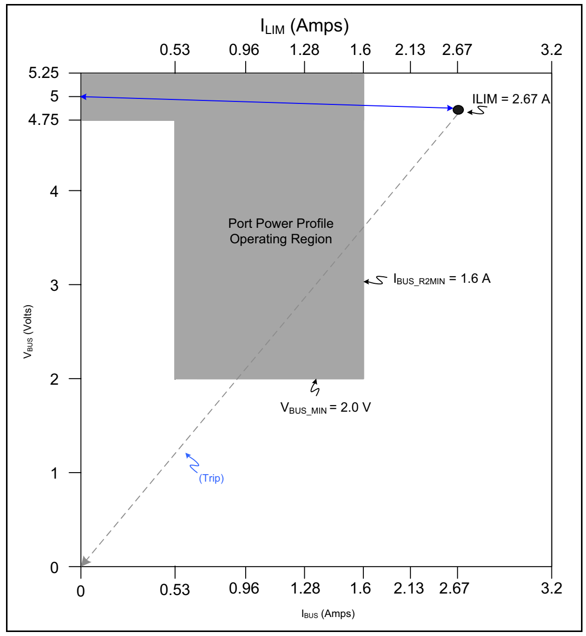


FIGURE 6-5: *$I_{LIM} > I_{BUS\_R2MIN}$ Example.*

6.3 Thermal Protection

The UCS2113 utilizes two-stage internal thermal management. The first is triggered when the die temperature exceeds T_{TSD_LOW} threshold and the second is triggered when the die temperature exceeds T_{TSD_HIGH} threshold.

6.3.0.1 THE FIRST THERMAL SHUTDOWN STAGE (T_{TSD_LOW})

The first stage turns off the individual power switch channel when the die temperature exceeds T_{TSD_LOW} threshold and a power switch operates in constant current mode. It also causes the corresponding channel to enter in error state and the corresponding ALERT# pin will be asserted.

When an over-current condition appears, the power switch operates in constant current mode for the duration of t_{MASK} time. Because of the increased voltage drop across the switch, the die temperature increases. If the die temperature exceeds T_{TSD_LOW} threshold before the expiration of the t_{MASK} time, then the power switch will open immediately.

If the T_{TSD_LOW} threshold has been exceeded, but the die temperature has not decreased below the T_{TSD_LOW} recovery threshold, then the power switch cannot be closed when commanded by the PWR_EN1 or PWR_EN2 controls in the following situations:

- PWR_EN1 and/or PWR_EN2 controls transition from inactive to active.
- it is a power up situation and PWR_EN1 and/or PWR_EN2 pins are active.

In these situations, the corresponding channel will enter in error state and the corresponding ALERT# pin will be asserted.

The first thermal shutdown stage allows the two ports to work independently, by preventing the die temperature to increase during over-current conditions and to exceed the maximum allowable temperature (T_{TSD_HIGH}).

The error state will persist and the power switches can not be closed until the temperature is below T_{TSD_LOW} - $T_{TSD\_LOW\_HYST}$.

6.3.0.2 THE SECOND THERMAL SHUTDOWN STAGE (T_{TSD_HIGH})

The second thermal protection stage turns off both power switches when the die temperature exceeds T_{TSD_HIGH} threshold, regardless of whether the power switch channels are in current limit. It also causes both channels to enter in error state and both ALERT#1 and ALERT#2 pins to be asserted.

The error state will persist and the power switches cannot be closed until the temperature is below T_{TSD_HIGH} - $T_{TSD\_HIGH\_HYST}$.

6.4 V_{BUS} Discharge

When the EN_VBUS_DISCHG bit from General Configuration 2 Register is set (by default it is not set), the UCS2113 will discharge V_{BUS} through an internal 100Ω resistor when at least one of the following conditions occur:

- The PWR_EN control is disabled (triggered on the inactive edge of the PWR_EN control).
- The V_S voltage drops below a specified threshold (V_{S_UVLO}) that causes the port power switch to be disabled.
- When commanded into the Sleep power state.
- Upon recovery from the Error state.
- When commanded via the SMBus in the Active state.

When the automatic V_{BUS} discharge circuitry is activated, the UCS2113 will confirm that V_{BUS} was discharged at the end of the $t_{DISCHARGE}$ time. If the V_{BUS} voltage is not below the V_{TEST} level, a discharge error will be flagged (by setting the DISCH_ERR(1/2) status bit) and the UCS2113 will enter the Error state.

When the EN_VBUS_DISCHG bit from General Configuration 2 Register is not set (default setting), the automatic V_{BUS} discharges described above are disabled. In this case, the SMBus master must set and clear bits DISCHG_LOAD1 and DISCHG_LOAD2 from the Current Limit Behavior Registers, to discharge the V_{BUS1} and V_{BUS2}. Setting the DISCHG_LOAD1 and DISCHG_LOAD2 bits connects the internal 100Ω resistor to discharge the corresponding V_{BUS} path. This functionality doesn't use any timers. The discharge time is controlled by the SMBus master, which must clear this bit when its internal timer expires.

6.5 Charge Rationing Interactions

When charge rationing is active, regardless of the specified behavior, the UCS2113 will function normally until the charge rationing threshold is reached. Note that charge rationing is only active when the UCS2113 is in the Active state. Changing the charge rationing behavior will have no effect on the charge rationing data registers. If the behavior is changed prior to reaching the charge rationing threshold, this change will occur and be transparent to the user. When the charge rationing threshold is reached, the UCS2113 will take action as shown in Table 6-2. If the behavior is changed after the charge rationing threshold has been reached, the UCS2113 will immediately adopt the newly programmed behavior, clearing the ALERT# pin and restoring switch operation respectively (see Table 6-4).

TABLE 6-2: CHARGE RATIONING BEHAVIOR

RATION_BEH (1 or 2) <1:0>		Behavior	Actions Taken	Notes
1	0			
0	0	Report	ALERT# pin asserted.	
0	1	Report and Disconnect (default)	1. ALERT# pin asserted 2. Port power switch disconnected	All bus monitoring is still active. Toggling the PWR_EN control will cause the device to change power states as defined by the registers; however, the port power switch will remain off until the rationing circuitry is reset.
1	0	Disconnect and Go to Sleep	1. Port power switch disconnected 2. Device will enter the Sleep state	All V_{BUS} and V_S monitoring will be stopped. Toggling the PWR_EN control will have no effect on the power state until the rationing circuitry is reset.
1	1	Ignore	Take no further action	

TABLE 6-3: CHARGE RATIONING RESET BEHAVIOR

Behavior	Reset Actions
Report	1. Reset the Total Accumulated Charge registers 2. Clear the RATION status bit 3. Release the ALERT# pin
Report and Disconnect	1. Reset the Total Accumulated Charge registers 2. Clear the RATION status bit 3. Release the ALERT# pin 4. Check the PWR_EN controls and enter the indicated power state if the controls changed
Disconnect and Go to Sleep	1. Reset the Total Accumulated Charge registers 2. Clear the RATION status bit 3. Check the PWR_EN controls and enter the indicated power state if the controls changed
Ignore	1. Reset the Total Accumulated Charge registers 2. Clear the RATION status bit

TABLE 6-4: EFFECTS OF CHANGING RATIONING BEHAVIOR AFTER THRESHOLD REACHED

Previous Behavior	New Behavior	Actions Taken
Ignore	Report	Assert ALERT# pin
	Report and Disconnect	1. Assert ALERT# pin 2. Open port power switch. See the Report and Disconnect (default) in Table 6-2
	Disconnect and Go to Sleep	1. Open port power switch 2. Enter the Sleep state. See the Disconnect and Go to Sleep in Table 6-2

TABLE 6-4: EFFECTS OF CHANGING RATIONING BEHAVIOR AFTER THRESHOLD REACHED

Previous Behavior	New Behavior	Actions Taken
Report	Ignore	Release ALERT# pin.
	Report and Disconnect	Open port power switch. See the Report and Disconnect (default) in Table 6-2.
	Disconnect and Go to Sleep	1. Release the ALERT# pin 2. Open the port power switch 3. Enter the Sleep state. See the Disconnect and Go to Sleep in Table 6-2.
Report and Disconnect	Ignore	1. Release the ALERT# pin 2. Check the PWR_EN controls and enter the indicated power state if the controls changed
	Report	Check the PWR_EN controls and enter the indicated power state if the controls changed
	Disconnect and Go to Sleep	1. Release the ALERT# pin 2. Enter the Sleep state. See the Disconnect and Go to Sleep in Table 6-2.
Disconnect and Go to Sleep	Ignore	Check the PWR_EN controls and enter the indicated power state if the controls changed
	Report	1. Assert the ALERT# pin 2. Check the PWR_EN controls and enter the indicated power state if the controls changed
	Report and Disconnect	1. Assert the ALERT# pin 2. Check the PWR_EN controls to determine the power state, then enter that state, except that the port power switch will not be closed

If the RATION_EN control is set to ‘0’ prior to reaching the charge rationing threshold, rationing will be disabled and the Total Accumulated Charge registers will be cleared. If the RATION_EN control is set to ‘0’ after the charge rationing threshold has been reached, the following additional steps occur:

1. RATION status bit will be cleared.
2. The ALERT# pin will be released if asserted by the rationing circuitry and no other conditions are present.
3. The PWR_EN controls are checked to determine the power state.

Setting the RATION_RST control to ‘1’ will automatically reset the Total Accumulated Charge registers to 00_00h. If this is done prior to reaching the charge rationing threshold, the data will continue to be accumulated restarting from 00_00h. If this is done after the charge rationing threshold is reached, the UCS2113 will take action as shown in Table 6-3.

6.6 Fault Handling Mechanism

The UCS2113 has two modes for handling faults:

- Latch (latch-upon-fault)
- Auto-recovery (automatically attempt to restore the Active power state after a fault occurs).

If the SMBus is actively utilized, Auto-Recovery Fault Handling is the default error handler as determined by the LATCH_SET bit. Faults include overcurrent, overvoltage (on V_S), undervoltage (on V_{BUS}), back-voltage (V_{BUS} to V_S or V_{BUS} to V_{DD}), discharge error, and maximum allowable internal die temperature (T_{TSD_HIGH}) exceeded. Fault conditions also include the situations when T_{TSD_LOW} die temperature has been exceeded and any of the following conditions are met:

- a power switch operates in constant current mode
- PWR_EN1 and/or PWR_EN2 controls transition from inactive to active.
- it is a power up situation and PWR_EN1 and/or PWR_EN2 pins are active.

Faults do not include:

- keep-out violations except VBUS_MIN.
- T_{TSD_LOW} die temperature has been exceeded and any of the following conditions are met:
  - the power switch is closed at the time when T_{TSD_LOW} is reached and it is not in constant current mode.
  - the power switch remains open (PWR_EN1 and/or PWR_EN2 controls are not active).

6.6.1 AUTO-RECOVERY FAULT HANDLING

When the LATCH_SET bit is low, Auto-Recovery Fault Handling is used. When an error condition is detected, the UCS2113 will immediately enter the Error state and assert the ALERT# pin. Independently from the host controller, the UCS2113 will wait a preset time (t_{CYCLE}), check error conditions (t_{TST}), and restore Active operation if the error condition(s) no longer exist. If all other conditions that may cause the ALERT# pin to be asserted have been removed, the ALERT# pin will be released. Short-Circuit Auto-Recovery example in Figure 6-6.

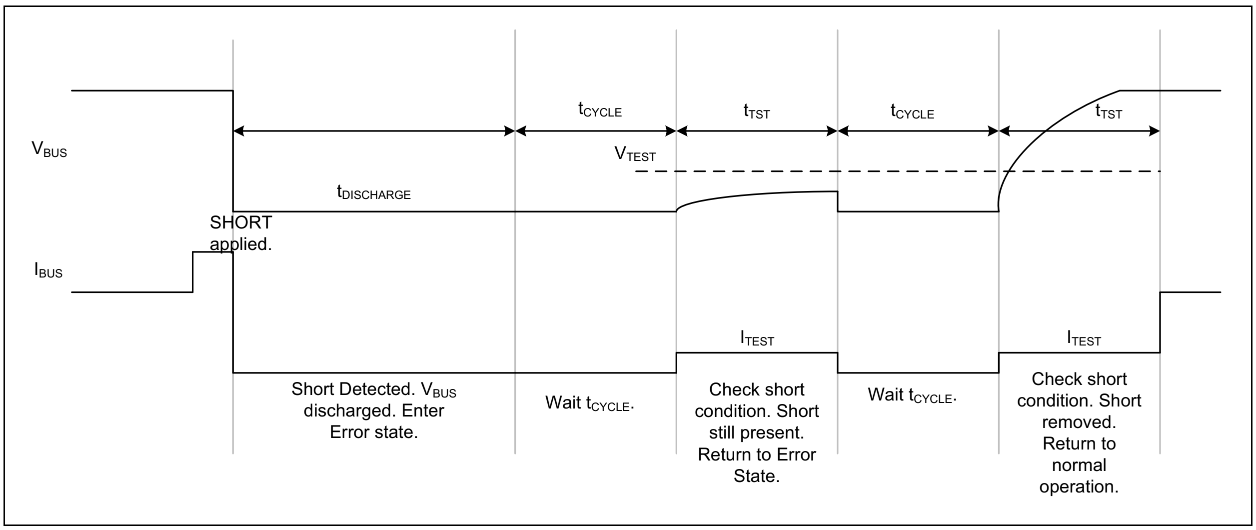


FIGURE 6-6: *Error Recovery.*

6.6.2 LATCHED FAULT HANDLING

When the LATCH_SET bit is high, latch fault handling is used. When an error condition is detected, the UCS2113 will enter the Error power state and assert the ALERT# (1 or 2) pin. Upon command from the host controller (by toggling the PWR_EN (1, or 2) pin control from enabled to disabled or by clearing the ERR bit via SMBus), the UCS2113 will check error conditions once and restore Active operation if error conditions no longer exist. If an error condition still exists, the host controller is required to issue the command again to check error conditions.

If the ALERT# pin is asserted and the interrupt status registers (addresses 03h or 04h) are not read, the corresponding ALERT# pin remains asserted until the corresponding PWR_EN pin is toggled.

If the ALERT# pin is asserted and the interrupt status registers are read, the ALERT# pin will deassert, but the UCS will remain in error state until the ERR bit is cleared via SMBus or the PWR_EN pin is toggled.

NOTES:

7.0 SYSTEM MANAGEMENT BUS PROTOCOL

In SMBus mode, the UCS2113 communicates with a host controller, such as a Microchip PIC® microcontroller or hub, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 1-1. Stretching of the SMCLK signal is supported; however, the UCS2113 will not stretch the clock signal.

7.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

7.2 SMBus Address and RD/$\overline{\text{WR}}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD/$\overline{\text{WR}}$ indicator bit. If this RD/$\overline{\text{WR}}$ bit is a logic '0', the SMBus Host is writing data to the client device. If this RD/$\overline{\text{WR}}$ bit is a logic '1', the SMBus Host is reading data from the client device.

The UCS2113 with the order code UCS2113-1-V/G4 has the SMBus address 57h - 1010_111(r/$\overline{\text{w}}$).

Customers should contact their distributor, representatives or field application engineer (FAE) for additional SMBus addresses. Local sales offices are also available to help customers. A list of sales offices and locations is included in the back of this document.

7.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8 bits of information.

7.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent. For the Block Read protocol, the Host will ACK (acknowledge) each data byte that it receives except the last data byte.

7.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the UCS2113 detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

7.6 SMBus Time-out

The UCS2113 includes an SMBus time-out feature. If the clock is held at logic '0' for $t_{TIMEOUT}$, the device can time out and reset the SMBus interface. The SMBus interface can also reset if both the clock and data lines are held at a logic '1' for t_{IDLE_RESET}. Communication is restored with a start condition.

The time-out function defaults to disabled. It can be enabled by clearing the DIS_TO bit in the General Configuration 3 register (see Register 8-9).

7.7 SMBus and I²C Compliance

The major difference between SMBus and I²C devices is highlighted here. For complete compliance information, refer to the SMBus 2.0 specification and Application Note 14.0.

- UCS2113 supports I²C fast mode at 400 kHz. This covers the SMBus maximum time of 100 kHz.
- The minimum frequency for SMBus communications is 10 kHz.
- The client protocol will reset if the clock is held low longer than 30 ms. This time out functionality is disabled by default in the UCS2113 and can be enabled by clearing the DIS_TO bit. I²C does not have a time out.
- Except when operating in Sleep, the client protocol will reset if both the clock and the data line are logic '1' for longer than 200 µs (idle condition). This function is disabled by default in the UCS2113 and can be enabled by clearing the DIS_TO bit. I²C does not have an idle condition.
- I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).
- I²C devices support block read and write differently. I²C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read/write is transmitted. The UCS2113 supports I²C formatting only.

7.8 SMBus Protocols

The UCS2113 is SMBus 2.0-compatible and supports Send Byte, Read Byte, Block Read, Receive Byte as valid protocols as shown below. The UCS2113 also supports the I²C block read and block write protocols. The device supports Write Byte, Read Byte, and Block Read/Block Write. All of the below protocols use the convention in Table 7-1.

TABLE 7-1: SMBUS PROTOCOL

Data Sent to Device	Data Sent to the Host
Data sent	Data sent

7.9 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in Table 7-2.

TABLE 7-2: WRITE BYTE PROTOCOL

START	Slave Address	WR	ACK	Reg. Addr.	ACK	Register Data	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

7.10 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 7-3.

TABLE 7-3: READ BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	
1→0	YYYY_YYY	0	0	XXh	0	
START	**Slave Address**	**RD**	**ACK**	**Register Data**	**NACK**	**STOP**
1 →0	YYYY_YYY	1	0	XXh	1	0 → 1

7.11 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers, as shown in Table 7-4. It is an extension of the Write Byte Protocol.

> **Note:** The Block Write and Block Read protocols require that the address pointer be automatically incremented. For a write command, the address pointer will be automatically incremented when the ACK is sent to the host. There are no over or under bound limit checking and the address pointer will wrap around from FFh to 00h if necessary

TABLE 7-4: BLOCK WRITE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	Repeat N Times		STOP
						Register Data	ACK	
1 → 0	**YYYY_YYY**	**0**	**0**	**XXh**	**0**	**XXh**	**0**	**0 → 1**

7.12 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers, as shown in Table 7-5. It is an extension of the Read Byte Protocol.

TABLE 7-5: BLOCK READ PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK			
1→0	YYYY_YYY	0	0	XXh	0			
START	**Slave Address**	**RD**	**ACK**	**Repeat N Times**		**Register Data**	**NACK**	**STOP**
				Register Data	**ACK**			
1→0	YYYY_YYY	1	0	XXh	0	XXh	1	0 → 1

7.13 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 7-6.

Note: The SMBus Send Byte command is expected to be followed by the SMBus Receive Byte command. When two SMbus Send Byte commands are sent in a row, the first command receives an ACK and will be processed by the UCS2113, but the second command receives a NACK and will be ignored.

TABLE 7-6: SEND BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	STOP
1→0	YYYY_YYY	0	0	XXh	0	0 → 1

7.14 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 7-7.

TABLE 7-7: RECEIVE BYTE PROTOCOL

START	Slave Address	RD	ACK	Register Data	NACK	STOP
1→0	YYYY_YYY	1	0	XXh	1	0 → 1

7.14.1 STAND-ALONE OPERATING MODE

Stand-Alone mode allows the UCS2113 to operate without active SMBus/I^{2}C communications. Stand-Alone mode can be enabled by connecting a pull-down resistor greater or equal to 47 kΩ on the COMM_ILIM pin as shown in Table 5-3.The SMCLK pin should be tied to ground in this mode.

NOTES:

8.0 REGISTER DESCRIPTION

The registers shown in Table 8-1 are accessible through the SMBus or I^2C. An entry of '—' indicates that the bit is not used. Writing to these bits will have no effect and reading these bits will return '0'. Writing to a reserved bit may cause unexpected results and reading from a reserved bit will return either '1' or '0' as indicated in the bit description. While in the Sleep state, the UCS2113 will retain configuration and charge rationing data as indicated in the text. If a register does not indicate that data will be retained in the Sleep power state, this information will be lost when the UCS2113 enters the Sleep power state.

TABLE 8-1: REGISTER SET IN HEXADECIMAL ORDER

Register Address	Register Name	R/W	Function	Default Value	Page No.
00h	Port 1 Current Measurement	R	Stores the current measurement for Port 1	00h	38
01h	Port 2 Current Measurement	R	Stores the current measurement for Port 2	00h	38
02h	Port Status	R	Indicates Port and general status	00h	39
03h	Interrupt Status1	See Text	Indicates why ALERT# pin asserted for Port 1	00h	40
04h	Interrupt Status2	See Text	Indicates why ALERT# pin asserted for Port 2	00h	42
0Fh	General Status1	R/R-C	Indicates General Status for Port 1	00h	44
10h	General Status2	R/R-C	Indicates General Status for Port 2	00h	45
11h	General Configuration1	R/W	Controls basic functionality for Port 1	06h	46
12h	General Configuration2	R/W	Controls basic functionality for Port 2	02h	47
13h	General Configuration3	R/W	Controls other functionality	60h	48
14h	Current Limit	R/W	Controls/Displays MAX Current Limit per port	00h	49
15h	Auto-Recovery Configuration	R/W	Controls the Auto-Recovery functionality	2Ah	50
16h	Port 1 Total Accumulated Charge High Byte	R	Stores the total accumulated charge delivered high byte, Port 1	00h	51
17h	Port 1 Total Accumulated Charge Middle High Byte	R	Stores the total accumulated charge delivered middle high byte, Port 1	00h	51
18h	Port 1 Total Accumulated Charge Middle Low Byte	R	Stores the total accumulated charge delivered middle low byte, Port 1	00h	51
19h	Port 1 Total Accumulated Charge Low Byte	R	Stores the total accumulated charge delivered low byte, Port 1	00h	51
1Ah	Port 2 Total Accumulated Charge High Byte	R	Stores the total accumulated charge delivered high byte, Port 2	00h	52
1Bh	Port 2 Total Accumulated Charge Middle High Byte	R	Stores the total accumulated charge delivered middle high byte, Port 2	00h	52
1Ch	Port 2 Total Accumulated Charge Middle Low Byte	R	Stores the total accumulated charge delivered middle low byte, Port 2	00h	52
1Dh	Port 2 Total Accumulated Charge Low Byte	R	Stores the total accumulated charge delivered low byte, Port 2	00h	52
1Eh	Port 1 Charge Rationing Threshold High Byte	R/W	Sets the maximum allowed charge that will be delivered to Port 1	FFh	53
1Fh	Port 1 Charge Rationing Threshold Low Byte	R/W	Sets the maximum allowed charge that will be delivered to Port 1	FFh	53
20h	Port 2 Charge Rationing Threshold High Byte	R/W	Sets the maximum allowed charge that will be delivered to Port 2	FFh	53

TABLE 8-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	Register Name	R/W	Function	Default Value	Page No.
21h	Port 2 Charge Rationing Threshold Low Byte	R/W	Sets the maximum allowed charge that will be delivered to Port 2	FFh	53
22h	Ration Configuration	R/W	Controls Charge Ration Functionality	11h	54
23h	Port 1 Current Limit Behavior	R/W	Controls the Current Limiting Behavior (CC Mode Region 2) for Port 1	96h	55
24h	Port 2 Current Limit Behavior	R/W	Controls the Current Limiting Behavior (CC Mode Region 2) for Port 2	96h	55
FDh	Product ID	R	Stores a fixed value that identifies each product	E1h	56
FEh	Manufacturer ID	R	Stores a fixed value that identifies Microchip	5Dh	56
FFh	Revision	R	Stores a fixed value that represents the revision number	81h	57

8.1 Current Measurement Register

The Current Measurement register stores the measured current value delivered to the portable device (I_{BUS}). This value is updated continuously while the device is in the Active power state.

REGISTER 8-1: PORTS 1 AND 2 CURRENT MEASUREMENT REGISTERS (ADDRESSES 00H, 01H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CM(x)<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CM(x)<7:0>:** Port X Current Measurement, where x=1 or 2 (address 00h for Port 1 and address 01h for Port 2).

Note 1: The bit weights are in mA,1 LSB = 13.3 mA (maximum value is 255 LSB corresponding to 3.4A).

2: This data will be cleared when the device enters the Sleep state. This data will also be cleared whenever the port power switch is turned off (or any time that V_{BUS} is discharged).

8.2 Status Registers

The Status registers store bits that indicate the state of the ALERT# pins and if the ports operate in Constant Current Mode.

REGISTER 8-2: PORT STATUS REGISTER (ADDRESS 02H)

R-0	R-0	R-0	R-0	U-0	U-0	R-x	R-x
ALERT2_PIN	ALERT1_PIN	CC_MODE2	CC_MODE1	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ALERT2_PIN:** Reflects the status of the ALERT#2 pin. This bit is set and cleared as the ALERT#2 pin changes states.
1 = ALERT#2 Pin asserted (logic low)
0 = ALERT#2 Pin not asserted

bit 6 **ALERT1_PIN:** Reflects the status of the ALERT#1 pin. This bit is set and cleared as the ALERT#1 pin changes states.
1 = ALERT#1 Pin asserted (logic low)
0 = ALERT#1 Pin not asserted

bit 5 **CC_MODE2:** Port 2 Constant Current Mode State
1 = Port 2 in Constant Current mode
0 = Port 2 operating normally

bit 4 **CC_MODE1:** Port 1 Constant Current Mode State
1 = Port 1 in Constant Current mode
0 = Port 1 operating normally

bit 3-0 **Unimplemented**

REGISTER 8-3: INTERRUPT STATUS 1 REGISTER (ADDRESS 03H)

R/W-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
ERR1	DISCH_ERR1	RESET	KEEP_OUT1	TSD_HIGH	OV_VOLT	BACK_V1	OV_LIM1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ERR1:** Error Port 1 - Indicates that an error was detected on the V_{BUS1} pin and the device has entered the Error state. Writing this bit to '0' will clear the Error state and allows the device to be returned to the Active state. When written to '0', all error conditions are checked. If all error conditions have been removed, the UCS2113 returns to the Active state. This bit is set automatically by the UCS2113 when the Error state is entered. If any other bit is set in the Interrupt Status register (03h), the device will not leave the Error state.

This bit is cleared automatically by the UCS2113 if the Auto-recovery fault handling functionality is active and no error conditions are detected. Likewise, this bit is cleared when the PWR_EN1 control is disabled (Note 1).

1 = Port 1 in Error State
0 = Port 1 in Active State (no errors detected)

bit 6 **DISCH_ERR1:** Discharge Error Port 1 - Indicates the device was unable to discharge Port1. This bit will be cleared when read if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT#1 pin to be asserted and the device to enter the Error state.

1 = UCS2113 was unable to Discharge V_{BUS1}
0 = No V_{BUS1} discharge error

bit 5 **RESET:** Indicates that the UCS2113 has just been reset and should be reprogrammed. This bit will be set at power-up. This bit is cleared when read or when the PWR_EN control is toggled. The ALERT# pins are not asserted when this bit is set. This data is retained in the Sleep state.

1 = UCS2113 has just been reset
0 = Reset did not occur

bit 4 **KEEP_OUT1:** Port 1 Minimum Keep-Out region - Indicates that the V-I output on the V_{BUS1} pin has dropped below V_{BUS_MIN}. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1 pin to be asserted and the device to enter the Error state.

1 = $V_{BUS1} < V_{BUS\_MIN}$
0 = $V_{BUS1} > V_{BUS\_MIN}$

bit 3 **TSD_HIGH:** Indicates that the internal temperature has exceeded T_{TSD_HIGH} threshold and the device has entered the Error state. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1and ALERT#2 pins to be asserted and the device to enter the Error state.

1 = Internal die temperature has exceeded T_{TSD_HIGH}
0 = Internal die temperature has not exceeded T_{TSD_HIGH}

bit 2 **OV_VOLT:** V_S Overvoltage indicates that the V_S voltage has exceeded the V_{S_OV} threshold, and the device has entered the Error state. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1 and ALERT#2 pins to be asserted and the device to enter the Error state.

1 = $V_S > V_{S\_OV}$
0 = $V_S < V_{S\_OV}$

REGISTER 8-3: INTERRUPT STATUS 1 REGISTER (ADDRESS 03H) (CONTINUED)

bit 1 **BACK_V1:** Back-Bias Voltage Port 1 - Indicates that the V_{BUS1} voltage has exceeded the V_S or V_{DD} voltages by more than 150 mV. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1 pin to be asserted and the device to enter the Error state.

1 = $V_{BUS1} > V_S$, or $V_{BUS1} > V_{DD}$ by more than 150 mV.
0 = V_{BUS1} voltage has not exceeded the V_S and V_{DD} voltages by more than 150 mV.

bit 0 **OV_LIM1:** Over Current Limit Port 1 - Indicates that the I_{BUS} current has exceeded both the I_{LIM} threshold and the I_{BUS_R2MIN} threshold settings for V_{BUS1}. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1 pin to be asserted and the device to enter the Error state.

1 = Current Limit for Port 1 exceeded
0 = Current Limit for Port 1 not exceeded

Note 1: Note that the ERR1 bit does not necessarily reflect the ALERT#1 pin status. The ALERT#1 pin may be cleared or asserted without the ERR1 bit changing states.

REGISTER 8-4: INTERRUPT STATUS 2 REGISTER (ADDRESS 04H)

R/W-0	R/C-0	R-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0
ERR2	DISCH_ERR2	VS_LOW	KEEP_OUT2	TSD_LOW	—	BACK_V2	OV_LIM2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ERR2:** Error Port 2 - Indicates that an error was detected on the V_{BUS1} pin and the device has entered the Error state. Writing this bit to a '0' will clear the Error state and allows the device to be returned to the Active state. When written to '0', all error conditions are checked. If all error conditions have been removed, the UCS2113 returns to the Active state. This bit is set automatically by the UCS2113 when the Error state is entered. If any other bit is set in the Interrupt Status register (04h), the device will not leave the Error state. This bit is cleared automatically by the UCS2113 if the auto-recovery fault handling functionality is active and no error conditions are detected. Likewise, this bit is cleared when the PWR_EN2 control is disabled (Note 1).

1 = Port 2 in Error State
0 = Port 2 in Active State (no errors detected)

bit 6 **DISCH_ERR2:** Discharge Error Port 2 - Indicates the device was unable to discharge Port2. This bit will be cleared when read if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT#2 pin to be asserted and the device to enter the Error state.

1 = Device was unable to Discharge V_{BUS2}
0 = No V_{BUS2} discharge error

bit 5 **VS_LOW:** Indicates that the V_S voltage has fallen below the V_{S_UVLO} threshold and both V_{BUS1} and V_{BUS2} port power switches are held off. This bit is cleared automatically when the V_S voltage is above the V_{S_UVLO} threshold.

1 = V_S voltage has fallen below the V_{S_UVLO}
0 = V_S voltage is above V_{S_UVLO}

bit 4 **KEEP_OUT2:** Port 2 Minimum Keep-out region - Indicates that the V-I output on the V_{BUS2} pin has dropped below V_{BUS_MIN}. This bit will be cleared when read if the error condition has been removed or if the ERR2 bit is cleared. This bit will cause the ALERT#2 pin to be asserted and the device to enter the Error state.

1 = $V_{BUS2} < V_{BUS\_MIN}$
0 = $V_{BUS2} > V_{BUS\_MIN}$

bit 3 **TSD_LOW**: Indicates that the die temperature has exceeded the T_{TSD_LOW} threshold and it is still above the $T_{TSD\_LOW} - T_{TSD\_LOW\_HYST}$. This bit is cleared automatically when the die temperature is below the $T_{TSD\_LOW} - T_{TSD\_LOW\_HYST}$. This bit will not cause the corresponding ALERT#1 and/or ALERT#2 pins to be asserted and ERR1 and/or ERR2 bits to be set unless:

- a power switch operates in constant current mode
- PWR_EN1 and/or PWR_EN2 controls transition from inactive to active
- it is a power up situation and PWR_EN1 and/or PWR_EN2 pins are active.

1 = Internal die temperature has exceeded T_{TSD_LOW}
0 = Internal die temperature has not exceeded T_{TSD_LOW}

bit 2 **Unimplemented:** Read as '0'

bit 1 **BACK_V2:** Back-Bias Voltage Port 2 - Indicates that the V_{BUS2} voltage has exceeded the V_S or V_{DD} voltages by more than 150 mV. This bit will be cleared when read if the error condition has been removed or if the ERR2 bit is cleared. This bit will cause the ALERT#2 pin to be asserted and the device to enter the Error state.

1 = $V_{BUS2} > V_S$, or $V_{BUS2} > V_{DD}$ by more than 150 mV
0 = V_{BUS2} voltage has not exceeded the V_S and V_{DD} voltages by more than 150 mV

REGISTER 8-4: INTERRUPT STATUS 2 REGISTER (ADDRESS 04H) (CONTINUED)

bit 0 **OV_LIM2:** Overcurrent Limit Port 2 - Indicates that the I_{BUS} current has exceeded both the I_{LIM} threshold and the I_{BUS_R2MIN} threshold settings for V_{BUS2}. This bit will be cleared when read if the error condition has been removed or if the ERR2 bit is cleared. This bit will cause the ALERT#2 pin to be asserted and the device to enter the Error state.

1 = Current Limit for Port 2 exceeded
0 = Current Limit for Port 2 not exceeded

Note 1: Note that the ERR2 bit does not necessarily reflect the ALERT#2 pin status. The ALERT#2 pin may be cleared or asserted without the ERR2 bit changing states.

REGISTER 8-5: GENERAL STATUS 1 REGISTER (ADDRESS 0FH)

R/C-0	U-x	U-x	R-0	R-0	U-x	U-x	U-x
RATION1	—	—	CC_MODE1	PWR_EN1_CON	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **RATION1:** Indicates the state of Port 1 Rationing. This bit is cleared when read, or cleared automatically when the RATION_RST1 bit is set or the RATION_EN1 bit is cleared.
1 = Port 1 has delivered the programmed mAh of current
0 = Port 1 has not delivered the programmed mAh of current

bit 6-5 **Unimplemented**

bit 4 **CC_MODE1:** Indicates whether Port 1 has entered CC mode.
1 = Port 1 is in CC mode
0 = Port 1 not in CC mode

bit 3 **PWR_EN1_CON:** Reflects the PWR_EN control state. This bit is set and cleared automatically with the logic expression (PWR_EN1 pin OR PWR_EN1S).
1 = Port 1 Power Enable is set
0 = Port 1 Power Enable is clear

bit 2-0 **Unimplemented**

REGISTER 8-6: GENERAL STATUS 2 REGISTER (ADDRESS 10H)

R/C-0	U-x	U-x	R-0	R-0	U-x	U-x	U-x
RATION2	—	—	CC_MODE2	PWR_EN2_CON	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **RATION2:** Indicates the state of Port 2 Rationing. This bit is cleared when read, or cleared automatically when the RATION_RST2 bit is set or the RATION_EN2 bit is cleared.

1 = Port 2 has delivered the programmed mAh of current
0 = Port 2 has not delivered the programmed mAh of current

bit 6-5 **Unimplemented**

bit 4 **CC_MODE2:** Indicates whether Port 2 has entered CC mode.

1 = Port 2 is in CC mode
0 = Port 2 not in CC mode

bit 3 **PWR_EN2_CON:** Reflects the PWR_EN control state. This bit is set and cleared automatically with the logic expression (PWR_EN2 pin OR. PWR_EN2S).

1 = Port 2 Power Enable is set
0 = Port 2 Power Enable is clear

bit 2-0 **Unimplemented**

8.3 Configuration Registers

The Configuration registers control basic device functionality. The contents of these registers are retained in Sleep.

REGISTER 8-7: GENERAL CONFIGURATION 1 REGISTER (ADDRESS 11H)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	U-1	U-0
ALERT1_MASK	—	DSCHG1	PWR_EN1S	DISCHG_TIME<1:0>		—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ALERT1_MASK:** Mask errors for all interrupts in Register 8-3 except OV_LIM1 and TSD.
1 = The ALERT#1 pin will only assert if a OV_LIM1 or TSD is detected
0 = The ALERT#1 pin will be asserted if an error condition or indicator event is detected

bit 6 **Unimplemented**

bit 5 **DSCHG1:** Forces the VBUS1 to be reset and discharged when the UCS2113 is in the Active state and the EN_VBUS_DISCHG bit is logic '1'. Writing this bit to a logic '1' will cause the port power switch to be opened and the discharge circuitry to activate and discharge V_{BUS}. Actual discharge time is controlled by DISCHG_TIME<1:0>. This bit must be cleared by the SMBus master after the forced VBUS discharge.
1 = V_{BUS1} discharge initiated
0 = Port 1 not in discharge

bit 4 **PWR_EN1S:** Power Enable Port 1 override - This bit is OR'ed with the PWR_EN1 pin. Thus, if the polarity is set to active-high, either the PWR_EN1 pin or this bit must be '1' to enable the port power switch.

bit 3-2 **DISCHG_TIME<1:0>:** Discharge time Port 1 - sets $t_{DISCHARGE}$. The discharge time value is the same for both ports.
00 = 100 ms
01 = 200 ms
10 = 300 ms
11 = 400 ms

bit 1-0 **Unimplemented**

REGISTER 8-8: GENERAL CONFIGURATION 2 REGISTER (ADDRESS 12H)

R/W-0	U-0	R/W-0	R/W-0	U	R/W-0	U-1	U-0
ALERT2_MASK	—	DSCHG2	PWR_EN2S	—	EN_VBUS_DISCHG	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ALERT2_MASK:** Mask errors for all interrupts in Register 8-4 except OV_LIM2 and TSD.

1 = The ALERT#2 pin will only assert if a OV_LIM2 or TSD is detected
0 = The ALERT#2 pin will be asserted if an error condition or indicator event is detected

bit 6 **Unimplemented**

bit 5 **DSCHG2:** Forces the VBUS2 to be reset and discharged when the UCS2113 is in the Active state and the EN_VBUS_DISCHG bit is logic '1'. Writing this bit to a logic '1' will cause the port power switch to be opened and the discharge circuitry to activate to discharge V_{BUS}. Actual discharge time is controlled by DISCHG_TIME<1:0>. This bit must be cleared by the SMBus master after the forced VBUS discharge.

1 = V_{BUS2} discharge initiated
0 = Port 2 not in discharge

bit 4 **PWR_EN2S:** Power Enable Port 2 override - This bit is OR’ed with the PWR_EN2 pin. Thus, if the polarity is set to active-high, either the PWR_EN2 pin or this bit must be ‘1’ to enable the port power switch.

bit 3 **Unimplemented**

bit 2 **EN_VBUS_DISCHG**: Enables V_{BUS} discharge circuitry.

If it is '0', it completely disables all the automatic V_{BUS} discharges from happening and allows only manual VBUS discharges (the SMBus master must set and clear DISCHG_LOAD1 and DISCHG_LOAD2 bits from the Current Limit Behavior Registers 23h and 24h). Setting DSCHG1 and DSCHG2 bits from the General Configuration 1 and 2 registers 11h and 12h does not have any effect in this case (Note 1).

If it is '1', the V_{BUS} is discharged automatically as described in Section 6.4, V_{BUS} Discharge. The VBUS can be discharged manually by the SMBus master only by setting DSCHG1 and DSCHG2 bits from the General Configuration 1 and 2 Registers 11h and 12h. Setting DISCHG_LOAD1 and DISCHG_LOAD2 bits from the Current Limit Behavior Registers 23h and 24h doesn't have any effect in this case.

bit 1-0 **Unimplemented**

Note 1: When the automatic VBUS discharges are disabled (EN_VBUS_DISCHG is '0'), the UCS2113 will not check that the VBUS voltage is below the VTEST level after the manual VBUS discharges.

REGISTER 8-9: GENERAL CONFIGURATION 3 REGISTER (ADDRESS 13H)

R/W-0	U-1	R/W-1	U-x	U-x	R/W-0	U-0	U-0
PIN_IGN	—	DIS_TO	—	—	BOOST	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **PIN_IGN:** Ignores the PWR_EN1 and PWR_EN2 pin states when determining the power state. This bit is retained in Sleep.
1 = PWR_EN1 and PWR_EN2 pin states are ignored.
0 = Power state is determined by the OR'd combination of the PWR_EN1 and PWR_EN2 pins states and the corresponding PWR_EN1S and PWR_EN2S bit states.

bit 6 **Unimplemented**

bit 5 **DIS_TO:** Disable Time Out - Disables the SMBus time out feature.
1 = Time out disabled
0 = Time out enabled

bit 4-3 **Unimplemented**

bit 2 **BOOST:** Indicates that the I_{BUS} current is higher than I_{BOOST} on V_{BUS1} or V_{BUS2} (bit is OR’ed).
1 = I_{BUS} has exceeded I_{BOOST} on either or both ports
0 = I_{BUS} is less than I_{BOOST} on either port individually

bit 1-0 **Unimplemented:** Read as ‘0’

8.4 Current Limit Register

The Current Limit register controls the I_{LIM} used by the port power switch. The default setting is based on the resistor on the COMM_ILIM pin and this value cannot be changed to be higher than hardware set value. The contents of this register are retained in Sleep.

REGISTER 8-10: CURRENT LIMIT REGISTER (ADDRESS 14H)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ILIM_PORT2<2:0>			ILIM_PORT1<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-3 **ILIM_PORT2<2:0>:** Sets the I_{LIM} value for Port 2
000 = 0.53A
001 = 0.96A
010 = 1.07A
011 = 1.28A
100 = 1.6A
101 = 2.13A
110 =2.67A
111 =3.2A

bit 2-0 **ILIM_SW<2:0>:** Sets the I_{LIM} value for Port 1
000 = 0.53A
001 = 0.96A
010 = 1.07A
011 = 1.28A
100 = 1.6A
101 = 2.13A
110 = 2.67A
111 = 3.2A

8.5 Auto-Recovery Register

The contents of this register are retained in Sleep.

The Auto-Recovery Configuration register sets the parameters used when the Auto-Recovery fault handling algorithm is invoked. Once the Auto-Recovery fault handling algorithm has checked the overtemperature and back-drive conditions, it will set the I_{LIM} value to I_{TEST} and then turn on the port power switch and start the t_{TST} timer. If, after the timer has expired, the V_{BUS} voltage is less than V_{TEST}, then it is assumed that a short-circuit condition is present and the Error state is restarted for Auto Recovery.

REGISTER 8-11: AUTO RECOVERY CONFIGURATION REGISTER (ADDRESS 15H)

R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
LATCHS	TCYCLE<2:0>			TTST<1:0>		VTST_SW<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **LATCHS:** Latch Set - Controls the fault-handling routine that is used in the case that an error is detected.
`1` = Error state will be latched. In order for the UCS2113 to return to normal Active state, the ERR bit must be cleared by the user.
`0` = The UCS2113 will automatically retry when an error condition is detected.

bit 6-4 **TCYCLE<2:0>:** Defines the delay (t_{CYCLE}) after the Error state is entered before the Auto-Recovery fault handling algorithm is started as shown below.
`000` = 15 ms
`001` = 20 ms
`010` = 25 ms
`011` = 30 ms
`100` = 35 ms
`101` = 40 ms
`110` = 45 ms
`111` = 50 ms

bit 3-2 **TTST<1:0>:** Retry Duration timer - Sets the t_{TST} as shown below
`00` = 10 ms
`01` = 15 ms
`10` = 20 ms
`11` = 25 ms

bit 1-0 **VTST_SW:** Short-circuit voltage threshold V_{TEST} that must be crossed during retries to declare the short removed
`00` = 250 mV
`01` = 500 mV
`10` = 750 mV
`11` = 1000 mV

8.6 Total Accumulated Charge Registers

The Total Accumulated Charge registers store the total accumulated charge delivered from the V_S source to a portable device. The bit weighting of the registers is given in mA-hrs. The register value is reset to 00_00h only when the RATION_RST bit is set or if the RATION_EN bit is cleared. This value will be retained when the device transitions out of the Active state and resumes accumulation, if the device returns to the Active state and charge rationing is still enabled.

These registers are updated every one (1) second while the UCS2113 is in the Active power state. Every time the value is updated, it is compared against the target value in the Charge Rationing Threshold registers. This data is retained in the Sleep state.

REGISTER 8-12: PORT1 TOTAL ACCUMULATED CHARGE REGISTERS (ADDRESS 16H, 17H, 18H, 19H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC1<25:18>							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC1<17:10>							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC1<9:2>							
bit 15							bit 8

R-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
TAC1<1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-6	**TAC1<25:0>:** Total Accumulated Charge Port 1 - Each LSB of this 26-bit value equals 0.00367 mAh
bit 5-0	**Unimplemented:** Read as ‘0’

REGISTER 8-13: PORT2 TOTAL ACCUMULATED CHARGE REGISTERS (ADDRESS 1AH,1BH,1CH,1DH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC2<25:18>							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC2<17:10>							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC2<9:2>							
bit 15							bit 8

R-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
TAC2<1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-6 **TAC2<25:0>:** Total Accumulated Charge Port 2 - Each LSB of this 26-bit value equals 0.00367 mAh

bit 5-0 **Unimplemented:** Read as ‘0’

8.7 Charge Rationing Threshold Registers

The Charge Rationing Threshold registers set the maximum allowed charge that will be delivered to a portable device. Every time the Total Accumulated Charge registers are updated, the value is checked against this limit. If the value meets or exceeds this limit, the RATION(1/2) bit is set and action taken according to the RATION_BEH1<1:0> and RATION_BEH2<1:0> bits.

REGISTER 8-14: PORT 1 CHARGE RATIONING THRESHOLD REGISTERS (ADDRESS 1EH,1FH)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CT1<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CT1<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CT1<15:0>:** Charge Rationing Threshold Port 1 - Each LSB of this 16-bit value equals 3.76 mAh

REGISTER 8-15: PORT 2 CHARGE RATIONING THRESHOLD REGISTERS (ADDRESS 20H, 21H)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CT2<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CT2<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CT2:** Charge Rationing Threshold Port 2 - Each LSB of this 16-bit value equals 3.76 mAh

REGISTER 8-16: RATION CONFIGURATION REGISTER (ADDRESS 22H)

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
RTN_EN2	RTN_RST2	RTN_BEH2<1:0>		RTN_EN1	RTN_RST1	RTN_BEH1<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **RTN_EN2:** Charge Ration Enable Port 2 - Enables Charge Rationing for Port 2.

1 = Charge Rationing enabled

0 = Charge Rationing disabled. The Total Accumulated Charge registers for Port 2 will be cleared to 00_00h and current data will no longer be accumulated. If the Total Accumulated Charge registers have already reached the Charge Rationing Threshold, the applied response will be removed as if the charge rationing had been reset. This will also clear the RATION2 status bit (if set).

bit 6 **RTN_RST2:** Port 2 Ration Reset - Resets the charge rationing functionality for Port 2.

1 = Total Accumulated Charge registers are reset to 00_00h. In addition, when this bit is set, the RATION2 status bit will be cleared and, if there are no other errors or active indicators, the ALERT#2 pin will be released.

0 = Normal operation. This bit must be cleared to enable charge rationing

bit 5-4 **RTN_BEH2<1:0>:** Ration Behavior Control bits - Controls how the UCS2113 responds when the Ration Threshold has been exceeded (as shown in Table 6-2).

00 = Report
01 = Report and Disconnect
10 = Disconnect and SLEEP
11 = Ignore

bit 3 **RTN_EN1:** Charge Ration Enable Port 1 - Enables Charge Rationing for Port 1.

1 = Charge Rationing enabled

0 = Charge Rationing disabled. The Total Accumulated Charge registers for Port 1 will be cleared to 00_00h and current data will no longer be accumulated. If the Total Accumulated Charge registers have already reached the Charge Rationing Threshold, the applied response will be removed as if the charge rationing had been reset. This will also clear the RATION1 status bit (if set).

bit 2 **RTN_RST1:** Port 1 Ration Reset - Resets the charge rationing functionality for Port 1.

1 = Total Accumulated Charge registers are reset to 00_00h. In addition, when this bit is set, the RATION1 status bit will be cleared and, if there are no other errors or active indicators, the ALERT#1 pin will be released.

0 = Normal operation. This bit must be cleared to enable charge rationing.

bit 1-0 **RTN_BEH1<1:0>:** Ration Behavior Control bits - Controls how the UCS2113 responds when the Ration Threshold has been exceeded (as shown in Table 6-2).

00 = Report
01 = Report and Disconnect
10 = Disconnect and SLEEP
11 = Ignore

8.8 Current Limit Behavior Registers

The Current Limit Behavior register stores the values used by the applied current limiting mode (Trip or CC). The contents of this register are not retained in Sleep.

REGISTER 8-17: PORT 1 CURRENT LIMIT BEHAVIOR REGISTER (ADDRESS 23H)

R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0
SEL_VBUS1_MIN<1:0>		DISCHG_LOAD1	SEL_R2_IMIN1<2:0>			Reserved	Reserved
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **SEL_VBUS1_MIN<1:0>:** Define the V_{BUS_MIN} voltage for Port 1 as follows:
`00` = 1.50V
`01` =1.75V
`10` =2.0V
`11` =2.25V

bit 5 **DISCHG_LOAD1**: Connects the internal 100Ω load to discharge V_{BUS1} (Note 1). The SMBus master must set this bit to discharge V_{BUS1} if the EN_VBUS_DISCHG bit from the General Configuration 2 register 12h is '`0`'. This functionality doesn't use any timer. The discharge time is controlled by the SMBus master, which must clear this bit when its internal timer expires. The difference from DSCHG1 bit from the General Configuration 1 register 11h is that, when that bit is set, the discharge time is controlled by the UCS2113 internal timer.

The state of this bit is ignored when the EN_VBUS_DISCHG bit from the General Configuration 2 register 12h is '`1`'.

bit 4-2 **SEL_R2_IMIN1<2:0>:** Defines the I_{BUS_R2MIN} current
`000` =100 mA
`001` =530 mA
`010` =960 mA
`011` =1280 mA
`100` =1600 mA
`101` =2130 mA

bit 1-0 **Reserved:** Do not change

Note 1: If the corresponding power switch is still turned on (PWR_EN1 control is active) while DISCHG_LOAD1 bit is set, the internal 100Ω load will be connected in parallel with the load on the VBUS1 pins.

REGISTER 8-18: PORT 2 CURRENT LIMIT BEHAVIOR REGISTER (ADDRESS 24H)

R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0
SEL_VBUS2_MIN<1:0>		DISCHG_LOAD2	SEL_R2_IMIN2_MIN<2:0>			Reserved	Reserved
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **SEL_VBUS2_MIN<1:0>:** Define the V_{BUS_MIN} voltage for Port 2 as follows:
`00` = 1.50V
`01` =1.75V
`10` =2.0V
`11` =2.25V

REGISTER 8-18: PORT 2 CURRENT LIMIT BEHAVIOR REGISTER (ADDRESS 24H) (CONTINUED)

bit 5	**DISCHG_LOAD2**: Connects the internal 100Ω load to discharge V_{BUS2} (Note 1). The SMBus master must set this bit to discharge V_{BUS2} if the EN_VBUS_DISCHG bit from the General Configuration 2 register 12h is '0'. This functionality doesn't use any timer. The discharge time is controlled by the SMBus master, which must clear this bit when its internal timer expires. The difference from DSCHG2 bit from the General Configuration 2 register 12h is that, when that bit is set, the discharge time is controlled by the UCS2113 internal timer. The state of this bit is ignored when the EN_VBUS_DISCHG bit from the General Configuration 2 register 12h is '1'.
bit 4-2	**SEL_R2_IMIN2_MIN<2:0>:** Defines the I_{BUS_R2MIN} current 000 =100 mA 001 =530 mA 010 =960 mA 011 =1280 mA 100 =1600 mA 101 =2130 mA
bit 1-0	**Reserved**: Do not change

Note 1: If the corresponding power switch is still turned on (PWR_EN2 control is active) while DISCHG_LOAD2 bit is set, the internal 100Ω load will be connected in parallel with the load on the VBUS2 pins.

8.9 Product ID Register

The Product ID register stores a unique 8-bit value that identifies the UCS device family.

REGISTER 8-19: PRODUCT ID REGISTER (ADDRESS FDH)

R-1	R-1	R-1	R-0	R-0	R-0	R-1	R-0
PID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PID<7:0>:** Product ID for the UCS2113

8.10 Manufacture ID Register

The Manufacturer ID register stores a unique 8-bit value that identifies Microchip Technology Inc.

REGISTER 8-20: MANUFACTURER ID REGISTER (ADDRESS FEH)

R-0	R-1	R-0	R-1	R-1	R-1	R-0	R-1
MID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **MID<7:0>:** Manufacturer ID for Microchip

8.11 Revision Register

The Revision register stores an 8-bit value that represents the part revision.

REGISTER 8-21: REVISION REGISTER (ADDRESS FFH)

R-1	R-0	R-0	R-0	R-0	R-0	R-0	R-1
REV<7:0>							
bit 7							bit 0

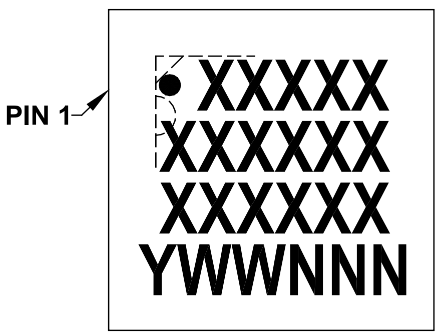
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **REV<7:0>:** Part Revision

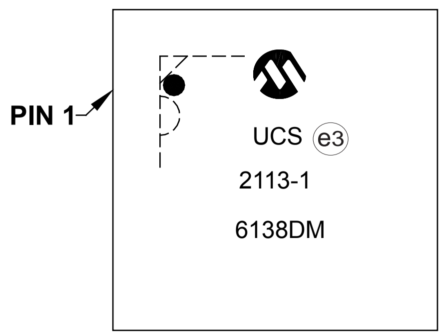
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

4x4 mm QFN, 20-lead

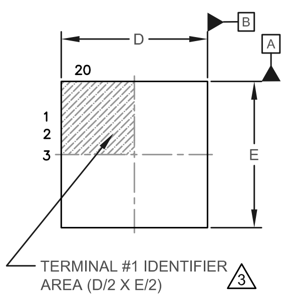


Example

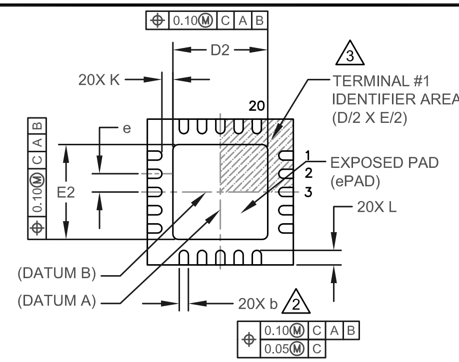


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

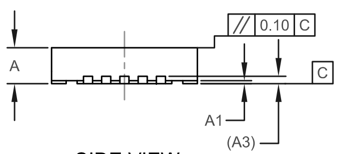
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.



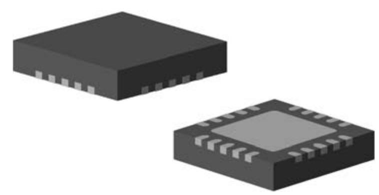
TOP VIEW



BOTTOM VIEW



SIDE VIEW

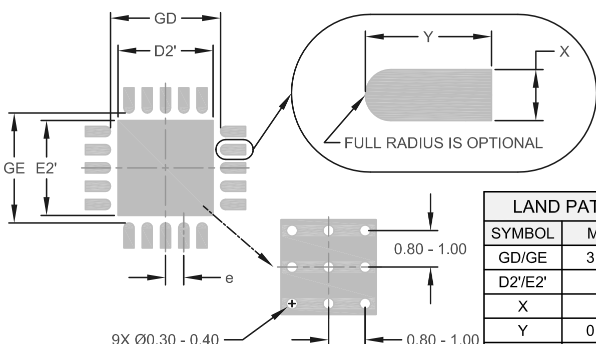


3-D VIEWS

REVISION HISTORY			
REVISION	DESCRIPTION	DATE	RELEASED BY
A	INITIAL PRELIMINARY RELEASE	3/18/07	S.K.ILIEV
B	INITIAL PRODUCTION RELEASE	12/5/07	S.K.ILIEV
C	L from 0.4±0.05 to 0.4±0.1mm. Y from 0.65 to 0.69mm. GD/GE from 3.01 to 3.00. K(min) from 0.2 to 0.25	4/21/08	S.K.ILIEV
D	ADDED GD/GE MAX. Y=0.69 from NOM to MIN	3/8/10	S.K.ILIEV
E	ADDED Y (MAX) = 0.80	3/15/10	S.K.ILIEV
F	ADDED Y CENTER PCB PAD VIA INFORMATION	2/17/12	S.K.ILIEV

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3	0.20 REF			-	LEAD-FRAME THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D2/E2	2.50	2.60	2.70	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
K	0.25	0.30	-	-	TERMINAL TO PAD DISTANCE
e	0.50 BSC			-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.



THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

PCB LAND PATTERN

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	3.00	-	3.10
D2'/E2'	-	2.60	2.60
X	-	0.28	0.28
Y	0.69	-	0.80
e	0.50		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.025
ANGULAR ±1°
INTERPRET DIM AND TOL PER ASME Y14.5M - 1994

THIRD ANGLE PROJECTION

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

	NAME	DATE
MATERIAL: -		
DRAWN	-	3/14/07
FINISH: -		
CHECKED	S.K.ILIEV	3/15/07
APPROVED	S.K.ILIEV	3/18/07

PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

TITLE: PACKAGE OUTLINE
20 PINS SQFN, 4x4mm BODY, 0.5mm PITCH
(SAWN QFN, FULL LEAD TERMINATION)

DWG NUMBER	REV
20SQFN-4x4B-0.5P	F

SCALE	STD COMPLIANCE	SHEET
1:1	JEDEC: MO-220	1 OF 1

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (December 2016)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[T](1)	–X	–X	/XX
Device	Tape and Reel	Version	Temperature Range	Package

Device:	UCS2113:	USB Dual-Port Power Switch and Current Monitor
Version:	1 =	SMBus address 57h
Temperature Range:	V =	-40°C to +105°C (Various)
Package:	G4 =	Plastic Quad Flat No Lead Package - 4x4 mm Body with 0.40 mm Contact Length, Saw Singulated, QFN, 20-lead

Examples:

a) UCS2113-1-V/G4: Various temperature, 20-pin 4x4 QFN package

b) UCS2113T-1-V/G4: Tape and Reel, Various temperature, 20-pin 4x4 QFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

ISBN: 978-1-5224-1240-3

MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-3326-8000
Fax: 86-21-3326-8021

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

France - Saint Cloud
Tel: 33-1-30-60-70-00

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820