2N7639-GA

Normally – OFF Silicon Carbide Junction Transistor

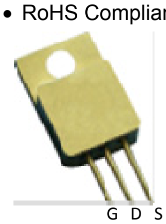
V_{DS}	=	600 V
$V_{DS(ON)}$	=	1.3 V
I_D	=	20 A
$R_{DS(ON)}$	=	65 mΩ

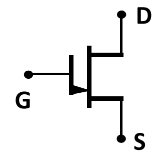
Features

- 250 °C maximum operating temperature
- Temperature independent switching performance
- Electrically isolated base-plate
- Gate oxide free SiC switch
- Suitable for connecting an anti-parallel diode
- Positive temperature coefficient for easy paralleling
- Low gate charge
- Low intrinsic capacitance

Package

- RoHS Compliant





TO – 257 (Isolated Base-plate Hermetic Package)

Advantages

- Low switching losses
- Higher efficiency
- High temperature operation
- High short circuit withstand capability

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Maximum Ratings at T_j = 250 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values	Unit
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	600	V
Continuous Drain Current	I_D	145 °C < T_C < 160 °C	20	A
Gate Peak Current	I_{GM}		5	A
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 250 °C, I_G = 1 A, Clamped Inductive Load	$I_{D,max}$ = 20 @ $V_{DS} \leq V_{DSmax}$	A
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 250 °C, I_G = 2.5 A, V_{DS} = 400 V, Non Repetitive	20	µs
Reverse Gate – Source Voltage	V_{GS}		30	V
Reverse Drain – Source Voltage	V_{DS}		40	V
Power Dissipation	P_{tot}	T_C = 25 °C	22	W
Operating and Storage Temperature	T_j, T_{stg}		-55 to 250	°C

Electrical Characteristics at T_j = 250 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values min.	Values typ.	Values max.	Unit
On Characteristics						
Drain – Source On Voltage	$V_{DS(ON)}$	I_D = 20 A, I_G = 400 mA, T_j = 25 °C I_D = 20 A, I_G = 500 mA, T_j = 125 °C I_D = 20 A, I_G = 1000 mA, T_j = 175 °C I_D = 20 A, I_G = 1000 mA, T_j = 250 °C		1.3 1.8 2.2 3.3		V
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 20 A, I_G = 400 mA, T_j = 25 °C I_D = 20 A, I_G = 500 mA, T_j = 125 °C I_D = 20 A, I_G = 1000 mA, T_j = 175 °C I_D = 20 A, I_G = 1000 mA, T_j = 250 °C		65 91 110 165		mΩ
Gate Forward Voltage	$V_{GS(FWD)}$	I_G = 1000 mA, T_j = 25 °C I_G = 1000 mA, T_j = 250 °C		3.0 2.7		V
DC Current Gain	β	V_{DS} = 5 V, I_D = 20 A, T_j = 25 °C V_{DS} = 5 V, I_D = 20 A, T_j = 125 °C V_{DS} = 5 V, I_D = 20 A, T_j = 175 °C V_{DS} = 5 V, I_D = 20 A, T_j = 250 °C		110 78 73 69		

Off Characteristics

Drain Leakage Current	I_{DSS}	V_R = 600 V, V_{GS} = 0 V, T_j = 25 °C	10	µA
		V_R = 600 V, V_{GS} = 0 V, T_j = 175 °C	50	
		V_R = 600 V, V_{GS} = 0 V, T_j = 250 °C	100	
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C	20	nA

Electrical Characteristics at T_j = 250 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values min.	Values typ.	Values max.	Unit
Capacitance Characteristics						
Gate-Source Capacitance	C_{gs}	V_{GS} = 0 V, f = 1 MHz		2400		pF
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_D = 1 V, f = 1 MHz		3700		pF
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	V_D = 1 V, f = 1 MHz		840		pF
Switching Characteristics						
Turn On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 20 A, V_{GS} = -8/15 V ,T_j = 175 ºC Refer to Figure 15 for gate drive current waveforms		92		ns
Rise Time	t_r			42		ns
Turn Off Delay Time	$t_{d(off)}$			51		ns
Fall Time	t_f			31		ns
Turn-On Energy Per Pulse	E_{on}			811		µJ
Turn-Off Energy Per Pulse	E_{off}			96		µJ
Total Switching Energy	E_{ts}			907		µJ
Turn On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 20 A, V_{GS} = -8/15 V ,T_j = 250 ºC Refer to Figure 15 for gate drive current waveforms		91		ns
Rise Time	t_r			17		ns
Turn Off Delay Time	$t_{d(off)}$			50		ns
Fall Time	t_f			21		ns
Turn-On Energy Per Pulse	E_{on}			100		µJ
Turn-Off Energy Per Pulse	E_{off}			40		µJ
Total Switching Energy	E_{ts}			140		µJ

Thermal Characteristics

Thermal resistance, junction - case	R_{thJC}	1.16	°C/W

Figures

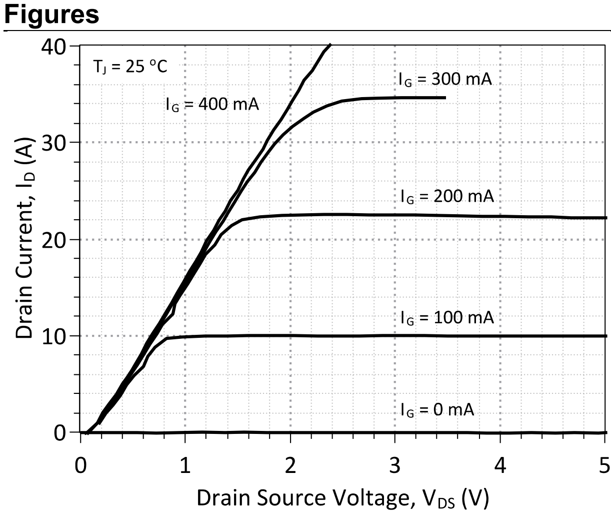


Figure 1: Typical Output Characteristics at 25 °C

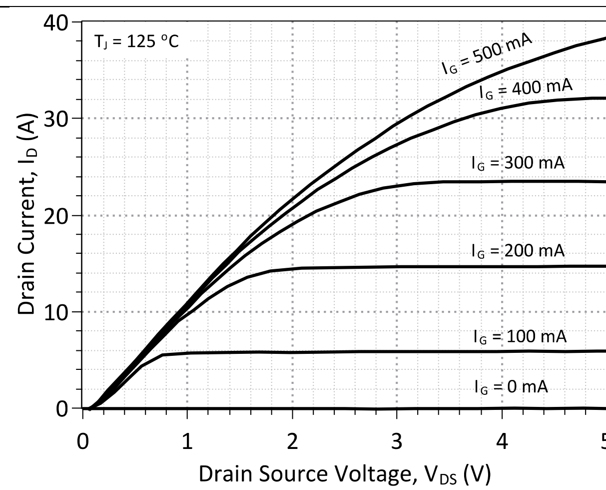


Figure 2: Typical Output Characteristics at 125 °C

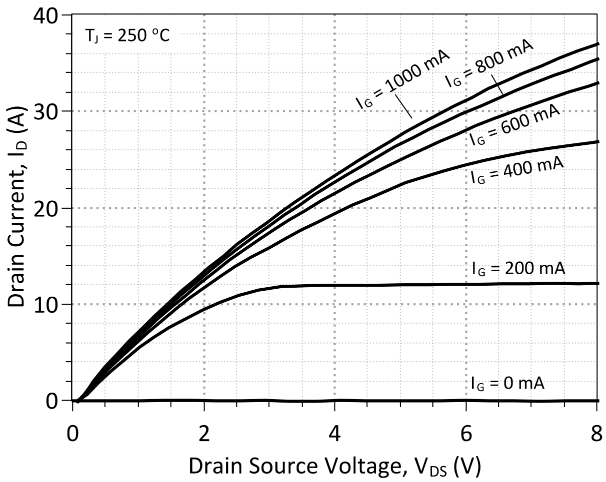


Figure 3: Typical Output Characteristics at 250 °C

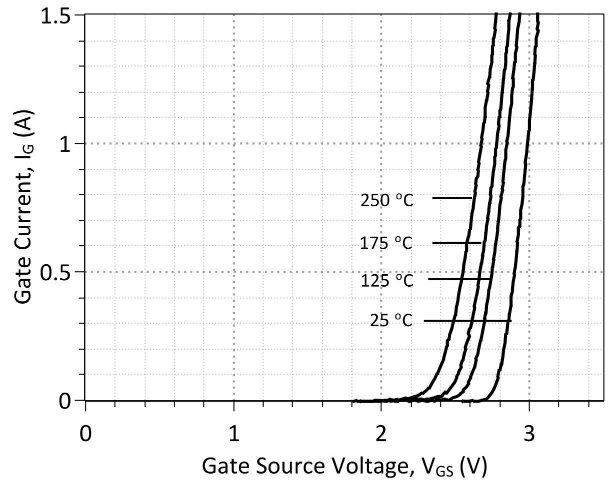


Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

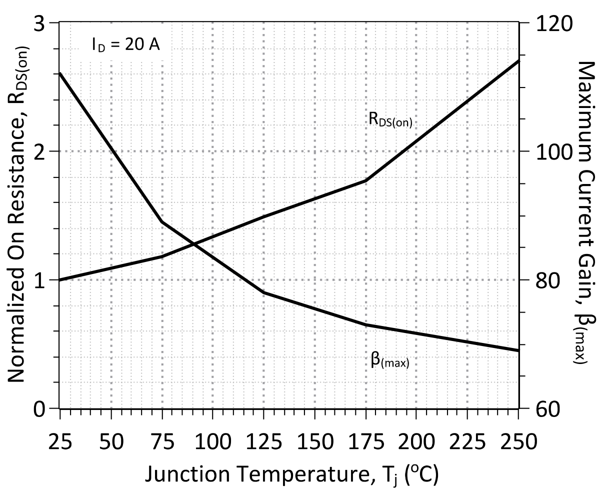


Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

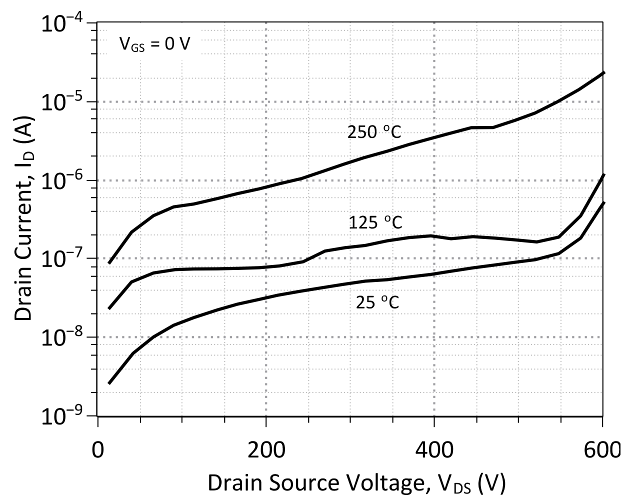


Figure 6: Typical Blocking Characteristics

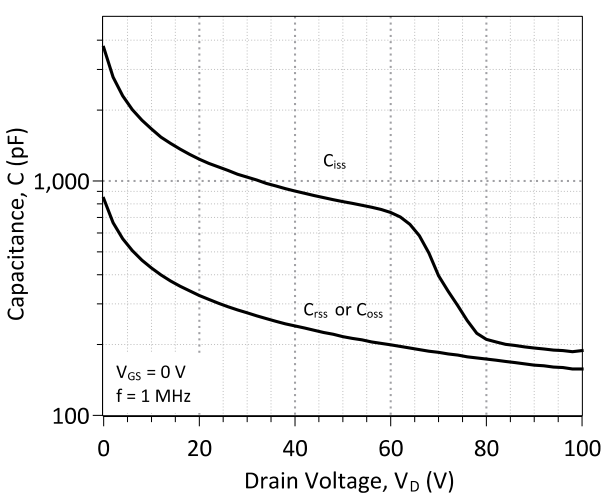


Figure 7: Capacitance Characteristics

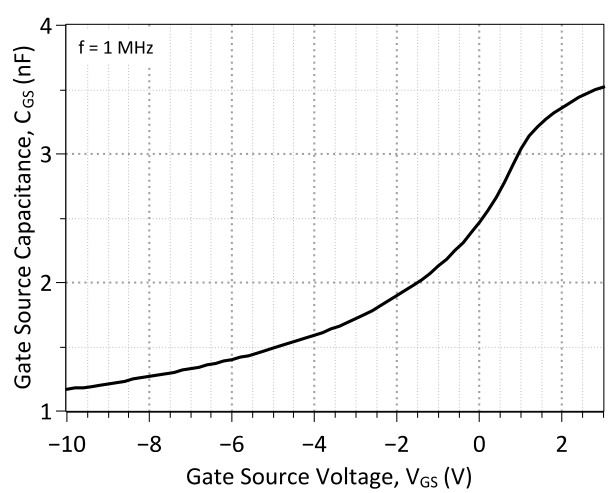


Figure 8: Capacitance Characteristics

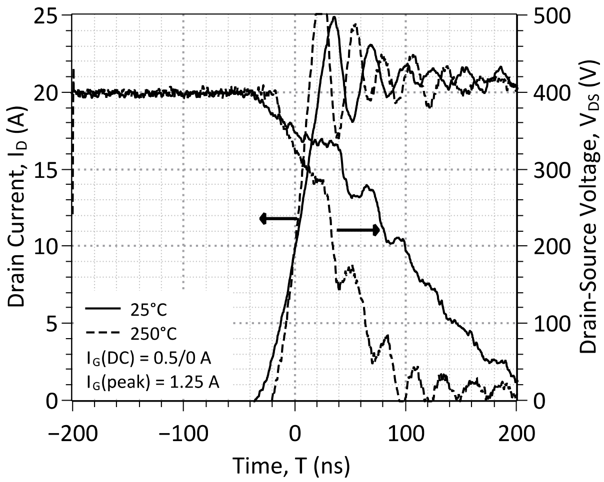


Figure 9: Typical Hard-switched Turn On Waveforms

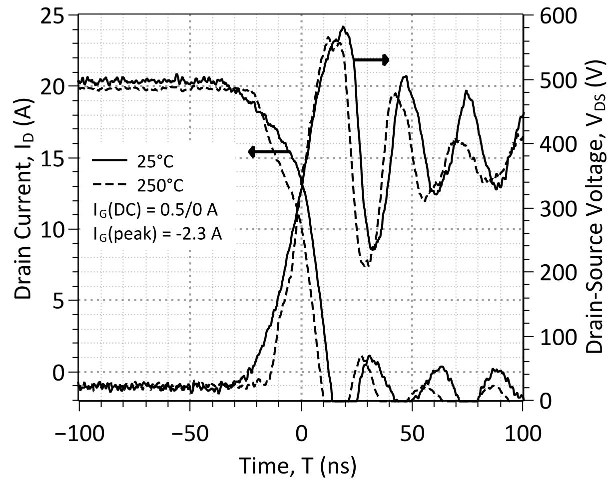


Figure 10: Typical Hard-switched Turn Off Waveforms

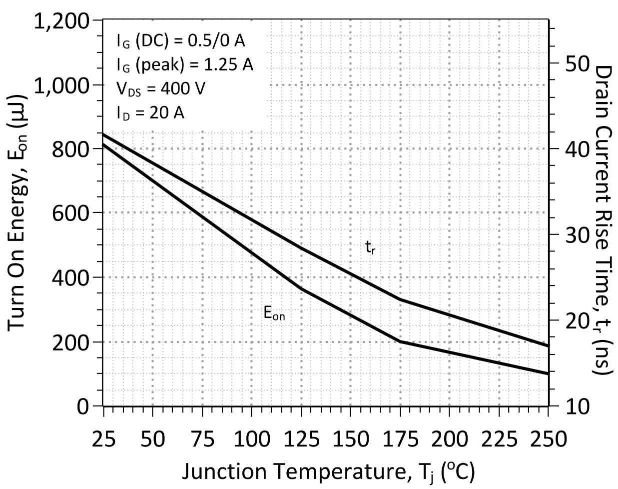


Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

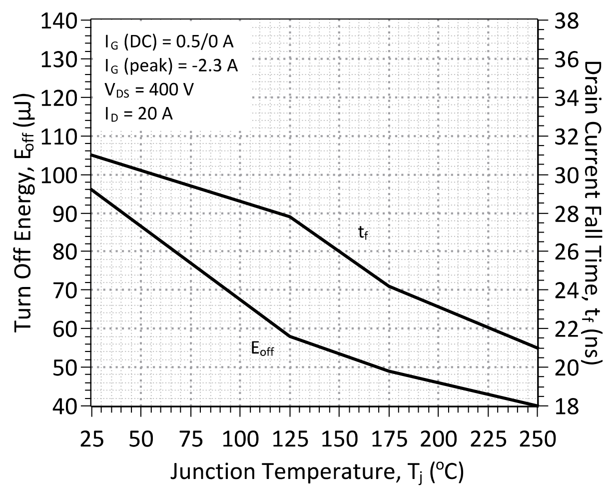


Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

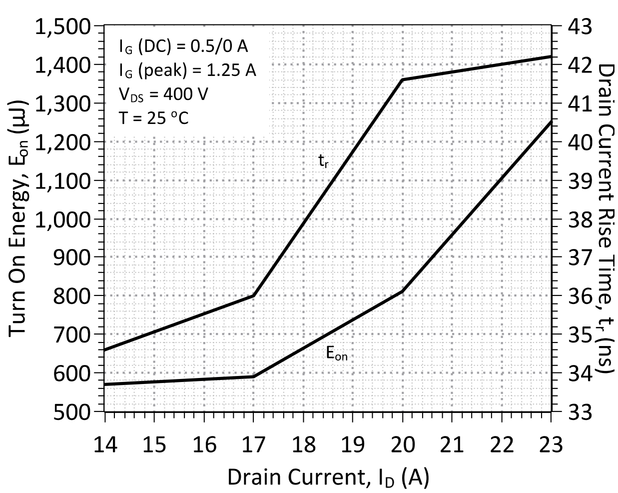


Figure 13: Typical Turn On Energy Losses vs. Drain Current

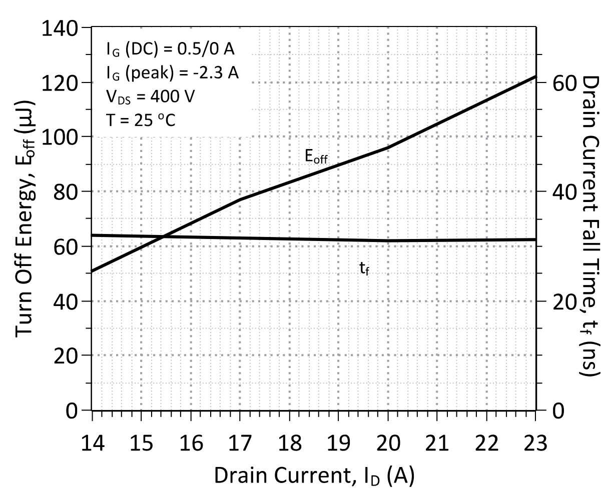


Figure 14: Typical Turn Off Energy Losses vs. Drain Current

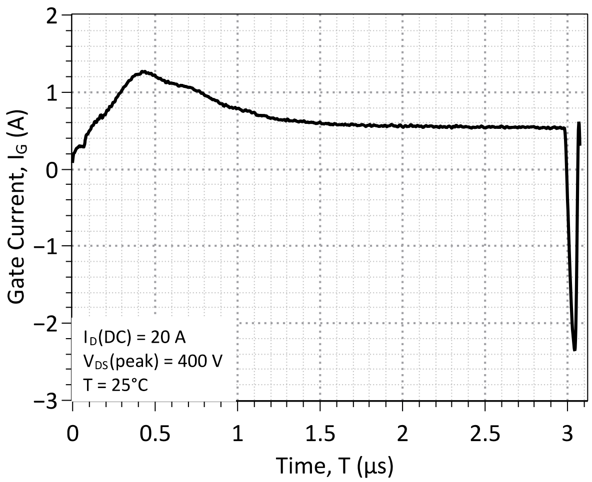


Figure 15: Typical Gate Current Waveform

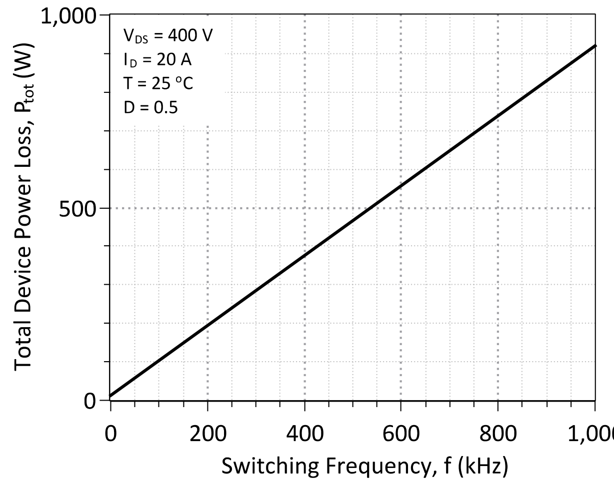


Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency [1]

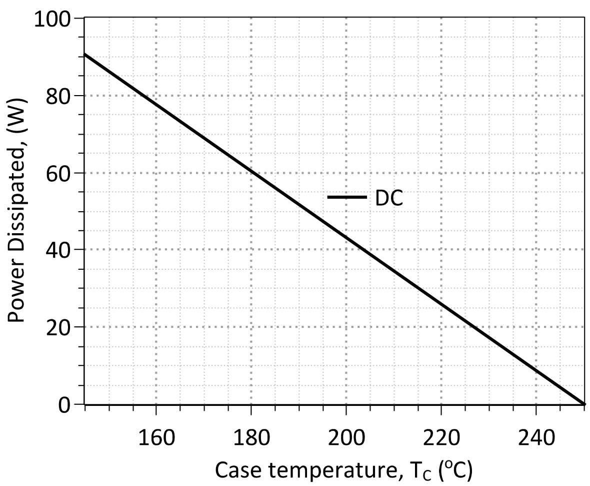


Figure 17: Power Derating Curve

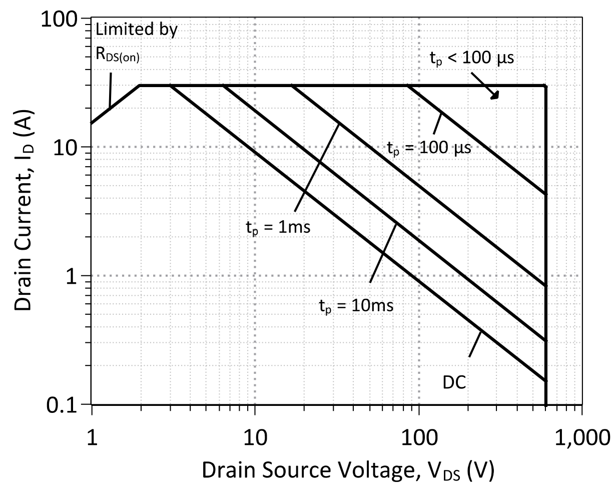


Figure 18: Forward Bias Safe Operating Area at T_c=145 °C

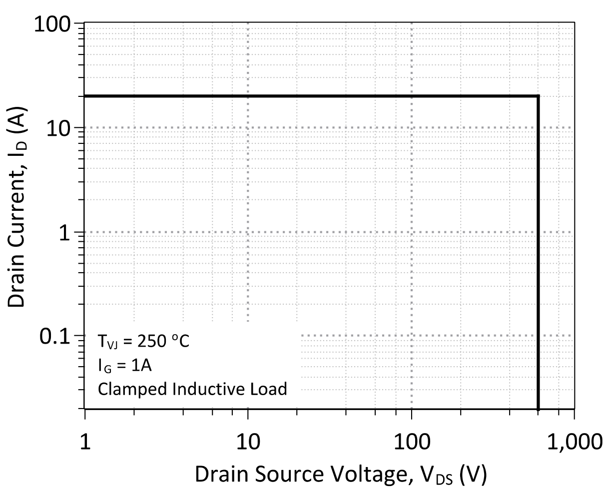


Figure 19: Turn-Off Safe Operating Area

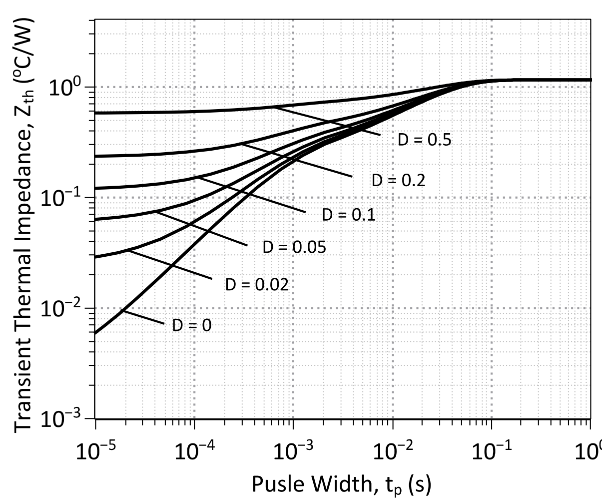


Figure 20: Transient Thermal Impedance

[1] – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

Gate Drive Technique (Option #1)

To drive the 2N7639-GA with the lowest gate drive losses, please refer to the dual voltage source gate drive configuration described in Application Note AN-10B (http://www.genesicsemi.com/index.php/references/notes).

Gate Drive Technique (Option #2)

The 2N7639-GA can be effectively driven using the IXYS IXDN614 / IXDD614 non-inverting gate driver IC **or a comparable product**. A typical gate driver configuration along with component values using this driver is offered below. Additional information is available in GeneSiC Application Note AN-10A and from the manufacturer at www.ixys.com.

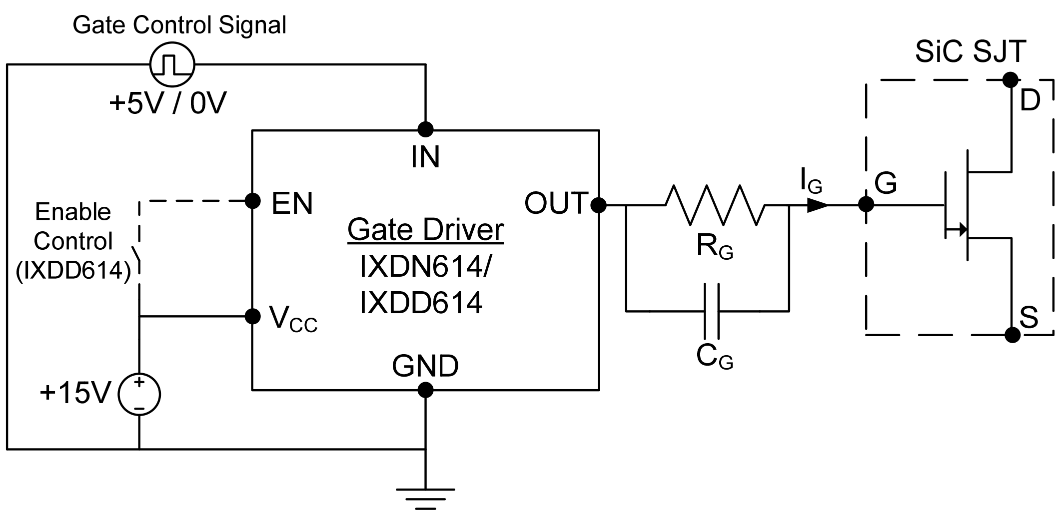
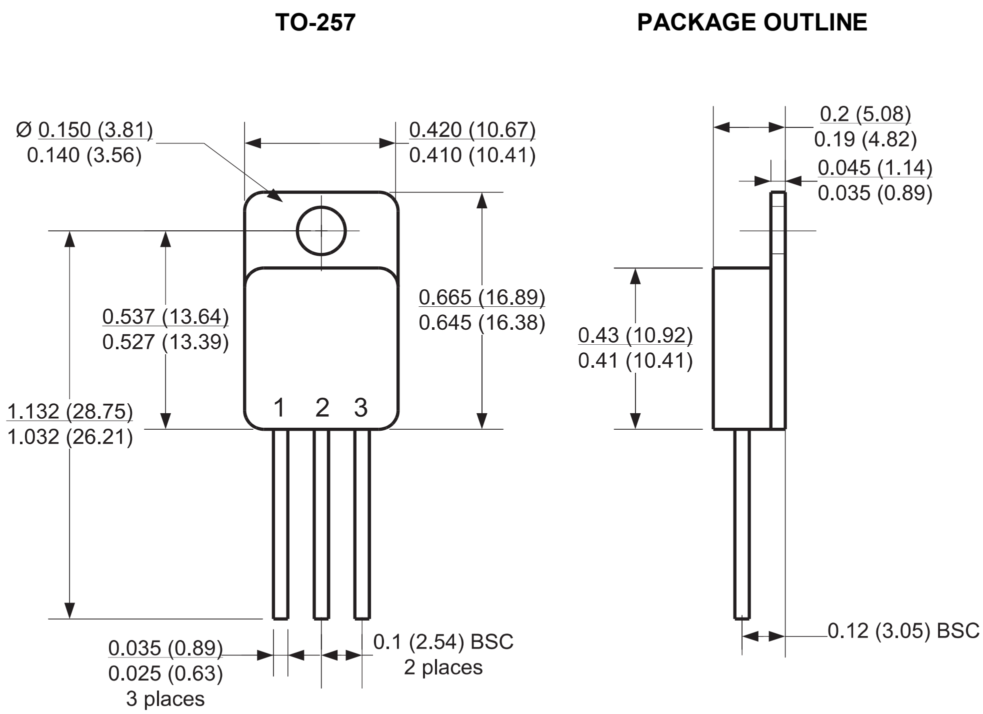


Figure 21: Recommended Gate Diver Configuration (Option #2)

Parameter	Symbol	Conditions	Values min.	Values typ.	Values max.	Unit
Option #1 Gate Drive Conditions (IXDD614/IXDN614)						
Supply Voltage, High Side Driver	V_{CC}	V_{GH}	15	20	30	V
Supply Voltage, Low Side Driver	V_{CC}	V_{GL}	5	6.5		V
Off State Voltage, Both Drivers	GND	V_{EE}		-10	0	V
Gate Control Input Signal, Low	IN		-5.0	0	0.8	V
Gate Control Input Signal, High	IN		4	5.0	V_{CC}+0.3	V
Enable, Low	EN	IXDD614 Only			1/3*V_{CC}	V
Enable, High	EN	IXDD614 Only	2/3*V_{CC}			V
Output Voltage, Low	V_{OUT}				0.025	V
Output Voltage, High	V_{OUT}		V_{CC}-0.025			V
Output Current, Peak	I_{OUT}	Package Limited			14	A
Output Current, Continuous	I_{OUT}			0.5	4.0	A
Passive Gate Components						
Gate Resistance	R_G	V_{GL} = 6.0 V, $I_G \approx$ 0.5 A		1.6	5	Ω
Gate Capacitance	C_G	V_{GH} = 20 V, $I_{G,pk} \approx$ 4.0 A	20	35		nF

Package Dimensions:



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2013/12/09	2	Updated Electrical Characteristics	
2013/11/18	1	Updated Electrical Characteristics	
2012/08/24	0	Initial release	

Published by
GeneSiC Semiconductor, Inc.
43670 Trade Center Place Suite 155
Dulles, VA 20166

SPICE Model Parameters

Copy the following code into a SPICE software program for simulation of the 2N7639-GA device.

```
*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision:   1.0            $
*     $Date:   06-SEP-2013        $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*     http://www.genesicsemi.com/index.php/hit-sic/sjt
*
*     COPYRIGHT (C) 2013 GeneSiC Semiconductor Inc.
*     ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model 2N7639-GA NPN
+ IS       6.03E-47
+ ISE      1.72E-28
+ EG       3.23
+ BF       122
+ BR       0.55
+ IKF      300
+ NF       1
+ NE       1.868
+ RB       0.26
+ RE       0.088
+ RC       0.01
+ CJC      5.68E-10
+ VJC      2.978967839
+ MJC      0.466424924
+ CJE      1.72E-09
+ VJE      2.77859888
+ MJE      0.48415
+ XTI      3
+ XTB      -0.78
+ TRC1     7.00E-02
+ VCEO     600
+ ICRATING 20
+ MFG      GeneSiC_Semiconductor
*
* End of 2N7639-GA SPICE Model
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