

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

Bare Die

OptiMOS™3 Power MOS Transistor Chip IPC042N03L3

Data Sheet

Rev. 2.5 Final



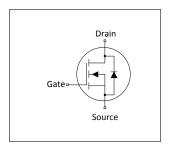
Description 1

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPD040N03LG
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV systemFrontside metallization: AlCu system



| Table 1 1to j 1 di lori la | | | | | |
|--|-------------|-----------------|--|--|--|
| Parameter | Value | Unit | | | |
| $V_{(BR)DSS}$ | 30 | V | | | |
| R _{DS(on)} | 4.01) | m $Ω$ | | | |
| Die size | 2.78 x 1.53 | mm ² | | | |
| Thickness | 175 | μm | | | |









IPC042N03L3



| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|---------|-------------|---------------|
| IPC042N03L3 | Chip | not defined | - |

2 Electrical Characteristics on Wafer Level at $T_j = 25$ °C, unless otherwise specified

Table 2

| Parameter | Symbol | Values | | l lm:4 | Note / Test Condition | |
|----------------------------------|----------------------|--------|-------------------------------------|-----------------------------------|-----------------------|---|
| | | Min. | Тур. | Max. | Unit | Note / Test Condition |
| Drain-source breakdown voltage | V _{(BR)DSS} | 30 | - | - | V | V _{GS} =0 V ,I _D =1 mA |
| Gate threshold voltage | $V_{\rm GS(th)}$ | 1 | - | 2.2 | V | $V_{\rm DS} = V_{\rm GS}, I_{\rm D} = 250 \ \mu {\rm A}$ |
| Zero gate voltage drain current | I _{DSS} | - | - | 1 | μΑ | V _{GS} =0 V , V _{DS} =30 V |
| Gate-source leakage current | I _{GSS} | - | - | 100 | nA | V _{GS} =20 V ,V _{DS} =0 V |
| Drain-source on- resistance | R _{DS(on)} | - | 3.7 ²⁾ 2.3 ²⁾ | 50 ³⁾ 50 ³⁾ | mΩ | V _{GS} =4.5 V ,I _D =2.0 A V _{GS} =10 V ,I _D =2.0 A |
| Reverse diode forward on-voltage | V _{SD} | - | 0.83 | 1.1 | V | V _{GS} =0 V ,I _F =1A |
| Avalanche energy, single pulse | E AS | - | - | 60 | mJ | I _D =50 A, R _{GS} =25 Ω |

 $^{^{1)}}$ packaged in a DPAK using Al bond wire (see ref. product) typical bare die $R_{\rm DS(on)};~V_{\rm GS}$ =10 V when used with 4x500µm Al-wedge double-stitch bonding limited by wafer test-equipment



3 Package Outlines

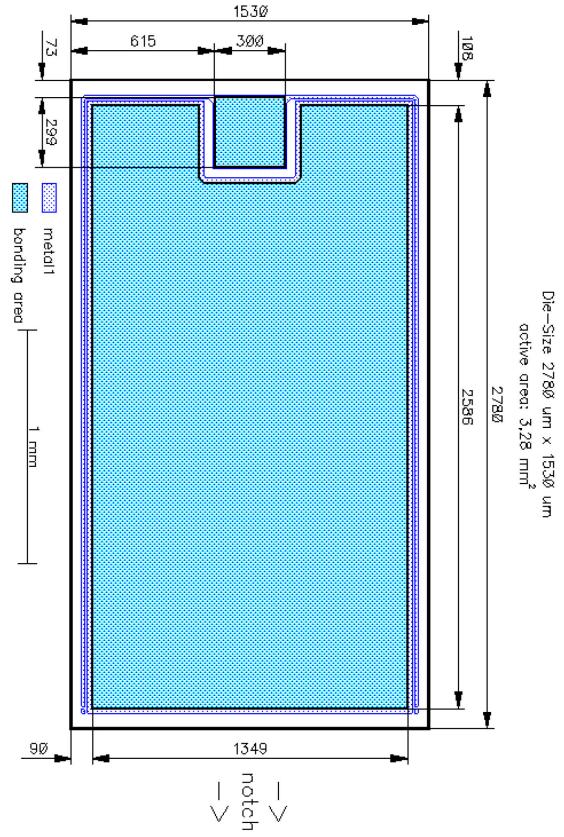


Figure 1 Outline Chip, dimensions in µm



OptiMOS™3 Power MOS Transistor Chip

IPC042N03L3

Revision History

IPC042N03L3

Revision: 2014-07-25, Rev. 2.5

Previous Revision

| Revision | Date | Subjects (major changes since last revision) | | |
|----------|------------|--|--|--|
| 2.5 | 2014-07-25 | Release of Final Version | | |

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