



16-string White & RGB LED Drivers with Adaptive Power Control, E<sup>2</sup>PROM, and SPI/I<sup>2</sup>C/SMBus Serial Interface

# Datasheet Brief



### **General Description**

The Atmel LED Drivers-MSL3163 and MSL3164 compact, high-power LED string drivers use internal current control MOSFETs to sink up to 100mA per string, with current accuracy and matching better than 3%. The MSL3163/4 drive 16 parallel strings of ten white LEDs each, for a total of 160 white LEDs per device. Sixteen interconnected devices control up to 2560 white LEDs.

# Atmel LED Drivers-MSL3163 and MSL3164

16-string White & RGB LED Drivers with Adaptive Power Control, E<sup>2</sup>PROM, and SPI/I<sup>2</sup>C/SMBus Serial Interface

The MSL3163/4 adaptively controls the DC-DC converters that power the LED strings, using Atmel's Adaptive SourcePower technology. These Efficiency Optimizers minimize power use while maintaining LED current accuracy.

The MSL3164 features a 20 MHz SPI serial interface, and the MSL3163 offers a 1 MHz I<sup>2</sup>C serial interface. Both interfaces support video frame-by-frame LED string intensity control for up to 16 interconnected devices to allow active area dimming. The devices include an advanced PWM engine that easily synchronizes to a video signal, and per-string phase adjustment to reduce unwanted LCD artifacts such as motion blur. Additionally, an on-chip E<sup>2</sup>PROM allows the power-up defaults to be customized through the serial interface.

A unique combination of peak current control and pulse width management offer simple full screen brightness control, versatile area dimming and a consistent white point. One external resistor provides the global peak reference current for all LED strings, and global peak current fine-tuning is available through an 8-bit register. Global string drive pulse width is adjusted with an 8-bit global intensity register, and individual string pulse width is modulated with 12-bit registers.

The MSL3163/4 feature fault monitoring of open circuit, short circuit, loss of video sync and over temperature conditions, and provides a fault output to notify the system controller. Detailed fault status and control are available through the serial interface.

The MSL3163/4 are offered in a  $6 \times 6 \times 0.75$ mm, 40-pin TQFN package and operate over the -40°C to 85°C temperature range.

### **Applications**

#### Long Life, Efficient LED Backlighting For:

- Televisions and Desktop Monitors
- Medical and Industrial Instrumentation
- Automotive Audio-visual Displays

#### **Channel Signs**

#### Architectural Lighting

### **Ordering Information**

16-CHANNEL LED STRING DRIVERS							
PART	INTERFACE	PACKAGE					
MSL3163BT	I <sup>2</sup> C interface	40 pin, 6 x 6 x 0.75mm TQFN					
MSL3164BT	SPI interface	40 pin, 6 x 6 x 0.75mm TQFN					

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### **Key Features**

- 12-bit PWM String Dimming Operates at 240Hz
- Fast Serial Interfaces Support up to 16 Devices
  per Bus:
  - MSL3164 20 MHz SPI
  - MSL3163 1 MHz I<sup>2</sup>C
- 8-bit Adaptive Power Correction Maximizes Efficiency of up to Three String Power Supplies
- Drives 16 Parallel LED Strings of 10 White LEDs Each for up to 2560 White LEDs per Serial Bus
- Supports Adaptive, Real-time Area Dimming for Highest Dynamic Range LCD TVs and Monitors
- Programmable String Phase Reduces Motion Blur
- Global Intensity Control via Serial Interface
- 100mA Peak, 60mA Average LED String Current
- Single Resistor Sets Peak Current for all LED Strings

### **Application Circuit**

- ±3% Current Accuracy and Current Balance
- Video Frame (VSYNC) and Line (HSYNC) Sync Inputs
- Sync Loss Detectors Optionally Disable LED Strings
- Multiple MSL3163/4s Share String Power Supplies and Automatically Negotiate the Optimum Supply Voltage
- E<sup>2</sup>PROM Allows Customized Power-On Defaults
- Less Than 1µA LED String Off-Leakage Current
- String Open Circuit and LED Short Circuit Fault
  Detection
- Individual Fault Detection Enable for Each String
- Over-temperature Shutoff Protection
- Broadcast Write Simplifies Configuration
- -40°C To +85°C Operating Temperature Range





### Package Pin-out





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Figure 3. Package Dimensions: 40 Pin 6mm x 6mm x 0.75mm TQFN (0.5mm pin pitch) with exposed pad



### Package Pin Description

### Table 1. Pin Assignments

PIN	PIN NAME PIN DESCRIPTION						
	MSL3163	MSL3164					
1	FBI2	FBI2	Efficiency Optimizer input 2 Connect FBI2 to FBO2 of the next device when chaining devices (Figure 7). If unused connect FBI2 to GND.				
2	FBO3	FBO3	Efficiency Optimizer output 3 Connect FBO3 to the third power supply's feedback node or to FBI3 of the previous device when chaining devices (Figure 7). If unused connect FBO3 to GND.				
3	FBI3	FBI3	Efficiency Optimizer input 3 Connect FBI3 to FBO3 of the next device when chaining devices (Figure 7). If unused connect FBI3 to GND.				
4	PHI	PHI	Phase synchronization input Drive PHI with an external signal from 40Hz to 10kHz to synchronize the MSL3163/4 clock. PHI is typically the VSYNC signal input.				
5	GSC	GSC	Gate shift clock input Drive GSC with the gate shift clock of the video signal, from 0 to 10MHz. GSC is typically the HSYNC signal input.				
6	PWM	PWM	<b>PWM input</b> PWM allows direct external control of the brightness of all LED strings. The PWM input may also be used as a gate signal for the output of the PWM. Drive PWM with a pulse-width modulated signal with duty ratio ranging from 0% to 100% and frequency up to 5kHz.When not configured for use as an input PWM is high-impedance.				
7 - 14, 17 - 24	STR0 thru STR15	STR0 thru STR15	LED string current sink outputs Connect the cathode of the n'th strings bottom LEDs to STRn. Connect unused STRn outputs to GND.				
15	CGND	CGND	Connect to ground Connect CGND to GND and to EP with short, wide traces.				
16, 32	GND	GND	Signal ground Connect all GNDs to system ground and to EP with short, wide traces.				
25	FLTB	FLTB	Fault indication output (active low) Open drain output FLTB sinks current to GND whenever a fault condition is verified. Toggle EN low or read the fault registers to clear FLTB. Once cleared, FLTB reasserts if the fault conditions persist.				
26,30	AD0, AD1	AD0, AD1	Slave ID selection inputs Connect AD1 and AD0 to GND through resistors to set the device address for the serial interface.				
07	201	SCK	MSL3163: I <sup>2</sup> C serial clock input SCL is the clock input for the I <sup>2</sup> C serial interface.				
27	SCL	SCK	MSL3164: SPI serial shift clock SCK is the clock input for the SPI interface.				
28	TEST	MISO	MSL3163: factory test I/O Factory test. Make no electrical connection to TEST.				
20	TEST	WIISO	MSL3164: Master input slave output MISO is the SPI serial data output.				
29	SDA	MOSI	MSL3163: I <sup>2</sup> C serial data I/O SDA is the data I/O for the I <sup>2</sup> C serial interface.				
23	SDA	MOSI	MSL3164: Master input slave output MOSI is the SPI serial data input.				
31	GND	CSB	MSL3163: ground. Connect GND to system ground and to EP with short, wide traces.				
51	GND	0.00	MSL3164: chip select (active low) CSB is the chip select input for SPI transactions. CSB is active low.				
33	ILED	ILED	<b>Maximum LED string current setting input</b> Connect a resistor from ILED to GND to set the full-scale LED string current for all strings using $I_{STRING} = 762 / R_{ILED}$ . For example, connect a $12.7k\Omega$ resistor to GND to set a 60mA maximum sink current through each LED string.				
34	EN	EN	<b>Enable input (Active high)</b> Drive EN high to turn on the MSL3163/4, drive EN low to turn off the MSL3163/4. For automatic startup connect EN to VIN. When EN is low the entire device, including the serial interface, is turned off. Driving EN high initiates a boot load of the E <sup>2</sup> PROM data into the control registers, simulating a cold start-up.				
35	VIN	VIN	Supply voltage input Connect a 5V supply to VIN. Bypass VIN to GND with a 10µF ceramic capacitor placed close to VIN.				

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DIN	PIN N	IAME	
PIN MSL3163 MSL3164			PIN DESCRIPTION
36	VDD	VDD	<b>2.5V internal LDO regulator output</b> VDD powers internal logic. Bypass VDD to GND with a 4.7μF ceramic capacitor placed close to VDD.
37	NC	NC	No connect Leave NC unconnected.
38	FBO1	FBO1	Efficiency Optimizer output 1 Connect FBO1 to the first power supply's feedback node or to FBI1 of the previous device when chaining devices (Figure 7). If unused connect FBO1 to GND.
39	FBI1	FBI1	Efficiency Optimizer input 1 Connect FBI1 to FBO1 of the next device when chaining devices (Figure 7). If unused connect FBI1 to GND.
40	FBO2	FBO2	Efficiency Optimizer output 2 Connect FBO2 to the second power supply's feedback node or to FBI2 of the previous device when chaining devices (Figure 7). If unused connect FBO2 to GND.
EP	EP	EP	<b>Exposed pad, power ground</b> EP is the path that the string currents take to ground. EP also provides thermal relief for the die. Provide large traces from EP back to the string power supplies. Also connect EP to system ground, and to GND using short, wide traces.

### Absolute Maximum Ratings

### Voltage (With Respect to GND, CGND = EP = GND)

VIN, EN	-0.3V to +6V
VDD	0.3V to +2.75V
MSL3163: SDA, SCL	-0.3V to +6V
MSL3164: MISO, MOSI, CSB, SCK	0.3V to (VIN + 0.3V)
FLTB	-0.3V to +6V
ILED, AD0, AD1	0.3V to (VDD + 0.3V)
PHI, GSC, PWM, FBO1, FBO2, FBO3, FBI1, FBI2, FBI3	0.3V to (VIN + 0.3V)
STR0 thru STR15	0.3V to +40V
CGND	-0.3V to +0.3V

#### Current (Into Pin)

VIN	50mA
EP	
STR0 thru STR15	105mA
All other pins	

#### **Continuous Power Dissipation**

40-Pin 6mm x 6mm QFN (derate 37mW/°C above $T_A = +70^{\circ}C$ )	2963mW
Ambient Operating Temperature Range $T_A = T_{MIN}$ to $T_{MAX}$	-40°C to +85°C
Junction Temperature	+125°C
Storage Temperature Range6	55°C to +125°C
Lead Soldering Temperature, 10s	+300°C



### **Electrical Characteristics**

(Typical Application Circuit, VIN = 5V,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at VIN = 5V,  $T_A = +25^{\circ}$ C).

PARAMETER	SYMBOL	CONDITIONS AND NOTE	MIN	ТҮР	MAX	UNIT	
DC ELECTRICAL CHARACTERISTICS							
VIN Operating Supply Voltage	VIN		4.75	5	5.5	V	
		EN = VIN, SLEEP = 0, R <sub>ILED</sub> = 12.7kΩ, PHI = 240Hz, CSC = 082.04LU=	PWMn = 0x7FF		18	28	
VIN Operating Supply Current	I <sub>VIN</sub>	GSC = 983.04kHz, POWERCTRL = 0x4F, ISTR = 0xFF, OSCCTRL = 0x04, GSCINTEN = 0, PHIINTEN = 0, STRnEN = 1	PWMn = 0xFFF		24	35	mA
VIN Shutdown Supply Current	I <sub>shdn</sub>	EN = GND, SDA, SCL, AD0, AD1, PHI and GSC = GND	PWM,		10		μA
VIN Sleep Current	I <sub>sleep</sub>	EN = 1, SLEEP = 1, SDA, SCL, AI PWM, PHI and GSC = GND or VD	D0, AD1, D		1.5		mA
VDD Regulation Voltage	VDD			2.4	2.5	2.6	V
Input High Voltage: SDA, SCL, PWM, PHI, GSC, MOSI, CSB	V <sub>IH</sub>			0.7 x VDD			V
Input Low Voltage: SDA, SCL, PWM, PHI, GSC, MOSI, CSB	V <sub>IL</sub>					0.3 x VDD	V
Input High Voltage: EN				1.22			V
Input Low Voltage: EN						0.8	V
Output High Voltage: PHI, GSC, MISO	V <sub>OH</sub>	I <sub>SOURCE</sub> = 5mA	VIN – 0.4			V	
Output Low Voltage: PHI, GSC, SDA, MISO, FLTB	V <sub>ol</sub>	I <sub>SINK</sub> = 5mA				0.4	V
ILED Regulation Voltage		$R_{ILED} = 12.7 k\Omega$			350		mV
FBI Feedback Input Current				0		365	μA
FBO Feedback Output Current Range		$V_{FBO} \le VIN - 0.5V$		0		365	μA
FBO Feedback Output Current Step Size					1.1		μA
FBI Input Disable Threshold						50	mV
STR0 thru STR15 Sink Current		$R_{ILED}$ = 12.7k $\Omega$ , ISTR = 0xFF, $V_{STR}$	= 1V	55	60	67	mA
STR0 thru STR15 Sink Current Maximum		$R_{ILED} = 7.68 k\Omega$ , ISTR = 0xFF (Note	1)		100		mA
STR0 thru STR15 Current Load Regulation		$R_{ILED}$ = 12.7kΩ; ISTR = 0xFF, FLDBKEN = 0, V <sub>STRn</sub> = 1V to 5V			0.033		%/V
STR0 thru STR15 Current Matching		$R_{ILED} = 12.7 k\Omega$ , ISTR = 0x7F, $V_{STRn} = 1V$				5	%
STR0 thru STR15 Minimum Headroom	V <sub>STR</sub>	$R_{ILED} = 12.7k\Omega$ ; ISTR = 0xFF			0.5		V
STR0 thru STR15 Short Circuit Fault Detection Threshold	SC <sub>REF</sub>				3.5		V
		Current rising (Note 2)			608		
STR0 thru STR15 Current Slew Rate		Current falling (Note 2)		10868		mA/µs	
Thermal Shutdown Temperature		(Note 2)			135		°C

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PARAMETER	SYMBOL	CONDITIONS AND NOTES	MIN	ТҮР	MAX	UNIT
AC ELECTRICAL CHARACTERISTICS						
OSC Frequency	f <sub>osc</sub>	OSCCTRL = 0x04	18.15	20.00	21.88	MHz
PHI Frequency	f <sub>PHI</sub>		0.04		10	kHz
PHI Lock				4		PHI cycles
GSC Frequency	f <sub>gsc</sub>		0		10	MHz
PWM Frequency	f <sub>PWM</sub>				50	kHz
PWM Duty Cycle			0		100	%

PARAMETER	SYMBOL	CONDITIONS AND NOTES	MIN	ТҮР	MAX	UNIT
I <sup>2</sup> C TIMING CHARACTERISTICS, MSL3	163					
SCL Clock Frequency	1/t <sub>scl</sub>	Bus timeout disabled (Note 3)	0		1	MHz
Bus Timeout Period		OSCCTRL = 0x04		30		ms
	t <sub>timeout</sub>	f <sub>osc</sub> = 16MHz to 23MHz	6	00,000 / 1	OSC	S
STOP to START Condition Bus Free Time	t <sub>BUF</sub>		0.5			μs
Repeated START condition Hold Time	t <sub>hd:sta</sub>		0.26			μs
Repeated START condition Setup Time	t <sub>su:sta</sub>		0.26			μs
STOP Condition Setup Time	t <sub>su:stop</sub>		0.26			μs
SDA Data Hold Time	t <sub>HD:DAT</sub>		50			ns
SDA Data Valid Acknowledge Time	t <sub>vd:ACK</sub>	(Note 4)	0.05		0.45	μs
SDA Data Valid Time	t <sub>vd:dat</sub>	(Note 5)	0.05		0.45	μs
SDA Data Set-Up Time	t <sub>su:dat</sub>		100			ns
SCL Clock Low Period	t <sub>LOW</sub>		0.5			μs
SCL Clock High Period	t <sub>ніGH</sub>		0.26			μs
SDA, SCL Fall Time	t <sub>r</sub>	(Note 6) (Note 7)			120	ns
SDA, SCL Rise Time	t <sub>r</sub>				120	ns
SDA, SCL Input Suppression Filter Period	t <sub>sP</sub>	(Note 8)		50		ns

PARAMETER	SYMBOL	CONDITIONS AND NOTES	MIN	ТҮР	MAX	UNIT		
SPI TIMING CHARACTERISTICS, MSL3164								
SCK Frequency					20	MHz		
CSB Falling Edge to SCK Rising Edge Setup Time	t <sub>CSB:SCK(SU)</sub>		100			ns		



PARAMETER	SYMBOL	CONDITIONS AND NOTES	MIN	ТҮР	МАХ	UNIT
SCK Falling Edge to CSB Rising Edge Setup Time	t <sub>SCK:CSB(SU)</sub>		50			ns
MOSI to Falling Edge of SCK Setup Time	t <sub>MOSI(SU)</sub>		16			ns
SCK Falling Edge to MOSI Setup Time	t <sub>MOSI(HOLD)</sub>		20			ns
MOSI, CSB, SCK Signal Rise Time	t <sub>R(SPI)</sub>			5.0		ns
MOSI, CSB, SCK Signal Fall Time	t <sub>F(SPI)</sub>			5.0		ns
CSB Falling Edge to MISO Data Valid	t <sub>CSB:MISO(DV)</sub>				50	ns
CSB Rising Edge to MISO High Impedance	t <sub>CSB:MISO(HIZ)</sub>				50	ns
SCK Rising Edge to MISO Data Valid	t <sub>valid</sub>			25	80	ns

Note 1. Subject to thermal dissipation characteristics of the device

Note 2. Guaranteed by design, not production tested.

Note 3. Minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface if either SDA or SCL is held low for  $t_{imeout}$ . Disable bus timeout via the Power Control register 0x02[6].

Note 4.  $t_{VD:ACK}$  = SCL LOW to SDA (out) LOW acknowledge time.

Note 5.  $t_{vDDAT}$  = minimum SDA output data-valid time following SCL LOW transition.

Note 6. A master device must internally provide an SDA hold time of at least 300ns to ensure an SCL low state.

Note 7. The maximum SDA and SCL rise times is 300ns. The maximum SDA fall time is 250ns. This allows series protection resistors to be connected between SDA and SCL inputs and the SDA/SCL bus lines without exceeding the maximum allowable rise time.

Note 8. MSL3163/4 includes input filters on SDA, SCL, AD0 and AD1 inputs that suppress noise less than 50ns.

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### **Block Diagram**

The block diagram for the Atmel LED Drivers-MSL3163/4 is shown in Figure 4.



Figure 4. Atmel LED Drivers-MSL3163/4 Block Diagram



### **Typical Application Circuit**



Figure 5. Atmel LED Driver-MSL3164 Driving 160 White LEDs in 16 Strings at 60mA Per String.

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### **Detailed Description**

The MSL3163 and MSL3164 are highly integrated, flexible multi-string LED drivers with power supply control to maximize system efficiency. The drivers easily connect to a video subsystem. Although optional, this offers a simple architecture for use in LCD TV backlight applications. Up to 16 drivers easily connect together to drive large numbers of LED strings in a system. The drivers provide multiple methods of controlling LED brightness, through both peak current control and through pulse width control of the string drive signals. Peak current control offers excellent color consistency, while pulse width control allows brightness management. An on-chip E<sup>2</sup>PROM holds all the default control register values. At power-up the data in the E<sup>2</sup>PROM automatically copy directly to the control registers, setting up the device for operation.

The devices interface to a µC via I<sup>2</sup>C (MSL3163) or SPI (MSL3164). The robust 1MHz I<sup>2</sup>C interface supports up to 16 devices on the bus. The 20MHz bus addressable SPI interface supports up to 16 devices per Chip Select line. While typically the LED drive PWM signal is internally generated, both drivers also accept an external direct-drive PWM signal and offer optional string drive phase spreading. With direct-drive PWM, a Pulse Width Modulated signal applied to the PWM input sets the PWM duty and the frequency of the LEDs drive signal. With phase spreading enabled, a progressive 1/16 PWM-frame time delay per string helps reduce both the transient load on the LED power supplies, and the power supply input capacitor size requirements.

The PWM frequency of the drivers is either synchronized to an external signal applied to PHI, or generated from the internal oscillator for stand-alone applications. Typically the VSYNC signal from the video system is used for the PHI input. The on-time of each string is individually programmed via the device registers, providing a peak resolution of 12-bits when using the on-chip PWM generator. The actual resolution of the PWM frequency depends upon on the ratio of the GSC frequency (typically provided by a systems HSYNC signal, but can be internally generated) to the PHI frequency, because the on-time of a string is programmed as a 12-bit count of the number of GSC clock cycles. This count can be further scaled by an 8-bit Global intensity value, when enabled. The GSC clock is also used to precisely set each string's phase delay so that it is synchronized relative to the video frame.

The Efficiency Optimizers control a wide range of different architectures of external DC/DC and AC/DC converters. Multiple drivers in a system communicate with each other in real time to select an optimized operating voltage for the LEDs. This allows design of the power supply for the worst case Forward Voltage ( $V_f$ ) of the LEDs without worrying about excessive power dissipation issues. During the start-up sequence the MSL3163/4 automatically reduce the power supply voltage to the minimum voltage required to keep the LEDs in current regulation. The devices can be configured to periodically perform this optimization to compensate for changes of the LED's forward voltage, and to assure continued optimum power savings.

#### Internal Regulators and Enable Input

The MSL3163/4 includes an internal linear regulator that operates from the 5V nominal input supply, VIN, and provides an internal 2.5V supply, VDD, to power the low-voltage internal circuitry. Bypass VDD (pin 36) to GND with a  $4.7\mu$ F capacitor. Bypass VIN (pin 35) to GND with a  $10\mu$ F capacitor.

The MSL3163/4 enable input, EN, enables the device. Drive EN low to enter low power operation, which lowers quiescent current draw to less than  $20\mu$ A. With EN low the serial interface is ignored. Drive EN high to turn on the device. When EN is driven high the contents of the E<sup>2</sup>PROM are boot-loaded into the control registers, simulating a cold start-up.



### Setting the LED String Current with $\mathrm{R}_{_{\mathrm{ILED}}}$ and ISTR

The MSL3163/4 features 16 current sink outputs, rated at 40V, each designed to sink up to 100mA peak. Limit average current to 60mA if the PCB copper around the MSL3163/4 is the only heat sink employed. The maximum string current,  $I_{LED}$ , for all 16 LED string inputs is set by a single external resistor,  $R_{LED}$ , placed from ILED to GND, whose value is determined using:

$$R_{ILED} = \frac{762}{I_{ILED}}$$

For example, a full-scale LED current of 60mA returns  $R_{ILED} = 12.7 k\Omega$ . The current for all LED strings is reduced from its full-scale value with 8-bit resolution using ISTR, the String Current Control register 0x0F.



Figure 6. FBOn Connects to the Power Supply Voltage Divider Through a Diode

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# Connecting the Efficiency Optimizer to an LED String Power Supply and Selecting Resistors

The MSL3163/4 are designed to control LED string power supplies that use a voltage divider ( $R_{TOP}$  and  $R_{BOTTOM}$  in Figure 6) to set output voltage, and whose regulation feedback voltage is not more than 3.5V. The Efficiency Optimizer improves power efficiency by injecting a current of between 0µA and 255µA into the voltage divider of the external power supply, dynamically adjusting the power supply's output to the minimum voltage required by the LED strings. To select the resistors first determine  $V_{OUT(MIN)}$  and  $V_{OUT(MAX)}$ , the minimum and maximum string supply voltage limits, using:

$$V_{OUT(MIN)} = \left(V_{f(MIN)} * [\#ofLEDs]\right) + 0.5 ,$$

and

$$V_{OUT(MAX)} = \left(V_{f(MAX)} * [\#ofLEDs]\right) + 0.5 ,$$

where V<sub>f(MIN)</sub> and V<sub>f(MAX)</sub> are the LED's minimum and maximum forward voltage drops at the peak current set by R<sub>ILED</sub> (page 10). For example, if the LED data are V<sub>f(MIN)</sub> = 3.5V and V<sub>f(MAX)</sub> = 3.8V, and ten LEDs are used in a string, then the total minimum and maximum voltage drops across the LEDs are 35V and 38V. Adding an allowance of 0.5V of for the string drive MOSFET headroom brings V<sub>OUT(MIN)</sub> to 35.5V and V<sub>OUT(MAX)</sub> to 38.5V. Do not to exceed the 40V maximum specification of the string drivers STR1 thru STR15. Then determine R<sub>TOP</sub> using:

$$R_{TOP} = \frac{V_{OUT(MAX)} - V_{OUT(MIN)}}{I_{FBOn(MAX)}}$$

where  $I_{\rm FBOn(MAX)}$  is the 255µA maximum output current of the Efficiency Optimizer outputs FBOn (if cascading multiple MSL3163/4s determine  $I_{\rm FBOn(MAX)}$  as shown in the next section). Finally, determine  $R_{\rm BOTTOM}$  using:

$$R_{BOTTOM} = R_{TOP} * \frac{V_{FB}}{V_{OUT(MAX)} - V_{FB}},$$

where  $V_{FB}$  is the regulation feedback voltage of the power supply. Place a diode (1N4148 or similar) between FBOn and the supply's feedback node to protect the MSL3163/4 against current flow into FBOn.

#### Using Multiple Atmel LED Drivers-MSL3163/4s to Control a Common Power Supply

Cascade multiple MSL3163/4 devices into a chain configuration, with the FBIn of one device connected to the FBOn of the next (Figure 7). Connect the first FBOn to the power supply feedback resistor node through a diode, and the unused FBIn inputs (and any unused FBOn outputs) to GND as close to the MSL3163/4 as possible. Assign all strings powered by a common supply to the proper FBOn output using String Set registers (STRNSET) 0x20 thru 0x3F. The chained devices work together to ensure that the system operates at optimum efficiency. Note that the accuracy of the feedback chain may degrade through each link of the FBIn/FBOn chain by as much as 2%. Determine the potential worst case maximum FBOn current I<sub>FBOn(MAX/MIN)</sub> using:

 $I_{FBOn(MAX/MIN)} = 255 \mu A^* (0.98)^{N-1} ,$ 

where N is the number of MSL3163/4s connected in series. Use this result in the above  $R_{TOP}$  resistor equation for the term  $I_{FBOn(MAX)}$  instead of using 255µA.

Take care in laying out the traces for the Efficiency Optimizer connections. Minimize the FBIn/FBOn trace lengths as much as possible. Do not route the signals close to traces with large variations in voltage or current, because noise may couple into FBIn. If these traces must be routed near noisy signals, shield them from noise by using ground planes or guard traces.





Figure 7. Example of Cascading Multiple Devices to Optimize Common Power Supplies

### Direct PWM Control of the LED Strings

An external PWM signal applied to the PWM input allows direct PWM control over the strings when bits PWMEN and PWMDIRECT are set in PWM Control register 0x1E. This configuration bypasses PHI and GSC, but allows automatic LED string phase delay using bit D2 of register 0x1E.

The PWM input can also be configured as a gate for the output of the PWM engine using the PWM Global Enable bit D3 of the PWM Control register 0x1E.

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### Register Map and the E<sup>2</sup>PROM

#### Register Map Summary

Control the MSL3163/4 using the 96 registers in the range 0x00 thru 0x5F (Table 2). It may be convenient, and it is allowed, to read and write to unused bits in this range when accessing registers, but always write zeros. Reads from unused bits always return zeros. Three additional registers, 0x90, 0x91 and 0x93 allow access to the E<sup>2</sup>PROM and provide Efficiency Optimizer status. The power-up default values for all control registers are stored within the on-chip E<sup>2</sup>PROM, and any of these E<sup>2</sup>PROM values may be changed through the serial interface.

#### Table 2. Atmel LED Drivers-MSL3163/4 Register Map

ADDRESS AND FUNCTION			REGISTER DATA								
REG	STER NAME	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0	
0x00	CONTROL0	LED string	STR7EN	STR6EN	STR5EN	STR4EN	STR3EN	STR2EN	STR1EN	STR0EN	
0x01	CONTROL1	enables	STR15EN	STR14EN	STR13EN	STR12EN	STR11EN	STR10EN	STR9EN	STR8EN	
0x02	POWERCTRL	Fault configuration	SLEEP	I <sup>2</sup> CTOEN	PHIMINFEN	GSCMAXFEN	STRSCFEN	STROCFEN	FBOOCEN	FBOEN	
0x03	FLTSTATUS	Fault status, global	-	-	PHIMINFLT	GSCMAXFLT	STRSCDET	STROCDET	FBOOC	FLTDET	
0x04	OCSTAT0	String open	OC7	OC6	OC5	OC4	OC3	OC2	OC1	OC0	
0x05	OCSTAT1	circuit fault status	OC15	OC14	OC13	OC12	OC11	OC10	OC9	OC8	
0x06	SCSTAT0	String short	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
0x07	SCSTAT1	circuit fault status	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	
0x08	FLTMASK0	String fault	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	
0x09	FLTMASK1	masks	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	
0x0A	FBOCTRL0	Efficiency	HDRMS	TEP[1:0]	FBCL	DLY[1:0]	FBSDL	Y[1:0]	FBCFI	DLY[1:0]	
0x0B	FBOCTRL1	Optimizer control	SCCD	LY[1:0]	DECRS	STEP[1:0]	INITPWM	ACAL100	ACALEN	ICHKDIS	
0x0C	FBODAC1	Efficiency				FBOD	AC1[7:0]				
0x0D	FBODAC2	Optimizer DAC		FBODAC2[7:0]							
0x0E	FBODAC3	readback				FBOD	AC3[7:0]				
0x0F	ISTR	8-bit global string current				IST	R[7:0]				
0x10	OSCCTRL	Oscillator frequency	-	-	-	-	-		OSCTRL[2:0	]	
0x11	GSCCTRL	GSC processing control	GSCCHK- SEL	-	-	-	GSCMAXEN	GSCPOL	GSCPHI- SYNCEN	GSCINTEN	
0x12	000051	Internal GSC				GSC	GEN[7:0]				
0x13	GSCGEN	clock generator				GSCG	EN[15:8]				
0x14	GSCMUL	GSC multiplier	-	-	-		G	SCMUL[4:0]			
0x15	GSCDIV	GSC divider	-	-	-	-		GSCD	IV[3:0]		
0x16		Max oscillator				GSC	MAX[7:0]				
0x17	GSCMAX	cycles between GSC pulses				GSCM	IAX[15:8]				
0x18	PHICTRL	PHI processing control	-	-	-	-	-	PHIMINEN	PHIPOL	PHIINTEN	
0x19	DUICEN	Internal PHI				PHIC	EN[7:0]				
0x1A	PHIGEN	clock generator				PHIG	EN[15:8]				



#### Table 2. Atmel LED Drivers-MSL3163/4 Register Map

ADDRESS AND REGISTER NAME		FUNCTION	REGISTER DATA											
		FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0				
0x1B UNUSED							SED							
0x1C	PHIMIN	Min GSC pulses	PHIMIN[7:0]											
0x1D	FILIVILIN	over PHI period	PHIMIN[11:8]											
0x1E	PWMCTRL	PWM control	FLDBKEN	-	GINTEN	PWM- OFLOWEN	PWMGLBLEN PHA- DLYEN		PWM- DIRECT	PWMEN				
0x1F	GINT	Global PWM scaling				G	INT[7:0]							
0x20		Phase delay and		PHDLY0[7:0]										
0x21	STR0SET	EO assignment for string 0	COLST	R0[1:0]	-	-	PHDLY[11:8]							
↓	$\downarrow$	Ļ												
0x3E		Phase delay and												
0x3F	STR15SET	EO assignment for string 15	COLSTR15[1:0] PHDLY[11:8]											
0x40		PWM0 12-bit PWM setting for string 0	PWM0[7:0]											
0x41	PWM0		-	-	-	-	PWM0[11:8]							
↓	$\downarrow$	↓					$\downarrow$							
0x5E		12-bit	PWM15[7:0]											
0x5F	PWM15	PWM setting for string 15	-	-	-	-	PWM15[11:8]							
			- Do	o Not Acces	s Address Rar	nge 0x60 Thru	0x8F -							
0x90	E2ADDR	E <sup>2</sup> PROM read/	-			E2ADDR[6:0]								
0x91	E2CTRLSTA	write access	E2BUSY	BLDACT	E2ERR	-	- RWCTRL[2:0]							
0x93	FBOSTATUS	FBO status	F	BOOPEN[	3:1]	FBOACTIVE[3:1] FBOCAL FBOINI								

16-string White & RGB LED Drivers with Adaptive Power Control, E<sup>2</sup>PROM, and SPI/I<sup>2</sup>C/SMBus Serial Interface

### Register Power-Up Defaults

Register power-up default values are shown in Table 3

#### Table 3. Atmel LED Drivers-MSL3163/4 Register Power-Up Defaults

REGISTER NAME AND ADDRESS		POWER-UP CONDITION	REGISTER DATA								
		I OWER-OF CONDITION		D6	D5	D4	D3	D2	D1	D0	
0x00	CONTROL0	LED strings STR0 thru STR7 enabled	1	1	1	1	1	1	1	1	
0x01	CONTROL1	LED strings STR8 thru STR15 enabled	1	1	1	1	1	1	1	1	
0x02	POWERCTRL	Efficiency Optimizer outputs enabled FBO open circuit detection enabled String open circuit detection enabled LED short circuit detection enabled GSC maximum fault detection disabled PHI minimum fault detection disabled I <sup>2</sup> C bus timeout detection enabled Device awake		1	0	0	1	1	1	1	
0x08	FLTMASK0	Fault detection enabled on all strings		1	1	1	1	1	1	1	
0x09	FLTMASK1			1	1	1	1	1	1	1	
0x0A	FBOCTRL0	Current sink error confirmation delay = 4µS FBO power supply correction delay = 2ms Efficiency Optimizer recalibration delay = 1s Efficiency Optimizer correction steps = 6 Current sink error detection not disabled Auto recalibration enabled PWM settings used during auto recalibration PWM duty cycle = 100% during initial calibration Efficiency Optimizer operates using 1µA steps LED short circuit confirmation delay = 4µs		0	0	0	0	0	0	0	
0x0B	FBOCTRL1			0	0	1	0	0	1	0	
0x0F	ISTR	Strings current set to 50% of $R_{_{\rm ILED}}$ setting	0	1	1	1	1	1	1	1	
0x10	OSCCTRL	f <sub>osc</sub> = 20MHz	0	0	0	0	0	1	0	0	
0x11	GSCCTRL	GSC synchronized to the falling edge of the external signal	0	0	0	0	0	0	0	0	
0x12	GSCGEN	Although disabled, Internal GSC frequency =	0	0	0	1	0	0	1	1	
0x13	GSCGEN	20MHz / (19 + 1) = 1MHz	0	0	0	0	0	0	0	0	
0x14	GSCMUL	GSC multiplied by 4	0	0	0	0	0	0	1	1	
0x15	GSCDIV	GSC not divided	0	0	0	0	0	0	0	0	
0x16	K16 GSCMAX	Although disabled, GSC max count is set to 19 clock cycles	0	0	0	1	0	0	1	1	
0x17			0	0	0	0	0	0	0	0	
0x18	PHICTRL	PHI synchronized to the falling edge of the external signal		0	0	0	0	0	0	0	
0x19		Although disabled,	1	0	1	1	0	0	0	0	
0x1A	PHIGEN	Internal PHI frequency = 20MHz / (8 * (10416 + 1)) = 240Hz		0	1	0	1	0	0	0	
0x1C	PHIMIN	No DHI minimum	0	0	0	0	0	0	0	0	
0x1D		No PHI minimum	0	0	0	0	0	0	0	0	



REGISTER NAME AND ADDRESS		POWER-UP CONDITION	REGISTER DATA									
			D7	D6	D5	D4	D3	D2	D1	D0		
0x1E	PWMCTRL	$\begin{array}{c} PWM \ Operation \ enabled \\ Internal \ PWM \ engine \ determines \ t_{ON} \ and \ t_{OFF} \\ Phase \ delay \ enabled \\ PWM \ input \ not \ esed \ as \ gate \ for \ PWM \ engine \ output \\ String \ on-times \ allowed \ to \ extend \ beyond \ PWM \ frame \\ GINT \ ignored \\ String \ current \ fold-back \ enabled \end{array}$		0	0	1	0	1	0	1		
0x1F	GINT	Although Disabled, Global Intensity is set to (127) / 256 = 49.6%		1	1	1	1	1	1	1		
0x20	STR0SET	All Strings set to 0 Phase Delay	0	0	0	0	0	0	0	0		
0x21	SIRUSEI	Strings Efficiency Optimizer assignments are:	0*	1*	0	0	0	0	0	0		
$\downarrow$	$\downarrow$	FBO1: Strings 0,4,8,12		↓								
0x3E	STR15SET	FBO2: Strings 1,2,5,6,9,10,13,14	0	0	0	0	0	0	0	0		
0x3F	STRIDGET	FBO3: Strings 3, 7, 11, 15		1*	0	0	0	0	0	0		
0x40	PWM0	↓ All Strings Have PWM Value = 512 GSC Cycles		0	0	0	0	0	0	0		
0x41	PVVIVIO			0	0	0	0	0	1	0		
↓	Ļ			↓								
0x5E	PWM15			0	0	0	0	0	0	0		
0x5F	CININA			0	0	0	0	0	1	0		
0x90	E2ADDR	E <sup>2</sup> PROM 7-bit address = 0x00		0	0	0	0	0	0	0		
0x91	E2CTRLSTA	E <sup>2</sup> PROM read/write disabled		0	0	0	0	0	0	0		
0x93	FBOSTATUS	Feed Back Output Status		0	0	0	0	0	0	0		

\* These bits set the FBOn string assignments.

#### Atmel Corporation

2325 Orchard Parkway San Jose, CA 95131 USA **Tel:** (+1)(408) 441-0311 **Fax:** (+1)(408) 487-2600 www.atmel.com

#### Atmel Asia Limited

Unit 01-5 & 16, 19F BEA Tower, Millennium City 5 418 Kwun Tong Road Kwun Tong, Kowloon HONG KONG **Tel:** (+852) 2245-6100 **Fax:** (+852) 2722-1369

#### Atmel Munich GmbH

Business Campus Parkring 4 D-85748 Garching b. Munich GERMANY Tel: (+49) 89-31970-0 Fax: (+49) 89-3194621

#### Atmel Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 JAPAN Tel: (+81)(3) 3523-3551 Fax: (+81)(3) 3523-7581

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