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Virtex 6 Reference Design vs1 A/T 12V Input Bus Design. 12V@64W #1 Sequence Voltage (First on) Core PTH08T230W 1V@3A **VCC**_{INT} 1.0V@6A $5k\Omega$ Eff. 83% TPS3808G0.9 /Reset -Vcc 5V-1V SVS VS2_A/T Delay VCC to #2 Sequence control logic high I/O Ethernet Phy. SVS PTH08T230W 2.5V@2A- VCC_{AUX} 2.5V@6A Eff. 90% ≥Vcc 5V TPS3808G25 /Reset(All other voltages) VS3_A/T 2.5V SVS Delay DDR3 VDD. PTH08T260W -1.5V@2A **VCCO** 1.5V@3A Eff. 87% VCC LDO VL1 TPS51200 -DDR3 DDR3 VTT 0.75V@2A From SVS2.5V 0.75 @3A /Reset(All other voltages) Eff. 60% VREF VS4 ♥A/T 5.1V I/O Ethernet Phy. PTH08000W 1.8V@1A 1.8V@2.25A Eff. 88% I/O SFP etc, PTH08000W -3.3V@1A-3.3V@2.25A Eff.92% 5V VCC SVS **GTP Core** PTH08T230W 1V@6A Rocket I/O 1.0V@6A Eff. 83% Low noise 5mV ripple VS7 ▼A/T **GTP Termination** PTH08T230W 1.2V@6A-Rocket I/O 1.2V@6A Low noise Eff. 85% 5mV Ripple VS8 PA/T **FMC Connector** PTH08T230W 3.3V@3A 3.3V@3A Eff.92%

1. The sequence for V6 power is VCCINT (1.0V), VCCAUX (2.5V), and VCCO (1.5V and 2.5V). All rails including 3.3V rail should be last to power-up.

12V@1A

FMC Conector

Note 2: A/T = auto track function

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Notes:

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