

**AEC-Q100 Qualified Low Skew 1 to 4 Automotive Clock Buffer**

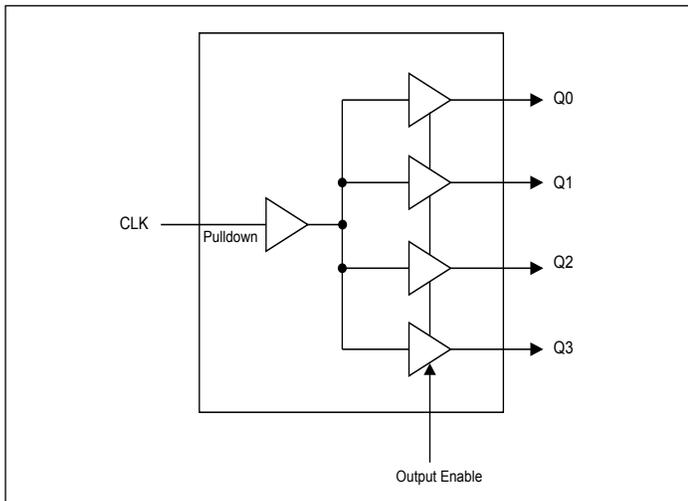
**Features**

- Low Skew Outputs (250ps)
- Low Power CMOS Technology
- Operating Voltages of 1.5V to 3.3V
- Output Enable pin Tri-States Outputs
- 3.6V Tolerant Input Clock
- AEC-Q100 Qualified
- Automotive Grade 2 Temperature Range (-40°C to 105°C)
- Automotive Grade 3 Temperature Range (-40°C to 85°C)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- The PI6C49CB04CQ is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.
- <https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green): 8-pin, SOIC (W)

**Description**

The PI6C49CB04CQ is an automotive-qualified, low-skew, single input to four output, clock buffer. Perfect for fanning out multiple clock outputs.

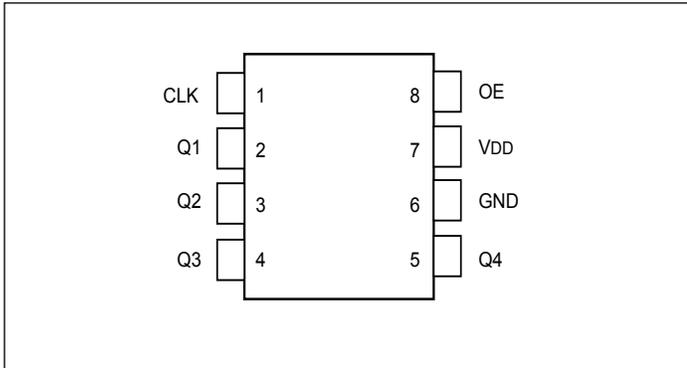
**Block Diagram**



**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Configuration



## Pin Descriptions

Pin#	Pin Name	Pin Type	Pin Description
1	CLK	Input	Clock Input. 3.3 V tolerant input. Internal 51k $\Omega$ pulldown resistor.
2	Q1	Output	Clock Output 1
3	Q2	Output	Clock Output 2
4	Q3	Output	Clock Output 3
5	Q4	Output	Clock Output 4
6	GND	Power	Connect to ground
7	VDD	Power	Connect to 1.5V, 1.8V, 2.5V, or 3.3V
8	OE	Input	Output Enable. Tri-states outputs when low. Internal 125K $\Omega$ pullup resistor. Default on.

## External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 $\mu$ F should be connected between VDD on pin 7 and GND on pin 6, as close to the device as possible. A 33 $\Omega$  series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

## Maximum Ratings

Supply Voltage, VDD	4.6V
Output Enable and All Outputs	-0.5V to VDD+0.5V
CLK	-0.5V to 3.6V (VDD > 0V)
Storage Temperature	-65°C to +150°C
ESD Protection (HBM)	2000V
Junction Temperature	125°C max

**Note:**

Stresses above the ratings listed below can cause permanent damage to the PI6C49X0204CQ. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (Automotive Grade 2)	-40	—	+105	°C
Ambient Operating Temperature (Automotive Grade 3)	-40	—	+85	°C
Power Supply Voltage (Measured in Respect to GND)	+1.425	—	+3.6	V

## DC ELECTRICAL CHARACTERISTICS

VDD=1.5 V ±5%, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage	—	1.425	1.5	1.575	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	0.9	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.575	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	40	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
I <sub>IH</sub>	Input High Current	OE <sup>(1)</sup>	—	—	1	μA
I <sub>IL</sub>	Input Low Current	OE <sup>(1)</sup>	—	—	40	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -6mA	0.95	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 6mA	—	—	0.45	V
IDD	Operating Supply Current	5pF, 160MHz	—	15	21	mA
		5pF, 100MHz	—	13	17	mA
		5pF, 50MHz	—	7	9	mA
		5pF, 25MHz	—	4	5.5	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±12	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

**VDD=1.8 V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage	—	1.7	1.8	1.89	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	1.1	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.6	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	50	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
I <sub>IH</sub>	Input High Current	OE <sup>(1)</sup>	—	—	1	μA
I <sub>IL</sub>	Input Low Current	OE <sup>(1)</sup>	—	—	50	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8mA	1.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA	—	—	0.4	V
IDD	Operating Supply Current	5pF, 160MHz	—	22	28	mA
		5pF, 100MHz	—	17	21	mA
		5pF, 50MHz	—	9	12	mA
		5pF, 25MHz	—	5	7	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin	—	5	—	pF
I <sub>OS</sub>	Short Circuit Current	—	—	±20	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

**VDD=2.5 V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage	—	2.375	2.5	2.625	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	1.7	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.7	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	60	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
I <sub>IH</sub>	Input High Current	OE <sup>(1)</sup>	—	—	1	μA
I <sub>IL</sub>	Input Low Current	OE <sup>(1)</sup>	—	—	60	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8mA	2	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA	—	—	0.4	V
IDD	Operating Supply Current	5pF, 100MHz	—	24	30	mA
		5pF, 50MHz	—	12	15	mA
		5pF, 25MHz	—	7	9	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±50	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

**VDD=3.3 V ±10%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage	—	3.0	3.3	3.6	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	2.4	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.7	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	85	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
I <sub>IH</sub>	Input High Current	OE <sup>(1)</sup>	—	—	1	μA
I <sub>IL</sub>	Input Low Current	OE <sup>(1)</sup>	—	—	85	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8mA	2.8	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA	—	—	0.2	V
IDD	Operating Supply Current	5pF, 100MHz	—	32	38	mA
		5pF, 50MHz	—	16	19	mA
		5pF, 25MHz	—	10	12	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±50	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

## AC ELECTRICAL CHARACTERISTICS

**VDD=1.5 V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	160	MHz
t <sub>OR</sub>	Output Rise Time	20% to 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% to 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	2	3	5	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps

**VDD=1.8 V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	160	MHz
t <sub>OR</sub>	Output Rise Time	20% to 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% to 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	1.3	2	4	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps
J <sub>ADD</sub>	Additive Jitter	@ 156.25MHz, 12k to 20MHz	—	0.1	—	ps

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**VDD=2.5 V ±5%**, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	160	MHz
t <sub>OR</sub>	Output Rise Time	20% TO 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% TO 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	0.8	1.5	3	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps
J <sub>ADD</sub>	Additive Jitter	@ 156.25MHz, 12k to 20MHz	—	0.05	—	ps

**VDD=3.3 V ±10%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	100	MHz
t <sub>OR</sub>	Output Rise Time	20% TO 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% TO 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	0.8	1.0	2.5	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps
J <sub>ADD</sub>	Additive Jitter	@ 156.25MHz, 12k to 20MHz	—	0.05	—	ps

Notes:

1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.

## DC ELECTRICAL CHARACTERISTICS

VDD=1.5 V ±5%, Ambient temperature -40°C to +85°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage	—	1.425	1.5	1.575	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	0.9	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.575	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	40	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
I <sub>IH</sub>	Input High Current	OE <sup>(1)</sup>	—	—	1	μA
I <sub>IL</sub>	Input Low Current	OE <sup>(1)</sup>	—	—	40	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -6mA	0.95	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 6mA	—	—	0.45	V
IDD	Operating Supply Current	5pF, 160MHz	—	15	21	mA
		5pF, 100MHz	—	13	17	mA
		5pF, 50MHz	—	7	9	mA
		5pF, 25MHz	—	4	5.5	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±12	—	mA

Notes: 1. Nominal switching threshold is VDD/2

VDD=1.8 V ±5%, Ambient temperature -40°C to +85°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage	—	1.7	1.8	1.89	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	1.1	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.6	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	50	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
I <sub>IH</sub>	Input High Current	OE <sup>(1)</sup>	—	—	1	μA
I <sub>IL</sub>	Input Low Current	OE <sup>(1)</sup>	—	—	50	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8mA	1.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA	—	—	0.4	V
IDD	Operating Supply Current	5pF, 160MHz	—	22	28	mA
		5pF, 100MHz	—	17	21	mA
		5pF, 50MHz	—	9	12	mA
		5pF, 25MHz	—	5	7	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω

**VDD=1.8 V ±5% Cont.**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C <sub>IN</sub>	Input Capacitance	CLK, OE pin	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±20	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

**VDD=2.5 V ±5%, Ambient temperature -40°C to +85°C, unless stated otherwise**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage	—	2.375	2.5	2.625	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	1.7	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.7	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	60	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
I <sub>IH</sub>	Input High Current	OE <sup>(1)</sup>	—	—	1	μA
I <sub>IL</sub>	Input Low Current	OE <sup>(1)</sup>	—	—	60	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8mA	2	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA	—	—	0.4	V
IDD	Operating Supply Current	5pF, 200MHz	—	46	56	mA
		5pF, 100MHz	—	24	30	mA
		5pF, 50MHz	—	12	15	mA
		5pF, 25MHz	—	7	9	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±50	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

**VDD=3.3 V ±10%, Ambient temperature -40°C to +85°C, unless stated otherwise**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage	—	3.0	3.3	3.6	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	2.4	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.7	V
I <sub>IH</sub>	Input High Current	CLK, OE <sup>(1)</sup>	—	—	85	μA
I <sub>IL</sub>	Input Low Current	CLK, OE <sup>(1)</sup>	—	—	1	μA
I <sub>IH</sub>	Input High Current	OE <sup>(1)</sup>	—	—	1	μA
I <sub>IL</sub>	Input Low Current	OE <sup>(1)</sup>	—	—	85	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8mA	2.8	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA	—	—	0.2	V

**VDD=3.3 V ±10% Cont.**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
IDD	Operating Supply Current	5pF, 200MHz	—	62	75	mA
		5pF, 100MHz	—	32	38	mA
		5pF, 50MHz	—	16	19	mA
		5pF, 25MHz	—	10	12	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±50	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

## AC ELECTRICAL CHARACTERISTICS

**VDD=1.5 V ±5%**, Ambient temperature -40°C to +85°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	166	MHz
t <sub>OR</sub>	Output Rise Time	20% to 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% to 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	2	3	5	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps

**VDD=1.8 V ±5%**, Ambient temperature -40°C to +85°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	166	MHz
t <sub>OR</sub>	Output Rise Time	20% to 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% to 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	1.3	2	4	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps
J <sub>ADD</sub>	Additive Jitter	@ 156.25MHz, 12k to 20MHz	—	0.1	—	ps

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**VDD=2.5 V ±5%**, Ambient temperature -40°C to +85°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	200	MHz
t <sub>OR</sub>	Output Rise Time	20% TO 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% TO 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	0.8	1.5	3	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps
J <sub>ADD</sub>	Additive Jitter	@ 156.25MHz, 12k to 20MHz	—	0.05	—	ps

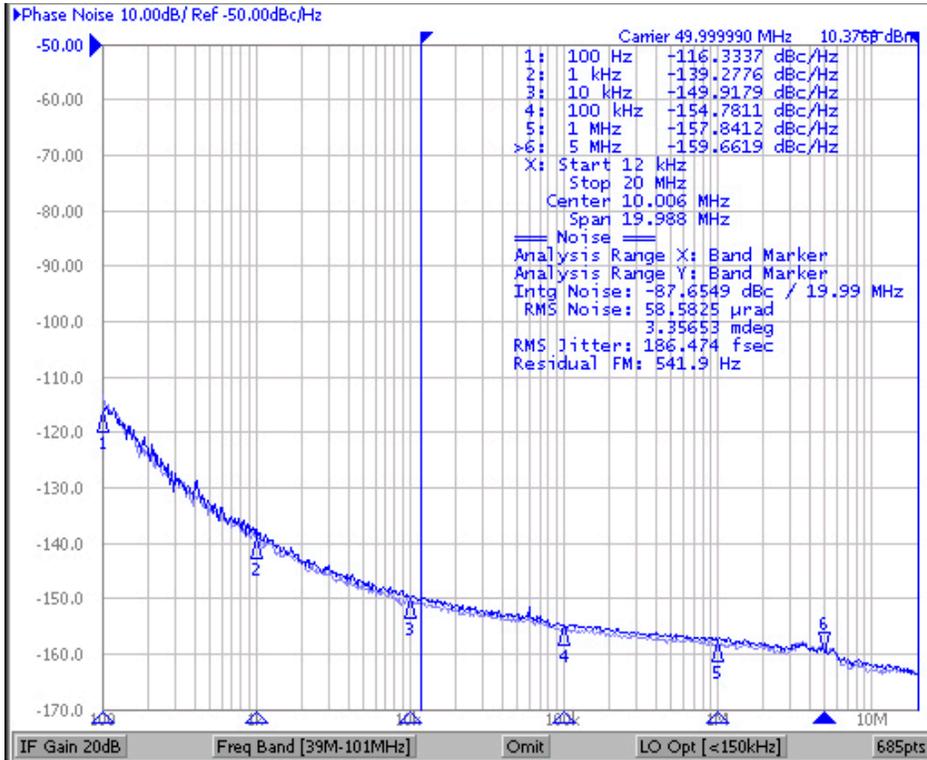
**VDD=3.3 V ±10%**, Ambient temperature -40°C to +85°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	200	MHz
t <sub>OR</sub>	Output Rise Time	20% TO 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% TO 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	0.8	1.0	2.5	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps
J <sub>ADD</sub>	Additive Jitter	@ 156.25MHz, 12k to 20MHz	—	0.05	—	ps

Notes:

1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.

**Phase Noise Plot**



**THERMAL CHARACTERISTICS**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$\theta_{JA}$	Thermal Resistance Junction to Ambient	Still air	—	157	—	°C/W
$\theta_{JC}$	Thermal Resistance Junction to Case	—	—	42	—	°C/W

## Application Information

### Suggest for Unused Inputs and Outputs

#### LVC MOS Input Control Pins

It is suggested to add pullup = 4.7k and pulldown = 1k for LVC MOS pins even though they have internal pullup/pulldown but with much higher value ( $\geq 50k$ ) for higher design reliability.

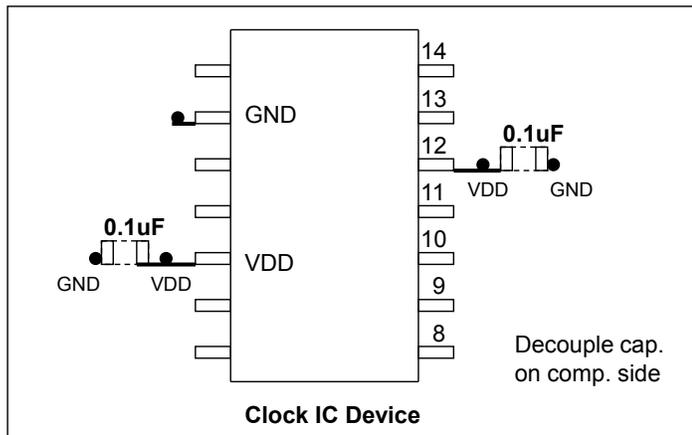
#### Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power consumption.

## Power Decoupling & Routing

### VDD Pin Decoupling

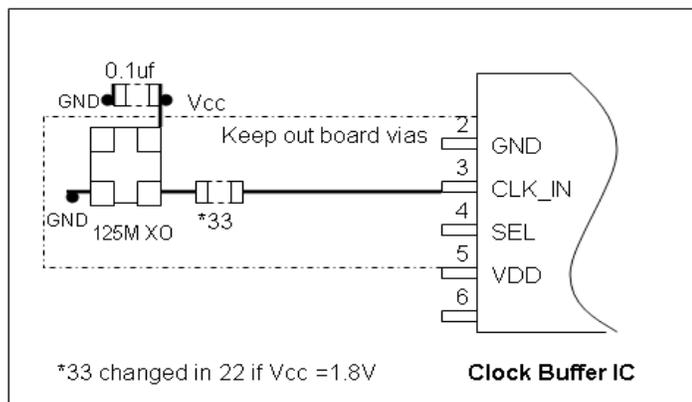
Each VDD pin must have a 0.1 $\mu$ F decoupling capacitor. For better decoupling, 1 $\mu$ F can be used. Placing the decoupling capacitor on the component side improves decoupling filter results, as shown below.



Placement of Decoupling Capacitors

### CMOS Clock Trace Routing

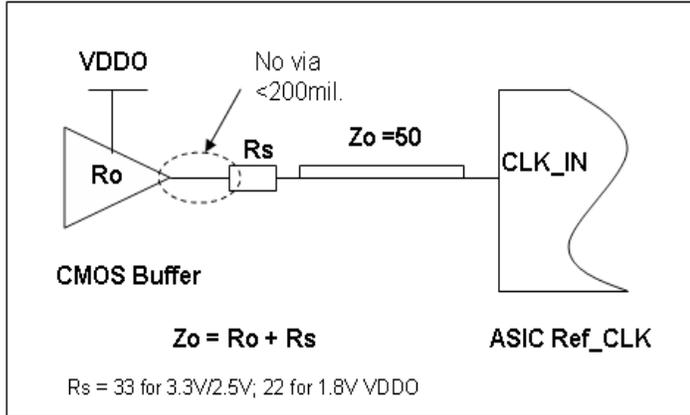
Ensure there is a sufficient keep-out area to the adjacent trace ( $> 20\text{mil.}$ ). In an example using a 125MHz XO driving a buffer IC, it is better to route the clock trace on the component side with a 33 $\Omega$  termination resistor.



## CMOS Output Termination

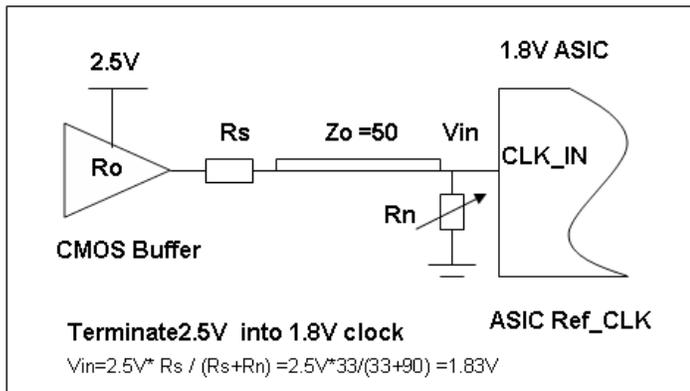
### Popular CMOS Output Termination

The most popular CMOS termination is a serial resistor close to the output pin ( $\leq 200\text{mil}$ ). It is simple and balances the drive strength. The resistor's value can be fine tuned for best performance during board bring-up based on VDDO voltage used.



### Combining Serial and Parallel Termination

Designers can also use a parallel termination for CMOS outputs. For example, a  $50\Omega$  pulldown resistor can be used at the Rx side to reduce signal reflection, but it reduces the signals  $V_{\text{swing}}$  in half. This pulldown can be combined with a serial resistor to form a smaller clock voltage difference. The following diagram shows how to transition a 2.5V clock into 1.8V clock.



$R_s = 33\Omega$  with  $R_n = 100\Omega$ , to transition 3.3V CMOS to 2.5V

$R_s = 43\Omega$  with  $R_n = 70\Omega$  to transition 3.3V CMOS to 1.8V

## Clock Jitter Definitions

### Total jitter= RJ + DJ

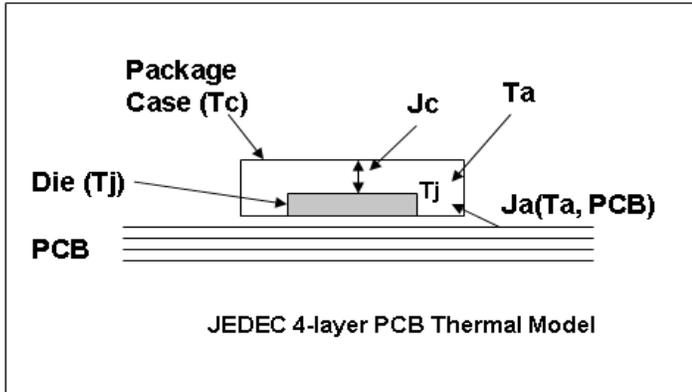
Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related to how long or how many test samples are available. Deterministic jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total jitter (TJ) is the combination of random jitter and deterministic jitter, where factors are based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

### Phase Jitter

Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz @ 10kHz, which is phase noise power in 1-Hz normalized bandwidth vs. the carrier power @ 10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter  $\leq 1\text{ps}$  at 12k to 20MHz offset band as SONET standard specification.

**Device Thermal Calculation**

The JEDEC thermal model in a 4-layer PCB is shown below.



**JEDEC IC Thermal Model**

Important factors to influence device operating temperature are:

- 1) The power dissipation from the chip (P\_chip) is found after subtracting power dissipation from external loads. Generally it can be the no-load device Idd.
- 2) Package type and PCB stack-up structure, for example, 1oz 4-layer board. PCB have more layers and are thicker, which improves heat dissipation.
- 3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature Tj.

The individual device thermal calculation formula:

$$T_j = T_a + P_{chip} \times J_a$$

$$T_c = T_j - P_{chip} \times J_c$$

Ja \_\_\_ Package thermal resistance from die to the ambient air in C/W unit. This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce Ja (still air) by 20% ~ 30%.

Jc \_\_\_ Package thermal resistance from die to the package case in C/W unit.

Tj \_\_\_ Die junction temperature in C (industry limit < 125C max).

Ta \_\_\_ Ambient air temperature in C.

Tc \_\_\_ Package case temperature in C.

Pchip\_\_\_ IC actually consumes power through Iee/GND current.

**Part Marking**

Q Package-2



Z: Die Rev  
Y: Year  
W: Workweek  
1st X: Assembly Code  
2nd X: Fab Code

Q Package-3



Z: Die Rev  
Y: Year  
W: Workweek  
1st X: Assembly Code  
2nd X: Fab Code

**Packaging Mechanical: 8-SOIC (W)**

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.10	—	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	—	1.27
h	0.25	—	0.50
$\theta^\circ$	0	—	8

UNIT : mm

**NOTE :**  
 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES  
 2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS  
 3. REFER JEDEC MS-012

DATE: 02/21/14

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 REVISION: G

15-0103

**For latest package information:**

See <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>.

**Ordering Information**

Ordering Code	Package Code	Package Description	Operating Temperature
PI6C49CB04CQ2WEX	W	8-pin, 150mil-Wide (SOIC)	-40°C to 105°C
PI6C49CB04CQ3WEX	W	8-pin, 150mil-Wide (SOIC)	-40°C to 85°C

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Q = Automotive Compliant
5. 2 and 3 = AEC-Q100 Grade Level
6. E = Pb-free and Green
7. X suffix = Tape/Reel

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