

Ultra-Low Jitter XTAL Oscillator with Fanout

Features

- Generates Five Output Clocks
- Frequency and Output Logic:
 - 156.25 MHz HCSL x 5
- Integrated Quartz Crystal for Frequency Reference
- Typical Phase Noise:
 - 73 fs (Integration Range: 1.875 MHz to 20 MHz)
 - 162 fs (Integration Range: 12 kHz to 20 MHz)
- Complete Ultra-Low Jitter Clocking Solution
- OE on Bank 1 and Bank 2
- 2.5V or 3.3V Operating Voltage Range
- ± 50 ppm Total Stability
- -40°C to $+85^{\circ}\text{C}$ Temperature Range
- 38-Pin 5 mm x 7 mm LGA Package

Applications

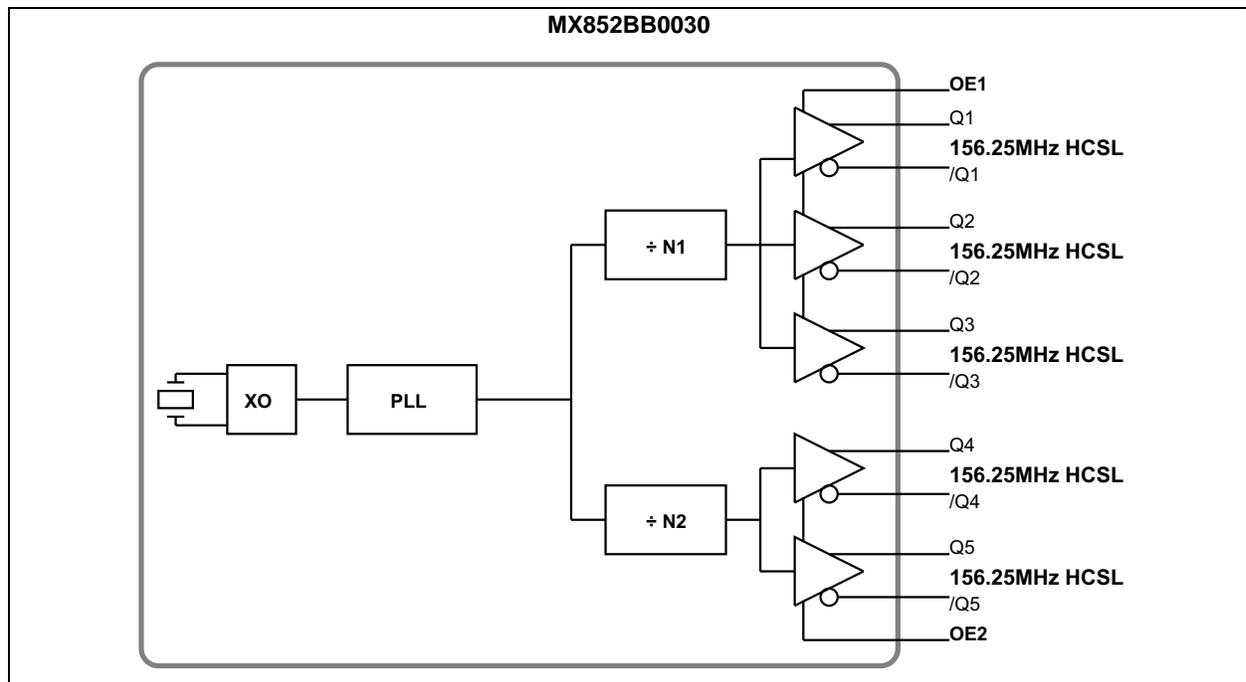
- 10/40/100 Gigabit Ethernet
- Fibre Channel 10G/12G SERDES

General Description

The MX852BB0030 clock management IC (CMIC) is a member of the ClockWorks[®] FUSION family of devices that integrates the crystal, synthesizer, and fanout buffers in a single 5 mm x 7 mm LGA package.

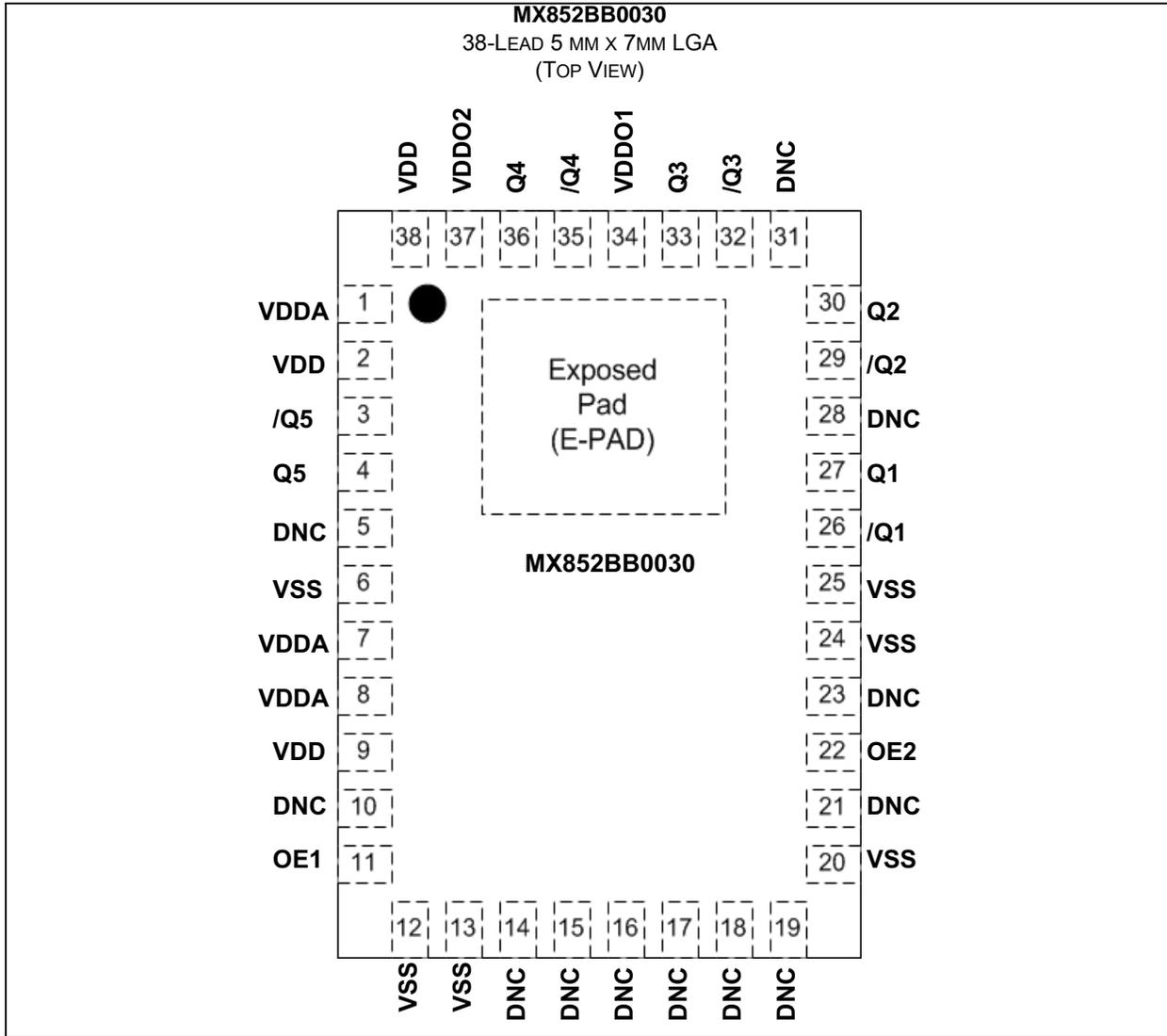
Integrating the entire clock chain delivers 162 fs typical phase noise performance, including fanout and crosstalk. The device operates from a 2.5V or 3.3V power supply.

Block Diagram



MX852BB0030

Package Type



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DDA} , V_{DD} , V_{DDOX})	+4.6V
Input Voltage (V_{IN})	-0.5V to $V_{DD}+0.5V$
ESD Human Body Model Rating	2 kV
ESD Machine Model Rating	200V

Operating Ratings ‡

Supply Voltage (V_{DDOX} , V_{DD} , V_{DDA})	+2.375V to +3.465V
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† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $V_{DD} = V_{DDA} = V_{DDO1} = V_{DDO2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$;
 $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO1} = V_{DDO2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
2.5V Operating Voltage	V_{DDx}	2.375	2.5	2.625	V	—
3.3V Operating Voltage		3.135	3.3	3.465		—
Core Supply Current	I_{DD}	—	—	210	mA	Outputs not loaded.
Output Frequency	f_O	—	156.25	—	MHz	Bank 1 and Bank 2
Frequency Stability	$f_{STABILITY}$	—	—	± 20	ppm	Note 2, Frequency stability over temperature
		—	—	± 50		Total stability
Start-Up Time	t_{START}	—	—	20	ms	—
Output-to-Output Skew	t_{SKEW}	—	—	50	ps	Note 3
Output Rise/Fall Time	t_r/t_f	150	300	450	ps	20% - 80%, HCSL output
Output Duty Cycle	ODC	48	50	52	%	<350 MHz output frequencies
RMS Phase Noise 156.25 MHz HCSL	$t_{jit}(\emptyset)$	—	73	—	fs	Integration range (1.875 MHz to 20 MHz)
		—	162	—		Integration range (12 kHz to 20 MHz)
		—	260	—		Integration range (12 kHz to 40 MHz)
Period Jitter	$t_{jit}(\emptyset)$	—	1.6	5	ps	Peak-to-peak (E5001A, 100 Hz to 40 MHz)
		—	135	—	fs	RMS (E5001A, 100 Hz to 40 MHz)
		—	5	10	ps	Peak-to-peak (10k Samples, DSA80000B)

Note 1: The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics table after thermal equilibrium has been established.

- 2:** Inclusive of temperature drift, aging, initial accuracy, shock, and vibration. Operating temperature range dependent on part number configuration.
- 3:** Skew between output buffers. Measured at the output differential crossing points. Applies to outputs at the same supply voltage using same output format.

TABLE 1-2: LVCMOS INPUTS DC ELECTRICAL CHARACTERISTICS (OE1, OE2)(Note 1)

Electrical Characteristics: $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	2	—	$V_{DD} + 0.3$	V	—
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	—
Input High Current	I_{IH}	—	—	150	μA	$V_{DD} = V_{IN} = 3.465V$
Input Low Current	I_{IL}	-150	—	—	μA	$V_{DD} = 3.465V, V_{IN} = 0V$

Note 1: The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics table after thermal equilibrium has been established.

TABLE 1-3: HCSL DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $V_{DD} = V_{DDO1} = V_{DDO2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$;

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO1} = V_{DDO2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$; $T_A = -40^\circ C$ to $+85^\circ C$, $R_L = 50\Omega$ to V_{SS}

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	640	700	850	mV	—
Output Low Voltage	V_{OL}	-150	0	27	mV	—
Crossing Point Voltage	V_{CROSS}	250	350	550	mV	—

Note 1: The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics table after thermal equilibrium has been established.

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature	T_S	-65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature	T_A	-40	—	+85	°C	—
Package Thermal Resistance						
Thermal Resistance 38-Ld LGA	θ_{JA}	—	38.5	—	°C/W	Still Air

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Pin Level	Description
1, 7, 8	VDDA	PWR	—	Analog Power Supply
2, 9, 38	VDD	PWR	—	Power Supply
3, 4	/Q5, Q5	O, Diff	HCSL	Bank 2 Clock Output Frequency = 156.25 MHz
5, 14, 15, 16, 17, 18, 19, 21, 23, 28, 31	DNC	—	—	Do not connect anything to these pins.
6, 24, 25, ePAD	VSS (Exposed Pad)	PWR	—	Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
10	DNC	—	—	Do not connect.
11	OE1	I, SE	LVC MOS	Output Enable, Bank 1 outputs disable to tri-state, 0 = Disabled, 1 = Enabled, 45 kΩ pull-up.
12, 13, 20	VSS	PWR	—	Crystal Ground
22	OE2	I, SE	LVC MOS	Output Enable, Bank 2 outputs disable to tri-state, 0 = Disabled, 1 = Enabled, 45 kΩ pull-up.
26, 27	/Q1, Q1	O, Diff	HCSL	Bank 1 Clock Output Frequency = 156.25 MHz
29, 30	/Q2, Q2	O, Diff	HCSL	Bank 1 Clock Output Frequency = 156.25 MHz
32, 33	/Q3, Q3	O, Diff	HCSL	Bank 1 Clock Output Frequency = 156.25 MHz
34	VDDO1	PWR	—	Power Supply for the outputs on Bank 1
35, 36	/Q4, Q4	O, Diff	HCSL	Bank 2 Clock Output Frequency = 156.25 MHz
37	VDDO2	PWR	—	Power Supply for the outputs on Bank 2

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3.0 APPLICATION INFORMATION

3.1 Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30Ω resistor in series with the output, as close as possible to the output pin and start a 50Ω trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50Ω traces.

For EMI reasons, it is better to use a balanced differential design. LVDS can be AC-coupled or DC-coupled to its termination.

3.2 Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7 nF below) between the V_{DD} and V_{SS} pins, as close as possible to those pins and on the same side of the PCB as the IC. The shorter the physical path from V_{DD} to the capacitor and back from the capacitor to V_{SS} , the more effective the decoupling. Use one 4.7 nF capacitor for each V_{DD} pin.

The impedance value of the Ferrite Bead (FB) needs to be between 80Ω and 240Ω with a saturation current ≥ 250 mA.

The V_{DDO1} and V_{DDO2} pins connect directly to the V_{DD} plane. All V_{DD} pins connect to V_{DD} after the power supply filter.

4.0 POWER SUPPLY FILTERING RECOMMENDATIONS

Preferred filtering, using a Microchip MIC94325 Ripple Block, is shown in Figure 4-1.

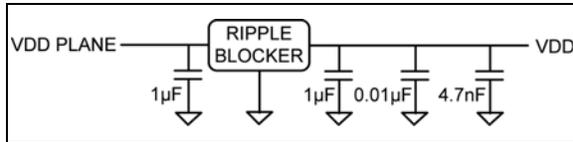


FIGURE 4-1: Preferred Filtering.

Figure 4-2 shows an alternative, traditional filter, using a ferrite bead.

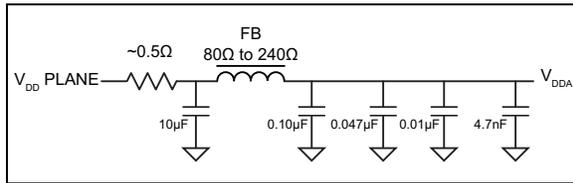


FIGURE 4-2: VDDA (Analog) Traditional Pi Filter.

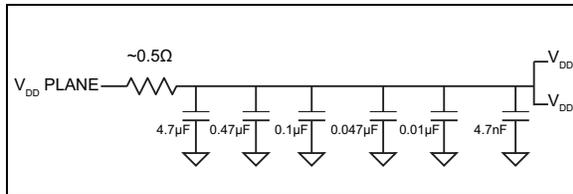


FIGURE 4-3: Recommended Power Supply Filtering.

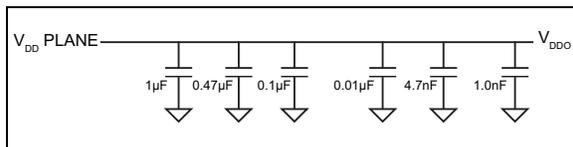


FIGURE 4-4: Recommended Decoupling for Each VDDO.

5.0 TIMING DIAGRAMS

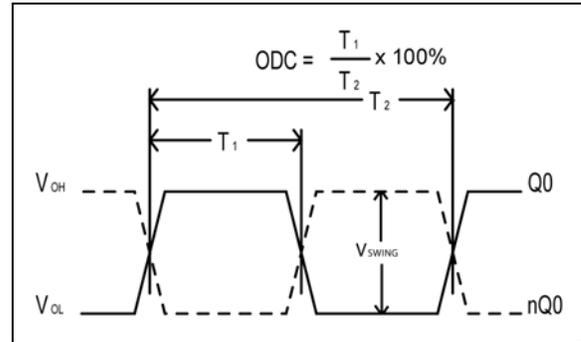


FIGURE 5-1: Duty Cycle Timing.

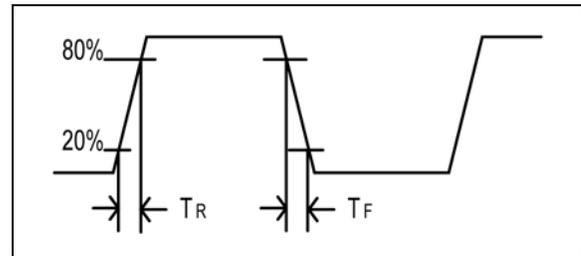


FIGURE 5-2: All Outputs Rise/Fall Time.

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6.0 RMS PHASE/NOISE/JITTER

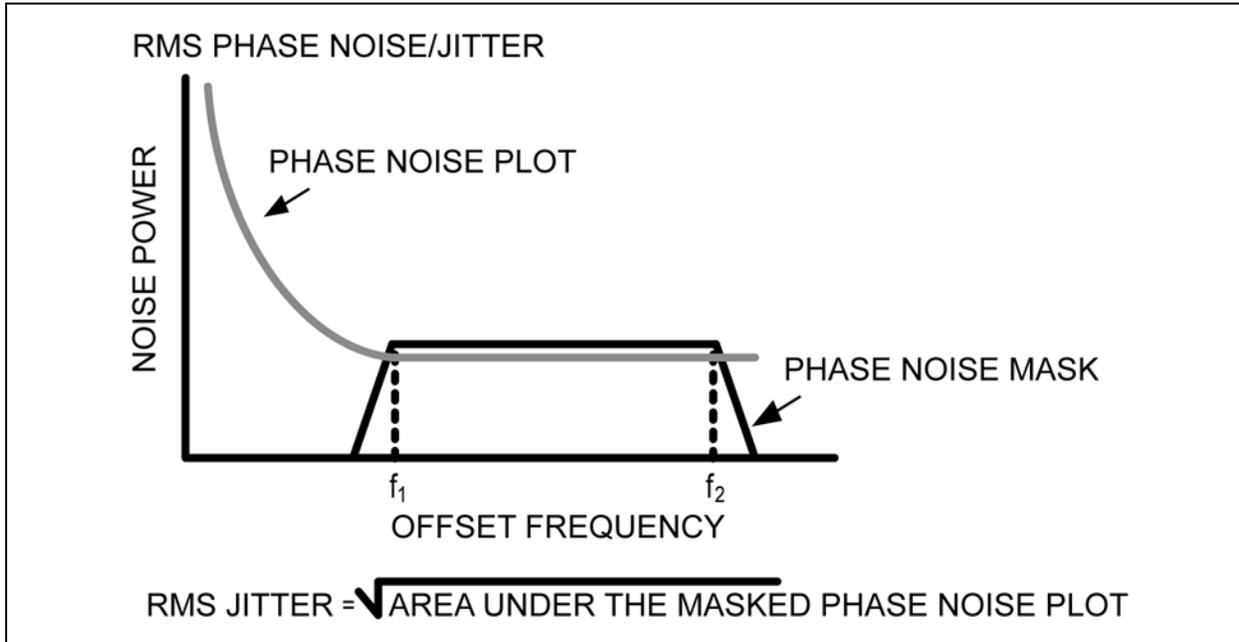


FIGURE 6-1: RMS Phase/Noise/Jitter.

7.0 OUTPUT TERMINATION

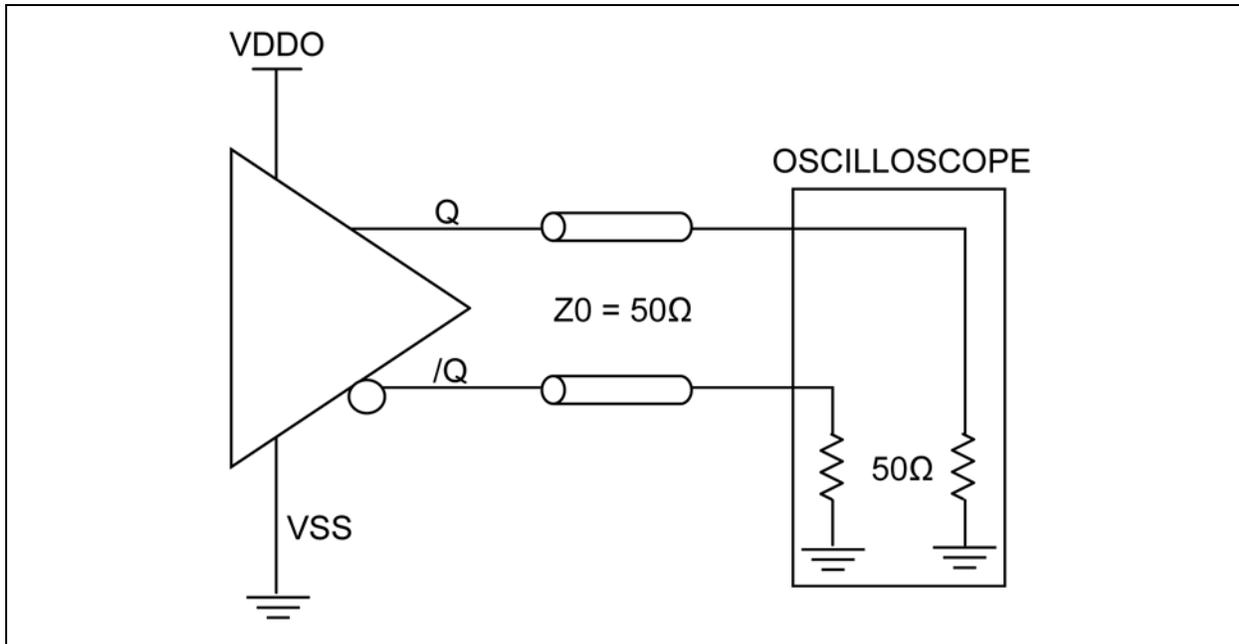


FIGURE 7-1: HCSL Output Load and Test Circuit.

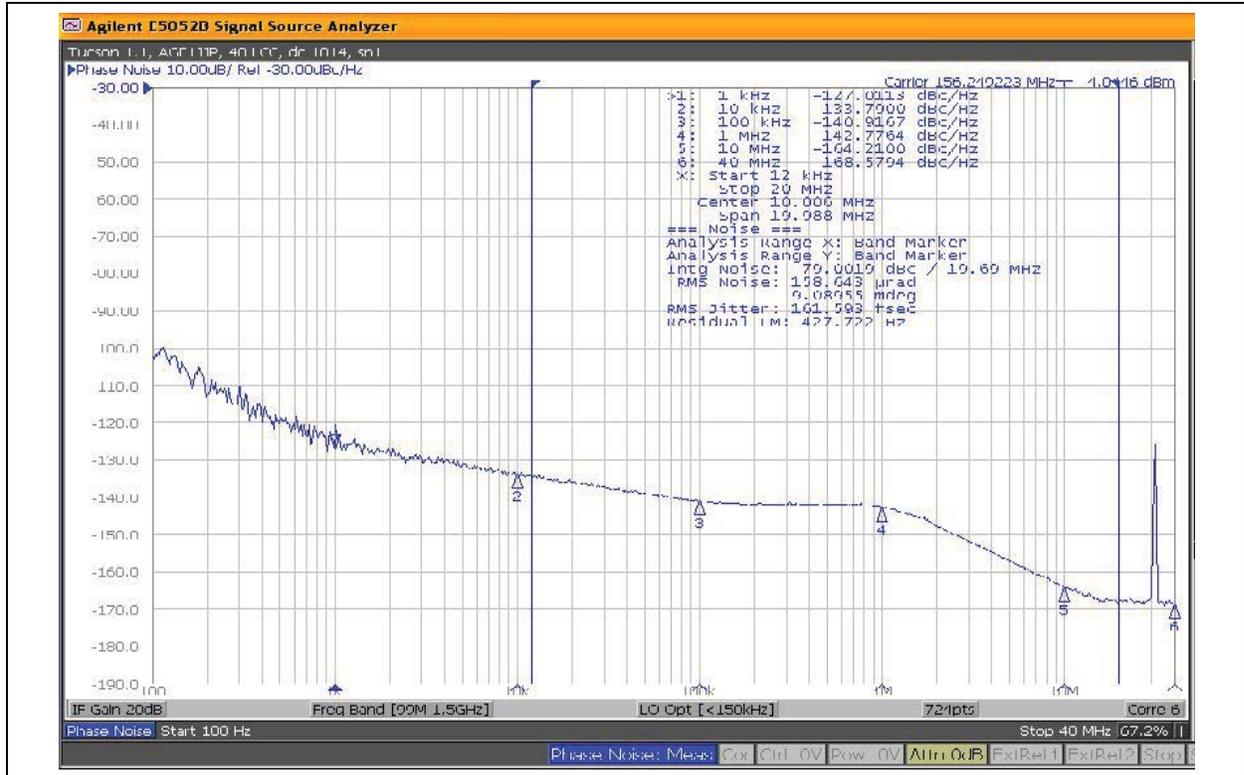


FIGURE 7-2: 156.25 MHz HCSL Output, 12 kHz to 20 MHz, 162 fs

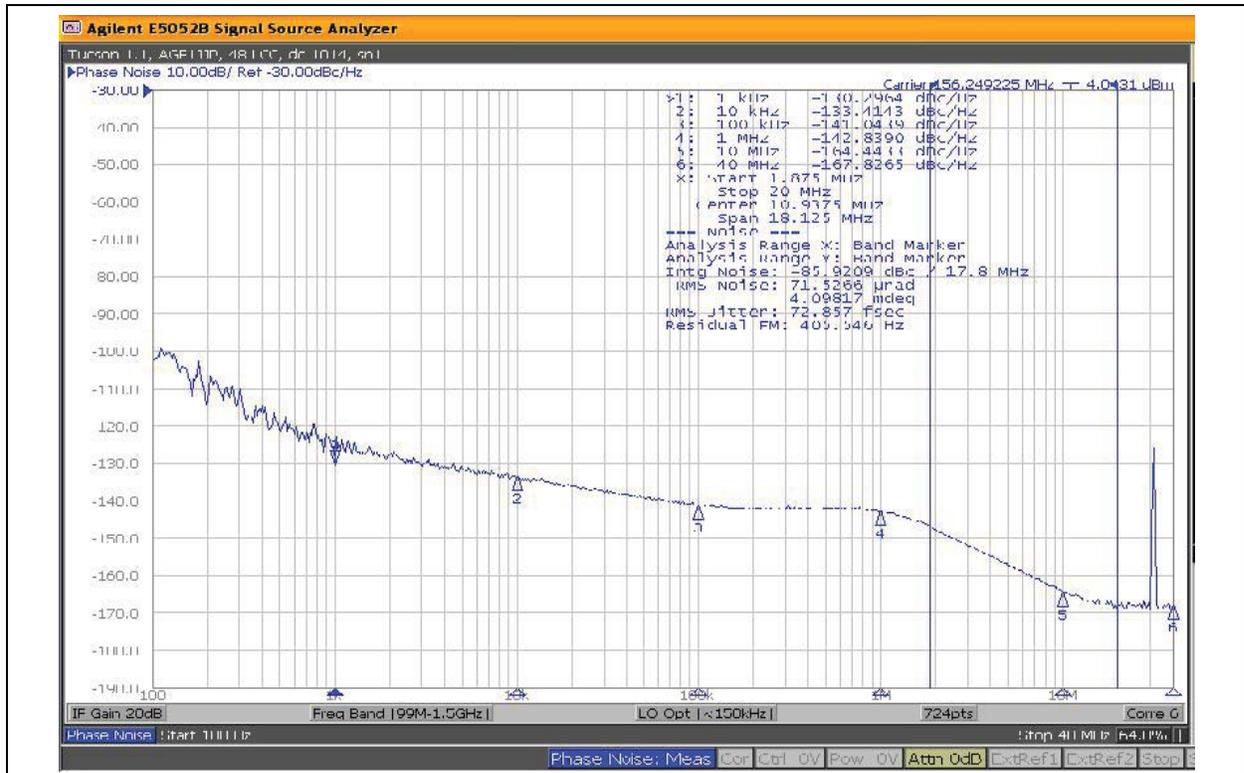


FIGURE 7-3: 156.25 MHz HCSL Output, 1.875 MHz to 20 MHz, 73 fs

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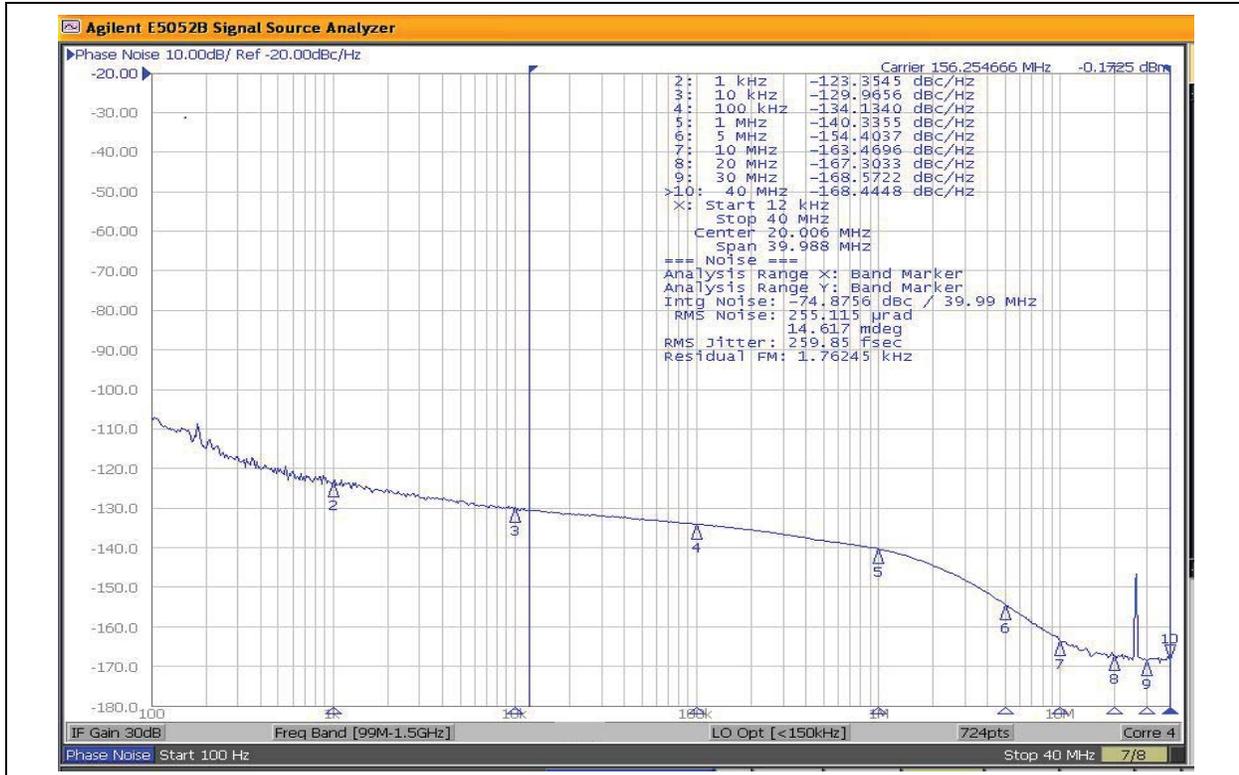


FIGURE 7-4: 156.25 MHz HCSL Output, 12 kHz to 40 MHz, 260 fs

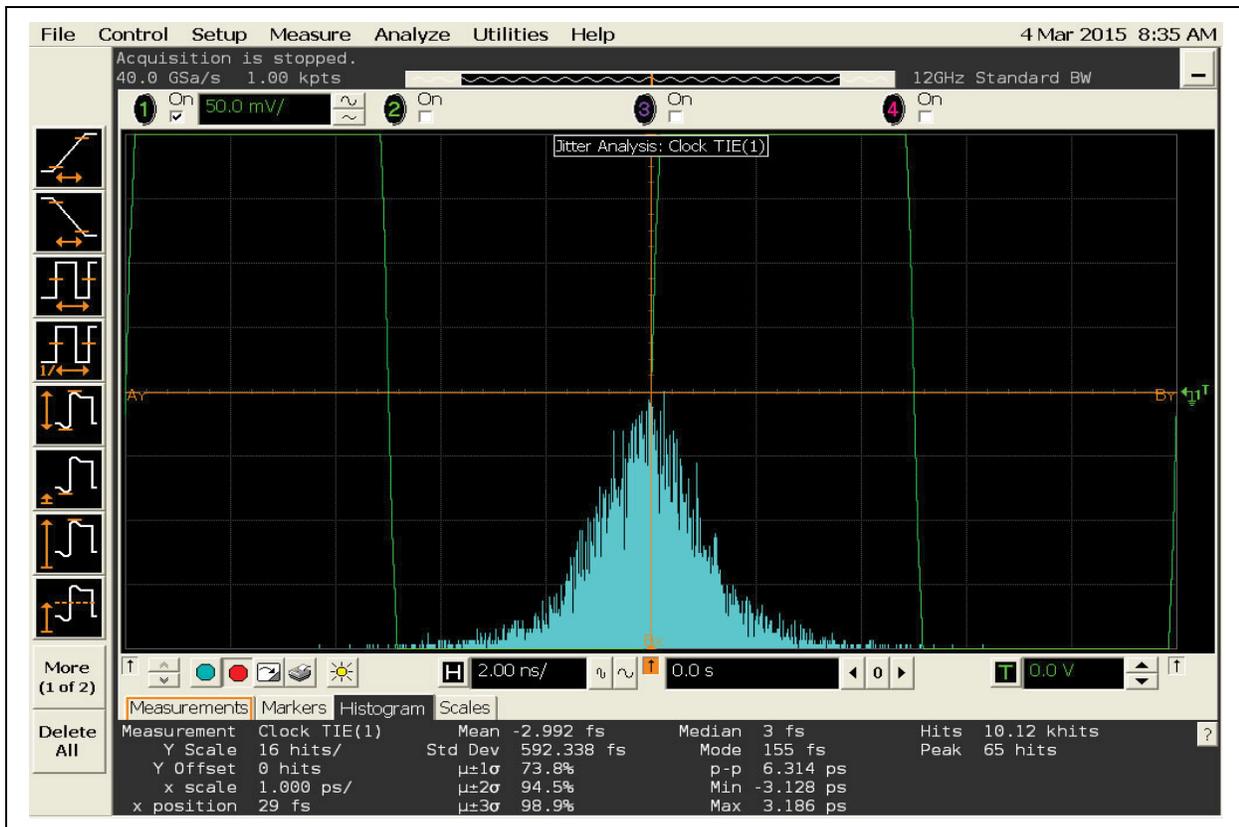
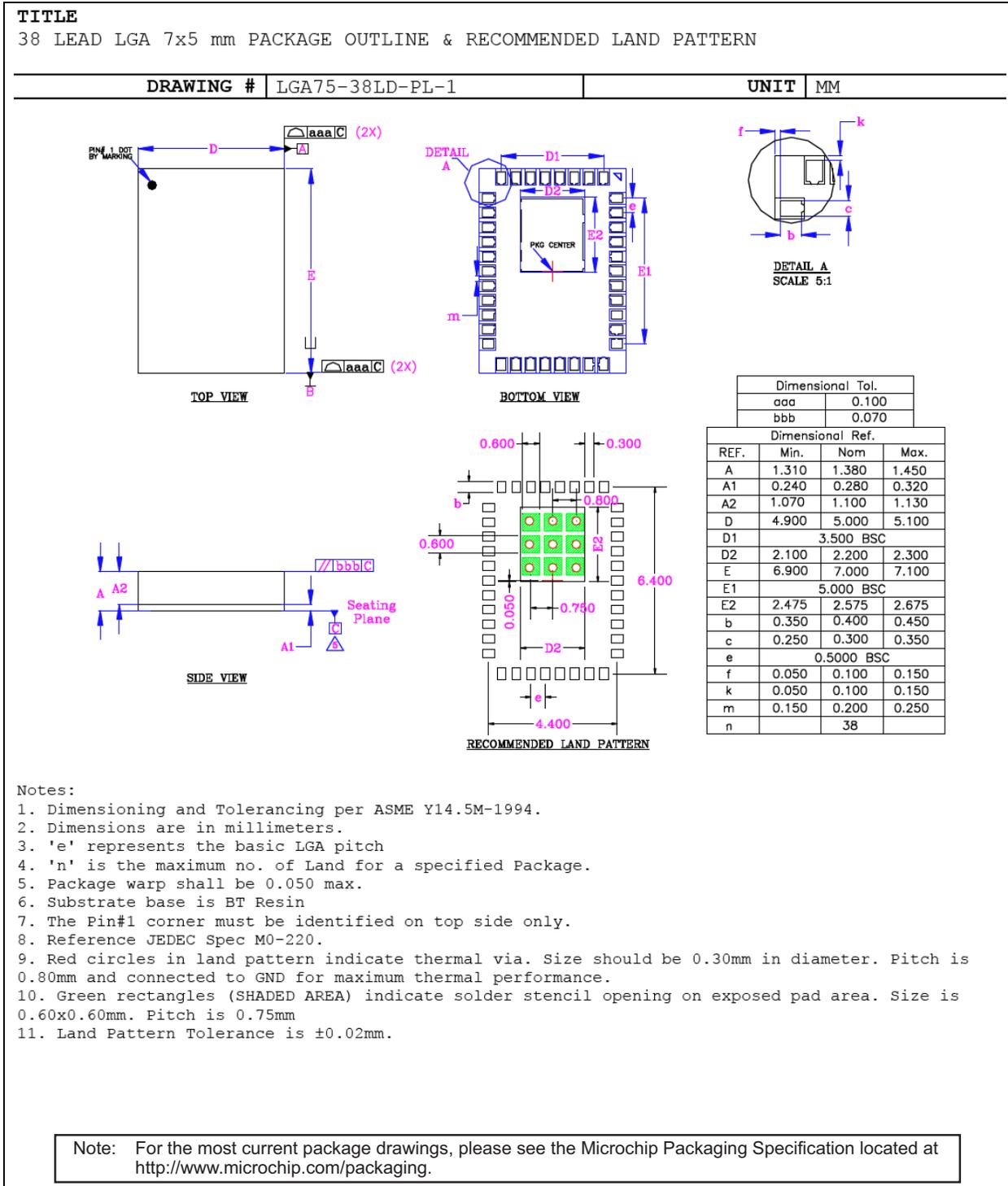


FIGURE 7-5: TIE Jitter (10k Samples).

8.0 PACKAGING INFORMATION

38-Lead LGA Package Outline and Recommended Land Pattern



MX852BB0030

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document MX852BB0030 to Microchip data sheet DS20005737A.
- Minor text changes throughout.

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NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>		-	<u>XX</u>
Device			Media Type
Device:	MX852BB0030: Ultra-Low Jitter 5 HCSSL Output Oscillator at 156.25 MHz		
Media Type:	(blank)= 43/Tube TR = 1,000/Reel		

Examples:

- a) MX852BB0030: Ultra-Low Jitter 5 HCSSL Output Oscillator at 156.25 MHz, 43/Tube
- b) MX852BB0030-TR: Ultra-Low Jitter 5 HCSSL Output Oscillator at 156.25 MHz, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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ISBN: 978-1-5224-3612-6



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